To: T10 Technical Committee
From: Rob Elliott, HP (elliott@hp.com)
Date: 30 May 2007
Subject: 07-091r3 SAS-2 SMP DISCOVER support for SNW-3 phy capabilities

Revision history

Revision 0 (28 February 2007) First revision (offshoot of 06-362r3).

Revision 1 (12 April 2007) Incorporated comments from March 2007 SAS physical WG - added mode page/log page support and SNW selection. Restructured the SNW-3 bit definitions into the traditional "byte\bit" table format rather than a single little-endian bitstream. Per request by Bob Sheffield (Intel), changed the PROGRAMMED PHY CAPABILITIES field from containing only the changeable bits that the application client has selected to containing the full set of bits (including START and PARITY) that are scheduled to be sent in the next SNW-3.

Revision 2 (2 May 2007) Incorporated comments from April 2007 SAS protocol/physical WG. Moved mode page/log page changes to a separate proposal 07-214 (and an independent, possibly supporting proposal 07-215).

Revision 3 (30 May 2007) Incorporated comments from May 2007 SAS protocol WG - added a NEGOTIATED SSC BIT to DISCOVER, clarified meaning of "supported" and "valid" in SNW text. Moved PHY CONTROL changes to a separate proposal. Restored supported settings priority table for the settings bits from 06-515r0 (which was missed when that proposal was incorporated into sas2r08).

Related documents

sas2r08 - Serial Attached SCSI - 2 (SAS-2) revision 8

06-324/06-515 SAS-2 SAS-2 Modifications to speed negotiation (Steve Finch, ST Microelectronics and Amr Wassal, PMC-Sierra) - incorporated into sas2r08

06-363r3 SAS-2 SNW-3 bit definitions (Rob Elliott, HP) - incorporated into 06-324r7

07-214 - SAS-2 Mode and log page support for SNW-3 phy capabilities (Rob Elliott, HP)

07-215 - SPC-4 Protocol-Specific log page subpages (Rob Elliott, HP)

Overview

Applications need to be able to access the SNW-3 phy capabilities bits to determine the current operating settings.

1. Fields are added to the SMP DISCOVER response for phys controlled by management device servers:

a) incoming SNW-3 phy capabilities bits last received by the phy
b) outgoing SNW-3 phy capabilities bits last sent by the phy
c) outgoing SNW-3 phy capabilities bits that will be sent by the phy in the next SNW-3
d) negotiated SSC. The negotiated PHYSICAL LINK RATE field indicates the physical link rate, but does not indicate if SSC ended up enabled or disabled.

07-214 defines mode page/log page equivalents of these for phys controlled by SCSI device servers.

2. The SNW-3 bit definitions are restructured to follow usual SCSI conventions of Byte\bit tables, rather than include one little-endian bit stream with bits numbered 0 through 31.

3. The definition of each SNW being "supported" and "valid" is clarified. Supported means the phy is going to transmit something other than D.C. idle and attempt to receive something; not supported means it is silent. Valid means the window was a success (both phys seem to have supported it). For SNW-1, SNW-2, Final-SNW, and Train-SNW, valid also means the speed negotiation was successful. For SNW-3, valid just means phy capabilities bits were transmitted and at least one was received; it does not consider whether parity is good or bad or whether there are any commonly supported settings.

4. All speed negotiation figures (including in annex B) are updated to indicate "valid" or "invalid", use the term "phy capabilities", and make other changes for consistency.

5. Restored the supported settings priority table for the settings bits from 06-515r0, which was missed when that proposal was incorporated into sas2r08.

Suggested changes to SAS-2

6.7.4.2 SAS speed negotiation sequence

6.7.4.2.1 SAS speed negotiation sequence overview

The SAS speed negotiation sequence establishes communications between the two phys of a physical link at the highest possible transmission rate.

The SAS speed negotiation sequence is a peer-to-peer negotiation technique that does not assume initiator and target (i.e., host and device) roles. The rules for speed negotiation are the same for both participating phys.

The SAS speed negotiation sequence consists of a set of speed negotiation windows (SNWs). Each ~~speed negotiation window~~SNW is identified by a name (e.g., Speed Negotiation Window-1 or SNW-1).

~~Speed negotiation window~~SNWs conform to one of three defined formats:

a) speed negotiation without training: SNW-1, SNW-2 and Final-SNW (see 6.7.4.2.3.2);
b) phy capabilities exchange: SNW-3 (see 6.7.4.2.3.3); and
c) speed negotiation with training: Train-SNW (see 6.7.4.2.3.4).

Many of the timing parameters used for defining the ~~speed negotiation window~~SNWs are common to multiple ~~window~~SNW types. All of the timing specifications for all ~~speed negotiation window~~SNW types are defined in 6.7.4.2.2.

A SAS speed negotiation sequence may or may not include all three types of ~~speed negotiation window~~SNWs. Phys may implement a subset of ~~speed negotiation window~~SNWs provided that the subset implements a valid speed negotiation sequence. SAS speed negotiation sequences are defined in 6.7.4.2.4.

The transmitter device shall use SAS signal output levels during the SAS speed negotiation sequence as described in 5.3.6.5.

6.7.4.2.2 SAS speed negotiation sequence timing specifications

Table 81 defines the timing specifications for the SAS speed negotiation ~~windows~~sequence.

Table 81 — SAS speed negotiation sequence timing specifications (part 1 of 2)

Parameter	Acronym	Time [a]	Comments
Rate change delay time	RCDT	750 000 OOBI [b]	The time the transmitter device shall transmit D.C. idle at the beginning of SNW-1, SNW-2, SNW-3, Final-SNW, and Train-SNW.
Speed negotiation transmit time	SNTT	163 840 OOBI [c]	During SNW-1, SNW-2, and Final-SNW, the time after RCDT during which ALIGN (0) or ALIGN (1) is transmitted ~~at each physical link rate during the speed negotiation sequence~~. During SNW-3, the time after RCDT in which bit cells and D.C. idle are transmitted.
Speed negotiation lock time	SNLT	153 600 OOBI [d]	The maximum time ~~during SNW-1, SNW-2, and Final-SNW~~ for a ~~transmitter device~~phy to reply with ALIGN (1) during SNW-1, SNW-2, and Final-SNW.
Actual lock time	ALT		The time during SNW-1, SNW-2, and Final-SNW at which actual dword synchronization occurs to the received ALIGN (0) or ALIGN (1) and the ~~transmitter~~phy begins transmitting ALIGN (1) rather than ALIGN (0).
~~Speed negotiation window~~SNW time	SNWT	913 840 OOBI [e]	The duration of SNW-1, SNW-2, SNW-3, or Final-SNW.
Bit cell time	BCT	2 200 OOBI [i]	The time to transmit a COMWAKE or D.C. idle during SNW-3.
Maximum training time	MTT	29 998 080 OOBI [f]	The maximum time for training to complete during Train-SNW.
Training lock time	TLT	28 497 920 OOBI [g]	The maximum time for a ~~transmitter device~~phy to reply with TRAIN_DONE during Train-SNW.

[a] OOBI is defined in table 73 (see 6.6.1).
[b] 750 000 OOBI (e.g., RCDT) is nominally 500 µs. Equal to: 18 750 x 40.
[c] 163 840 OOBI (e.g., SNTT) is nominally 109,226 µs. Equal to: 4 096 x 40.
[d] 153 600 OOBI (e.g., SNLT) is nominally 102,4 µs. Equal to: (4 096 - 256) x 40.
[e] 913 840 OOBI (e.g., SNWT) is nominally 609,226 µs. Equal to: RCDT + SNTT.
[f] 29 998 080 OOBI (e.g., MTT) is nominally 19,998 719 ms. Equal to: 11 718 x 64 x 40. This is the time of the maximum number of complete training patterns that fit into 20 ms.
[g] 28 497 920 OOBI (e.g., TLT) is nominally 18,998 613 ms. Equal to: 11 132 x 64 x 40. This is the time of the maximum number of complete training patterns that fit into 19 ms.
[h] 30 748 080 OOBI (e.g., MTWT) is nominally 20,498 719 ms. Equal to: RCDT + MTT.
[i] 2 200 OOBI is nominally 1,466.6 µs. Equal to the COMWAKE signal time (see table 74 in 6.6.2).

Table 81 — SAS speed negotiation sequence timing specifications (part 2 of 2)

Parameter	Acronym	Time [a]	Comments
Actual training time	ATT		The time ~~in~~at which training of the receiver is complete.
Train-SNW ~~window~~ time	TWT		The actual duration of Train-SNW.
Maximum Train-SNW ~~window~~ time	MTWT	30 748 080 OOBI [h]	The maximum duration of Train-SNW.

[a] OOBI is defined in table 73 (see 6.6.1).
[b] 750 000 OOBI (e.g., RCDT) is nominally 500 µs. Equal to: 18 750 x 40.
[c] 163 840 OOBI (e.g., SNTT) is nominally 109,226 µs. Equal to: 4 096 x 40.
[d] 153 600 OOBI (e.g., SNLT) is nominally 102,4 µs. Equal to: (4 096 - 256) x 40.
[e] 913 840 OOBI (e.g., SNWT) is nominally 609,226 µs. Equal to: RCDT + SNTT.
[f] 29 998 080 OOBI (e.g., MTT) is nominally 19,998 719 ms. Equal to: 11 718 x 64 x 40. This is the time of the maximum number of complete training patterns that fit into 20 ms.
[g] 28 497 920 OOBI (e.g., TLT) is nominally 18,998 613 ms. Equal to: 11 132 x 64 x 40. This is the time of the maximum number of complete training patterns that fit into 19 ms.
[h] 30 748 080 OOBI (e.g., MTWT) is nominally 20,498 719 ms. Equal to: RCDT + MTT.
[i] 2 200 OOBI is nominally 1,466.6 µs. Equal to the COMWAKE signal time (see table 74 in 6.6.2).

6.7.4.2.3 Speed negotiation window (SNW) definitions

6.7.4.2.3.1 ~~Speed negotiation window~~SNW definitions overview

During each ~~speed negotiation window~~SNW, a phy shall either:

a) transmit and receive as defined for the ~~speed negotiation window~~SNW if it supports the SNW; or
b) transmit D.C. idle and not receive if it does not support the SNW.

If a phy ~~transmits as defined for the speed negotiation window~~supports the SNW and receives the expected transmission, then the ~~speed negotiation window~~SNW is valid. [join] If a phy does not receive the expected transmission from the attached phy, then the ~~speed negotiation window~~SNW is invalid.

NOTE 1 - If a phy transmits D.C. idle during a ~~speed negotiation window~~SNW, then the attached phy ~~may~~does not receive the expected transmission and the ~~speed negotiation window~~SNW is invalid.

6.7.4.2.3.2 SNW-1, SNW-2, and Final-SNW

Figure 127 defines the ~~speed negotiation window~~SNW format for SNW-1, SNW-2, and Final-SNW, including:

a) speed negotiation window time (SNWT);
b) rate change delay time (RCDT);
c) speed negotiation transmit time (SNTT);
d) speed negotiation lock time (SNLT); and

e) actual lock time (ALT).

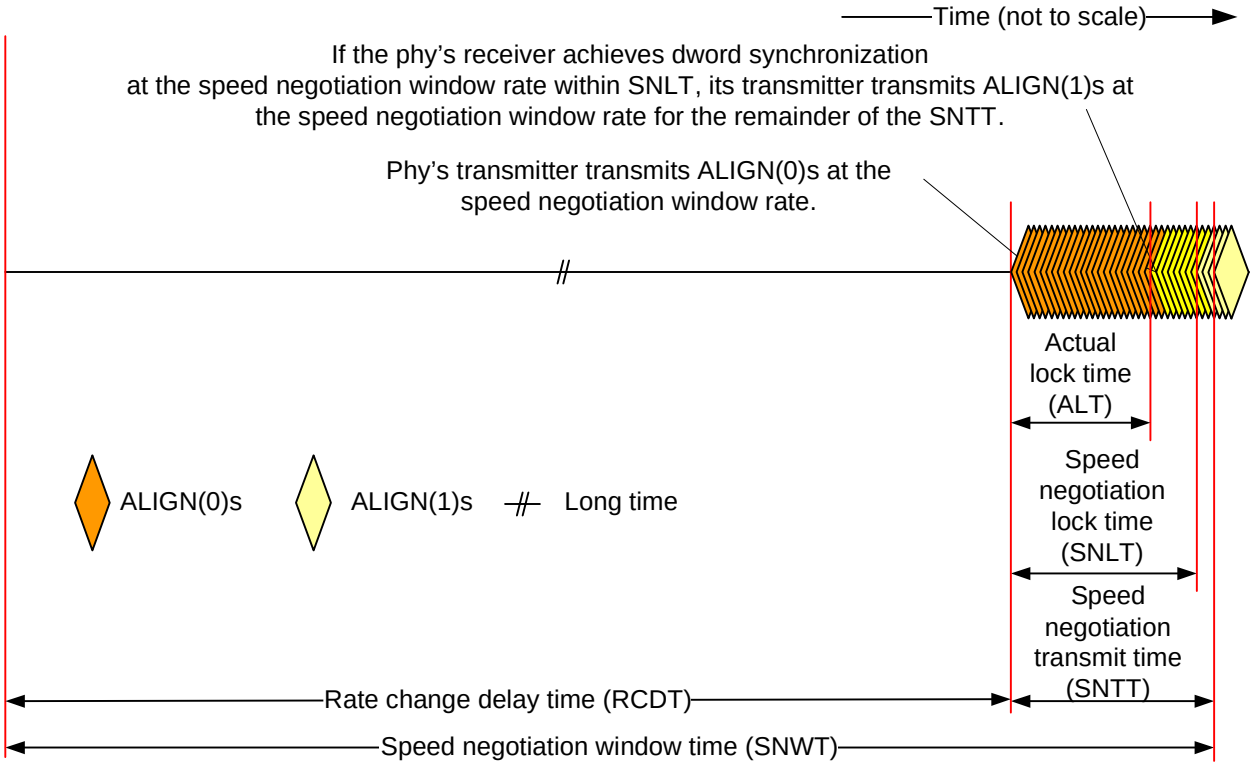

Figure 127 — SNW-1, SNW-2, and Final-SNW

If the phy supports the ~~physical link rate~~SNW, the ~~speed negotiation windowshall consist of the following transmission sequence~~phy shall transmit:

1) ~~transmission of~~ D.C. idle for an RCDT; and
2) ~~if the phy supports the physical link rate, transmission of~~ ALIGNs at ~~that physical link~~the SNW rate for the remainder of the SNWT (i.e., for SNTT).

If the phy does not support the ~~physical link rate~~SNW, the phy shall transmit ~~transmission of~~ D.C. idle for the entire SNWT.

Table 82 defines the ~~speed negotiation window~~SNW rate used in SNW-1, SNW-2, and Final-SNW.

Table 82 — ~~Speed negotiation window~~SNW rates used in SNW-1, SNW-2, and Final-SNW

SNW	~~Speed negotiation window~~SNW rate
SNW-1	1,5 Gbps
SNW-2	3 Gbps
Final-SNW	Based on SNW-1, SNW-2, and SNW-3 validity: a) 1,5 Gbps if SNW-1 is valid and SNW-2 is invalid; and b) 3 Gbps if SNW-2 is valid and SNW-3 is invalid.

If the phy supports the ~~speed negotiation window~~SNW ~~rate~~, it shall attempt to synchronize on an incoming series of dwords at that rate for the SNLT after RCDT. The received dwords may be ALIGN (0) or ALIGN (1) primitives. If the phy achieves dword synchronization within the SNLT, it shall change from transmitting ALIGN (0) primitives to transmitting ALIGN (1) primitives for the remainder of the SNTT (i.e., the remainder of the~~speed negotiation window~~SNW time). The point at which the phy achieves dword synchronization is called the actual lock time (ALT). If the phy does not achieve dword synchronization within the SNLT, it shall continue

transmitting ALIGN (0) primitives for the remainder of the SNTT (i.e., the remainder of the ~~speed negotiation window~~SNW).

At the end of the SNTT, if a phy is both transmitting and receiving ALIGN (1) primitives, it shall consider the SNW to be valid. If the phy is not both transmitting and receiving ALIGN (1) primitives, it shall consider the SNW to be invalid.

The phy shall ~~enable or disable SSC~~transmit with SSC disabled (see 5.3.8) during SNW-1, SNW-2, and Final-SNW.

6.7.4.2.3.3 SNW-3 [with some text reordered]

SNW-3 allows the phys to exchange phy capabilities ~~values indicating supported settings and other information~~ to establish phy parameters used in Train-SNW.

Figure 128 defines SNW-3, including:

a) ~~speed negotiation window~~SNW time (SNWT);
~~b) speed negotiation window rate of 1,5 Gbps;~~
c) rate change delay time (RCDT); and
d) speed negotiation transmit time (SNTT).

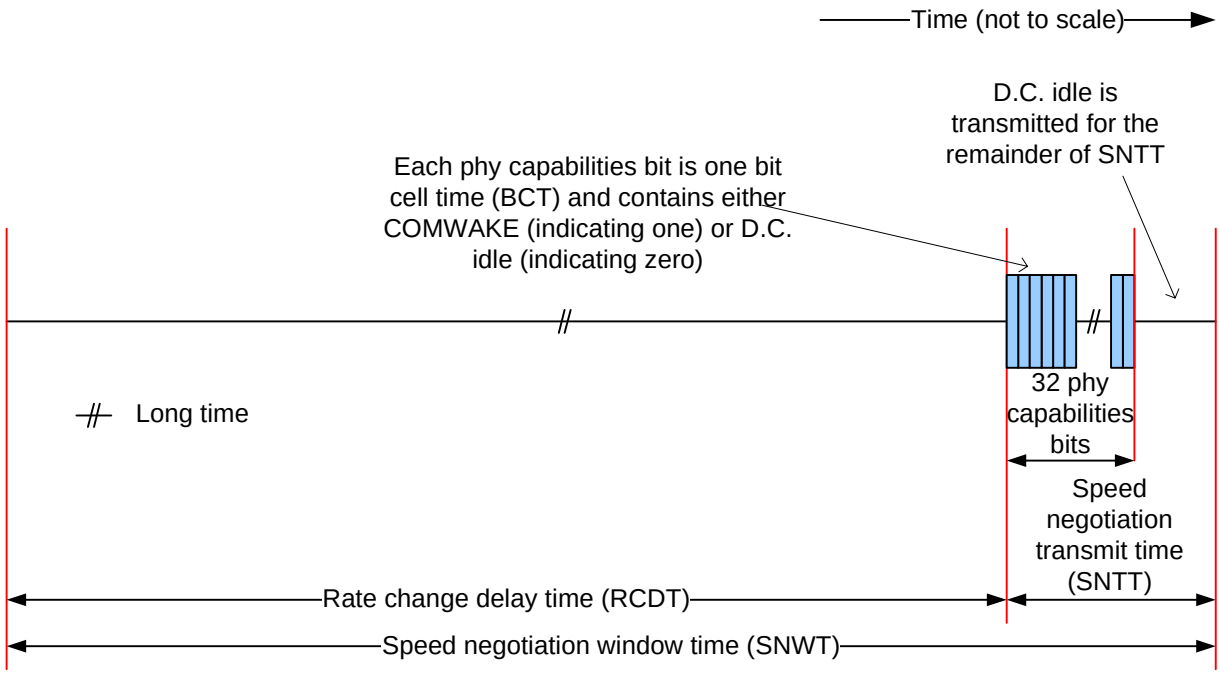

Figure 128 — SNW-3

Table 83 defines the content of each phy capabilities bit.

Table 83 — SNW-3 phy capabilities bit

Value	Transmitted
One	COMWAKE (see 6.6)
Zero	D.C. idle

~~If a phy supports SNW-3, then the phy:~~

~~a) transmits a 32-bit phy capabilities value describing the capabilities of the phy; and~~
~~b) receives a 32-bit phy capabilities value from the attached phy. If the attached phy does not support SNW-3, the phy capabilities bits are all set to zero (i.e., D.C. idle).~~

~~If a phy does not support SNW-3, then the phy:~~

~~a) transmits D.C. idle; and~~
~~b) ignores any SNW-3 phy capabilities bits received.~~

If the phy supports SNW-3, the phy ~~The transmitter~~ shall:

1) transmit D.C. idle for an RCDT;
2) transmit 32 phy capabilities bits; and
3) transmit D.C. idle for the remainder of SNTT.

and shall receive a 32-bit phy capabilities value from the attached phy. If the attached phy does not support SNW-3, the phy capabilities bits are all set to zero (i.e., D.C. idle).

If the phy does not support SNW-3, the phy shall transmit D.C. idle for the entire SNWT and ignore any SNW-3 phy capabilities bits received.

The first ~~bit of the~~ phy capabilities ~~value~~bit is the START bit and ~~shall be transmitted as a one~~is set to one. Each of the remaining 31 phy capabilities bits is ~~a~~set to one or zero. The receiver shall use the START bit to detect the beginning of the phy capabilities bits.

The phy shall consider SNW-3 to be valid if it supports SNW-3 and receive at least one phy capabilities bit set to one. If the phy does not support SNW-3 or does not receive at least one phy capabilities bit set to one, it shall consider SNW-3 to be invalid.

The phy may ~~enable or disable SSC~~transmit with SSC enabled or disabled (see 5.3.8) during SNW-3.

~~Table 84 defines the SNW-3 phy capabilities bits. For each bit defined as reserved, the phy shall transmit a zero (i.e., D.C. idle) and shall ignore the received value.~~

~~Table 84 — SNW-3 phy capabilities bits~~

~~Bit(s)~~	**~~Description~~**	**~~Changeable~~** [a]
~~Header~~		
~~0 (first bit)~~	~~START bit~~	~~no~~
~~1~~	~~TX SSC TYPE bit~~	~~no~~
~~2 to 3~~	~~Reserved~~	~~no~~
~~4 to 7~~	~~REQUESTED LOGICAL LINK RATE field bit 4 is the MSB; bit 7 is the LSB~~	~~no~~
~~Supported settings bits~~		
~~8~~	~~G1 WITHOUT SSC SUPPORTED bit~~	~~yes~~
~~9~~	~~G1 WITH SSC SUPPORTED bit~~	~~yes~~
~~10~~	~~G2 WITHOUT SSC SUPPORTED bit~~	~~yes~~
~~11~~	~~G2 WITH SSC SUPPORTED bit~~	~~yes~~
~~12~~	~~G3 WITHOUT SSC SUPPORTED bit~~	~~yes~~
~~13~~	~~G3 WITH SSC SUPPORTED bit~~	~~yes~~
~~14 to 30~~	~~Reserved~~	~~no~~
~~Trailer~~		
~~31 (last bit)~~	~~PARITY bit~~	~~no~~

~~[a] In the "Changeable" column, phys controlled by a management device server with the SMP PHY CONTROL function (see 10.4.3.24) may set bits labeled "yes" to one in the SNW-3 PHY CAPABILITIES CHANGEABLE field and shall set bits labeled "no" to zero.~~

Table 85 defines the SNW-3 phy capabilities. For each bit defined as reserved, the phy shall transmit a zero (i.e., D.C. idle) and shall ignore the received value. Byte 0 shall be transmitted first and byte 3 shall be

transmitted last. Within each byte, bit 7 shall be transmitted first and bit 0 shall be transmitted last (e.g., overall, the START bit is transmitted first and the PARITY bit is transmitted last).

Table 85 — SNW-3 phy capabilities

Byte\Bit	7	6	5	4	3	2	1	0
0	START (1b)	TX SSC TYPE	Reserved		REQUESTED LOGICAL LINK RATE			
1	SUPPORTED SETTINGS						Reserved	
	G1 WITHOUT SSC	G1 WITH SSC	G2 WITHOUT SSC	G2 WITH SSC	G3 WITHOUT SSC	G3 WITH SSC		
2	Reserved							
3	Reserved							PARITY

The START bit shall be set to one. The phy's receiver shall use this bit to establish the timing for the subsequent bits.

A TX SSC TYPE bit set to one indicates that the phy's transmitter uses center-spreading SSC when SSC is enabled (e.g., the phy is an expander phy that supports attachment to SATA devices)(see 5.3.8). A TX SSC TYPE bit set to zero indicates that the phy's transmitter uses down-spreading SSC when SSC is enabled (e.g., the phy is a SAS phy), or that the phy does not support SSC.

NOTE 2 - The phy receiver may use the TX SSC TYPE bit to optimize its CDR circuitry. ~~This bit indicates the type of SSC used when attached to a SAS phy or an expander phy.~~

The REQUESTED LOGICAL LINK RATE field indicates if the phy supports multiplexing (see 6.10) and, if so, the logical link rate that the phy is requesting. If the phy is managed by an SMP target port, the field is based on the REQUESTED LOGICAL LINK RATE field in the SMP PHY CONTROL ~~and DISCOVER~~ function~~s~~(see 10.4.3.18). ~~This field is independent of the supported settings bits (e.g., G3, G2, and G1 with or without SSC).~~

Table 86 defines the requested logical link rate based on the transmitted and received REQUESTED LOGICAL LINK RATE fields.

Table 86 — Requested logical link rate

Transmitted REQUESTED LOGICAL LINK RATE field	Received REQUESTED LOGICAL LINK RATE field	Requested logical link rate
0h (i.e., no multiplexing)	Any	Negotiated physical link rate
8h (i.e., 1,5 Gbps) [a]	8h (i.e., 1,5 Gbps)	1,5 Gbps
	9h (i.e., 3 Gbps)	
	Ah (i.e., 6 Gbps)	
	Bh - Fh (i.e., future rates)	
9h (i.e., 3 Gbps) [a]	8h (i.e., 1,5 Gbps)	1,5 Gbps
	9h (i.e., 3 Gbps)	3 Gbps
	Ah (i.e., 6 Gbps)	
	Bh - Fh (i.e., future rates)	
Ah (i.e., 6 Gbps) [a]	8h (i.e., 1,5 Gbps)	1,5 Gbps
	9h (i.e., 3 Gbps)	3 Gbps
	Ah (i.e., 6 Gbps)	6 Gbps
	Bh - Fh (i.e., future rates)	

[a] ~~A phy that transmits a value other than 0h allows multiplexing to be enabled.~~

Table 87 defines whether or not multiplexing is enabled and defines the negotiated logical link rate based on the requested logical link rate (see table 86) and the negotiated physical link rate (see 6.7.4.2.4).

Table 87 — Multiplexing negotiation

Requested logical link rate (see table 86)	Negotiated physical link rate	Multiplexing	Negotiated logical link rate
1,5 Gbps	1,5 Gbps	Disabled	1,5 Gbps
	3 Gbps	Enabled	1,5 Gbps
	6 Gbps		3 Gbps
3 Gbps	1,5 Gbps	Disabled	1,5 Gbps
	3 Gbps		3 Gbps
	6 Gbps	Enabled	3 Gbps
6 Gbps	1,5 Gbps	Disabled	1,5 Gbps
	3 Gbps		3 Gbps
	6 Gbps		6 Gbps
Negotiated physical link rate	1,5 Gbps	Disabled	1,5 Gbps
	3 Gbps		3 Gbps
	6 Gbps		6 Gbps

The SUPPORTED SETTINGS bits include the G1 WITHOUT SSC bit, the G1 WITH SSC bit, the G2 WITHOUT SSC bit, the G2 WITH SSC bit, the G3 WITHOUT SSC bit, and the G3 WITH SSC bit.

A G1 WITHOUT SSC ~~SUPPORTED~~ bit set to one indicates that the phy supports G1 (i.e., 1,5 Gbps) without SSC. A G1 WITHOUT SSC ~~SUPPORTED~~ bit set to zero indicates that the phy does not support G1 without SSC. If the phy supports SNW-1 and supports SNW-3, then the G1 WITHOUT SSC ~~SUPPORTED~~ bit shall be set to one.

A G1 WITH SSC ~~SUPPORTED~~ bit set to one indicates that the phy supports G1 (i.e., 1,5 Gbps) with SSC. A G1 WITH SSC ~~SUPPORTED~~ bit set to zero indicates that the phy does not support G1 with SSC.

A G2 WITHOUT SSC ~~SUPPORTED~~ bit set to one indicates that the phy supports G2 (i.e., 3 Gbps) without SSC. A G2 WITHOUT SSC ~~SUPPORTED~~ bit set to zero indicates that the phy does not support G2 without SSC. If the phy supports SNW-2 and supports SNW-3, then the G2 WITHOUT SSC ~~SUPPORTED~~ bit shall be set to one.

A G2 WITH SSC ~~SUPPORTED~~ bit set to one indicates that the phy supports G2 (i.e., 3 Gbps) with SSC. A G2 WITH SSC ~~SUPPORTED~~ bit set to zero indicates that the phy does not support G2 with SSC.

A G3 WITHOUT SSC ~~SUPPORTED~~ bit set to one indicates that the phy supports G3 (i.e., 6 Gbps) without SSC. A G3 G3 WITHOUT SSC ~~SUPPORTED~~ bit set to zero indicates that the phy does not support G3 without SSC.

A G3 WITH SSC ~~SUPPORTED~~ bit set to one indicates that the phy supports G3 (i.e., 6 Gbps) with SSC. A G3 WITH SSC ~~SUPPORTED~~ bit set to zero indicates that the phy does not support G3 with SSC.

Table 88 defines the priority of the SUPPORTED SETTINGS bits.

Table 88 — SUPPORTED SETTINGS bit priorities

Priority	Bit
Highest	G3 WITH SSC bit
...	G3 WITHOUT SSC bit
...	G2 WITH SSC bit
...	G2 WITHOUT SSC bit
...	G1 WITH SSC bit
Lowest	G1 WITHOUT SSC bit

If none of the transmitted SUPPORTED SETTINGS bits are equal to their corresponding received SUPPORTED SETTINGS bits, then the phy shall consider a phy reset problem (see 6.7.4.2.4) to have occurred.

The PARITY bit provides for error detection of the SNW-3 phy capabilities. The PARITY bit shall be set to one or zero such that the total number of SNW-3 phy capabilities bits that are set to one is even, including the START bit and the PARITY bit. If the PARITY bit received is incorrect based upon the received SNW-3 phy capabilities bits, then the parity is bad and the phy shall consider ~~it~~ a phy reset problem (see 6.7.4.2.4) to have occurred.

Table 89 lists some example SNW-3 phy capabilities values.

Table 89 — Example SNW-3 phy capabilities values

Code [a]	Description
80540000h	Down-spreading SSC G1, G2, and G3 with SSC supported
80FC0001h	Down-spreading SSC G1, G2, and G3 with and without SSC supported
80A80000h	G1, G2, and G3 without SSC supported
C0FC0000h	Center-spreading SSC G1, G2, and G3 with and without SSC supported
C9FC0000h	Center-spreading SSC Requested 3 Gbps logical link rate G1, G2, and G3 with and without SSC supported
C8F00001h	Center-spreading SSC Requested 1,5 Gbps logical link rate G1 and G2 with and without SSC supported

[a] Expressed as a 32-bit value with byte 0 bit 7 (i.e., the START bit) as the MSB and byte 3 bit 0 as the LSB (i.e., the PARITY bit).

6.7.4.2.3.4 Train-SNW

Figure 129 defines the Train-SNW, including:

a) maximum Train-SNW window time (MTT);
b) rate change delay time (RCDT);
c) maximum train time (MTT);
d) train lock time (TLT); and

e) actual training time (ATT).

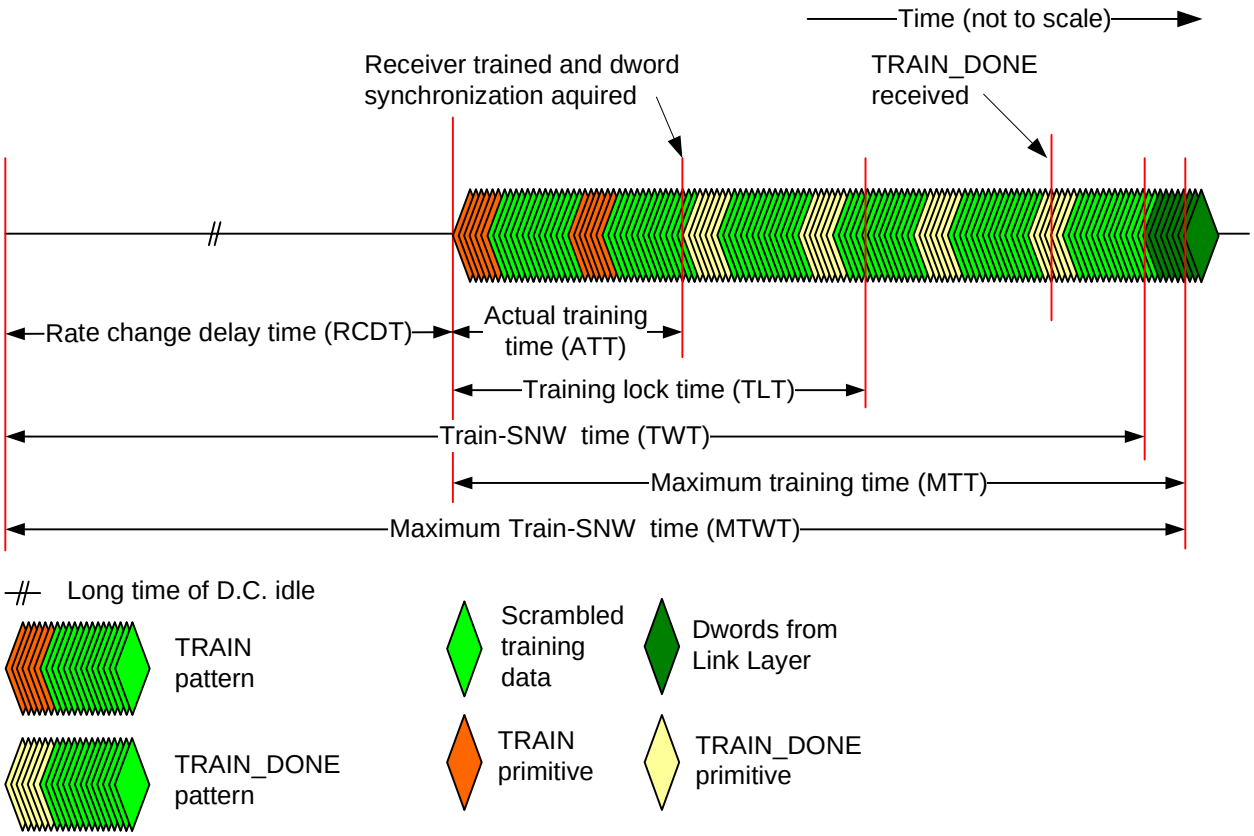

Figure 129 — Train-SNW [updated]

The Train-SNW utilizes TRAIN and TRAIN_DONE (see 7.2) to create training patterns, defined in table 90.

~~There are two training patterns:~~

~~a) the TRAIN pattern; and~~
~~b) the TRAIN_DONE pattern.~~

~~The TRAIN pattern consists of:~~

~~1) TRAIN; and~~
~~2) 58 dwords set to 00000000h that are transmitted scrambled and 8b10b encoded.~~

~~The TRAIN_DONE pattern consists of:~~

~~1) TRAIN_DONE; and~~
~~2) 58 dwords set to 00000000h that are transmitted scrambled and 8b10b encoded.~~

Table 90 — Training patterns

Training pattern	Description
TRAIN pattern	Sequence of: 1) TRAIN primitive sequence; and 2) 58 dwords set to 00000000h that are transmitted scrambled and 8b10b encoded.
TRAIN_DONE pattern	Sequence of: 1) TRAIN_DONE primitive sequence; and 2) 58 dwords set to 00000000h that are transmitted scrambled and 8b10b encoded.

The scrambler is the same as that defined for the link layer (see 7.6) and shall be initialized at the end of RCDT ~~within the Train-SNW~~. The scrambler shall not be re-initialized for the remainder of the Train-SNW.

The phy shall start transmitting TRAIN patterns at the end of RCDT. The first TRAIN pattern may have either starting disparity. The number of TRAIN patterns transmitted is determined by the time required for the phy's receiver to complete training and acquire dword synchronization. The phy shall transmit at least one TRAIN pattern.

If the phy's receiver is trained and acquires dword synchronization before TLT, then the phy shall stop transmitting TRAIN patterns and start transmitting TRAIN_DONE patterns. The phy shall transmit a minimum of four TRAIN_DONE patterns.

If the phy:

a) transmits four or more TRAIN_DONE patterns; and
b) receives a minimum of one TRAIN_DONE before MTT,

then the phy shall:

a) stop transmitting TRAIN_DONE patterns;
b) start transmitting dwords from the link layer; and
c) consider the Train-SNW ~~as~~to be valid.

If the phy does not receive TRAIN_DONE before MTT and transmit four or more TRAIN_DONE patterns, then it shall consider the Train-SNW to be invalid.

6.7.4.2.4 SAS speed negotiation sequence

~~The SAS speed negotiation sequence consists of a set of speed negotiation windows (see 6.7.4.2.3) in the following order:~~

~~1) SNW-1 (i.e., 1,5 Gbps without training);~~
~~2) SNW-2 (i.e., 3 Gbps without training);~~
~~3) if SNW-1 is valid and SNW-2 is invalid, Final-SNW negotiating 1,5 Gbps;~~
~~4) if SNW-1 is invalid, or SNW-1 is valid and SNW-2 is valid, SNW-3;~~
~~5) Either:~~
~~A) if SNW-2 is valid and SNW-3 is invalid, Final-SNW negotiating 3,0 Gbps; or~~
~~B) if SNW-3 is valid, the parity is good, and at least one supported settings bit (see 6.7.4.2.3.3) is common, one or more Train-SNWs.~~

~~The SAS speed negotiation sequence ends after Final-SNW or Train-SNW.~~

The SAS speed negotiation sequence consists of a set of speed negotiation windows (see 6.7.4.2.3) in the order shown in figure 130.

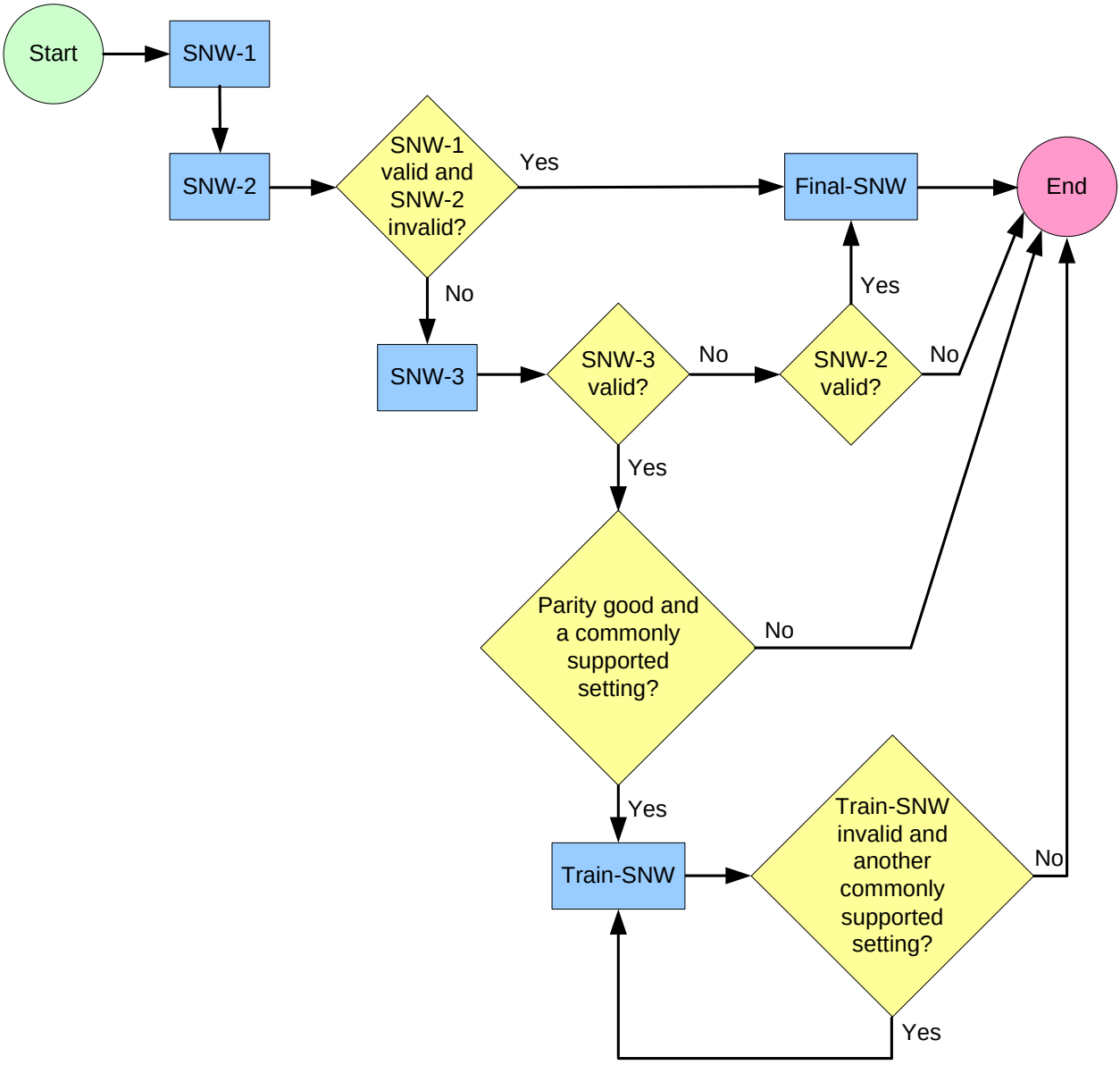

Figure 130 — SAS speed negotiation sequence SNW flowchart

~~If a phy participates in a valid SNW-3 and parity is good, then the phy shall participate in a~~ Train-SNW ~~utilizing~~ is based on the highest untried commonly supported settings based on the outgoing and incoming SNW-3 supported settings bits (see 6.7.4.2.3).

If a Train-SNW is invalid and there are additional, untried, commonly supported settings exchanged during SNW-3, then a new Train-SNW shall be performed ~~at~~based on the next highest, untried, commonly supported ~~capability~~settings.

A phy reset problem occurs if:

a) after SNW-3, if SNW-1, SNW-2, and SNW-3 are all invalid;
b) after Final-SNW, if ~~a~~ Final-SNW is performed and is invalid;
c) after SNW-3, if SNW-3 is valid ~~supported settings are exchanged during SNW-3 and~~ and:
   A) the parity is bad; or
   B) there are no commonly supported settings;

or

d) after a Train-SNW, if the Train-SNW ~~is performed and~~ is invalid and there are no additional, untried, commonly supported settings ~~exchanged during SNW-3~~.

Phy reset problems terminate the SAS speed negotiation sequence and are counted and reported in the PHY RESET PROBLEM COUNT field in the SMP REPORT PHY ERROR LOG page (see 10.4.3.9) and the Protocol-Specific Port log page (see 10.2.8.1).

Figure 131 shows speed negotiation between a phy A and phy B where phys participate in:

1) SNW-1, supported by phy A but not by phy B;
2) SNW-2, supported by both phys;
3) SNW-3, supported by phy A but not by phy B; and
4) Final-SNW negotiating 3 Gbps.

Phy A and phy B detect:

a) SNW-1 invalid;
b) SNW-2 valid; and
c) SNW-3 invalid,

and proceed to Final-SNW negotiating 3 Gbps.

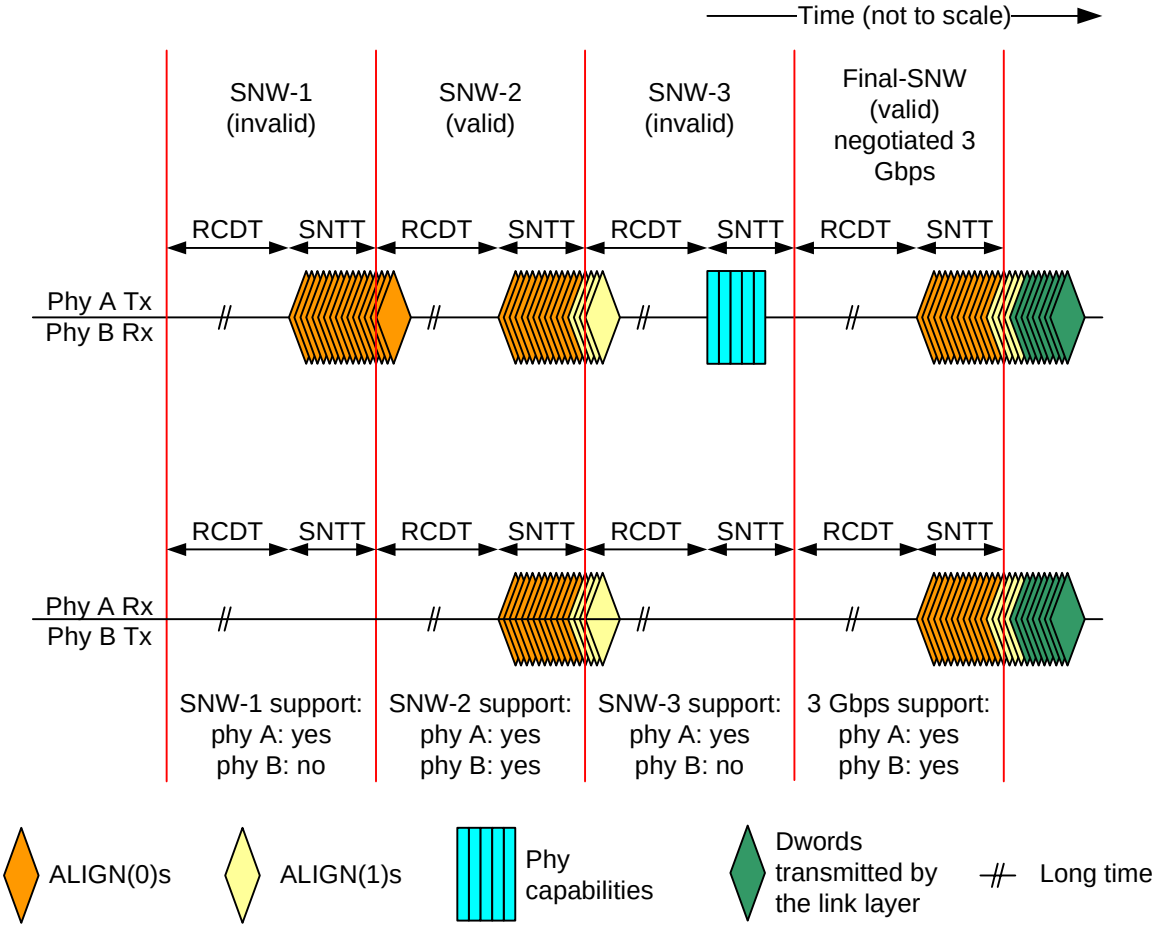

Figure 131 — SAS speed negotiation sequence (phy A: SNW-1 through SNW-3, phy B: SNW-2 only) [modified]

Figure 132 shows speed negotiation between a phy A and a phy B where both phys participate in:

1) SNW-1, supported by both phys;
2) SNW-2, supported by both phys;

3) SNW-3, supported by both phys; and
4) Train-SNW.

Phy A and phy B detect:

a) SNW-1 valid;
b) SNW-2 valid; and
c) SNW-3 valid,

and proceed to Train-SNW negotiating based on SNW-3 phy capabilities bits.

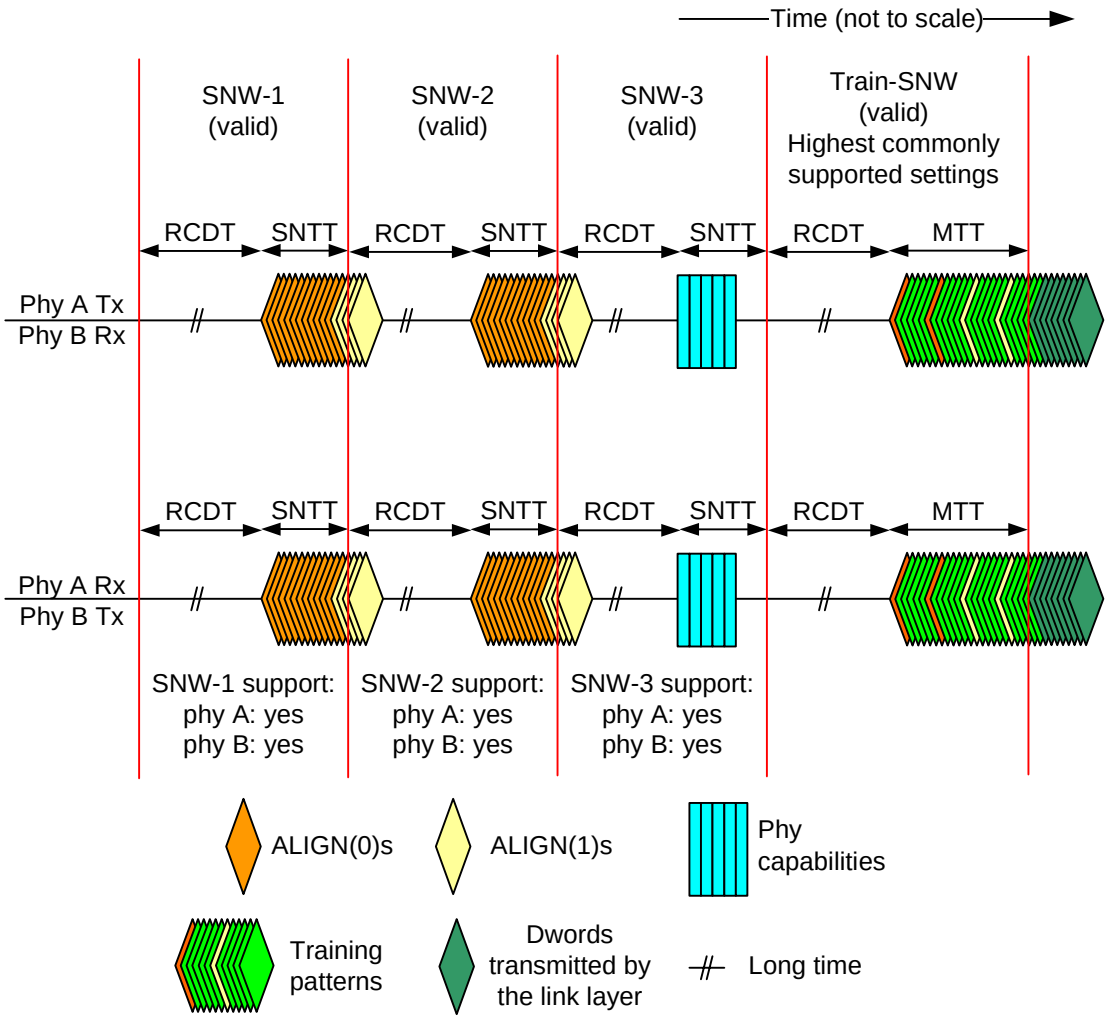

Figure 132 — SAS speed negotiation sequence (both phys SNW-1 through SNW-3) [modified]

Figure 133 shows a speed negotiation sequence where phy B does not achieve dword synchronization during Final-SNW, creating a phy reset problem. If this occurs, the handshake is not complete and the phy reset sequence is retried.

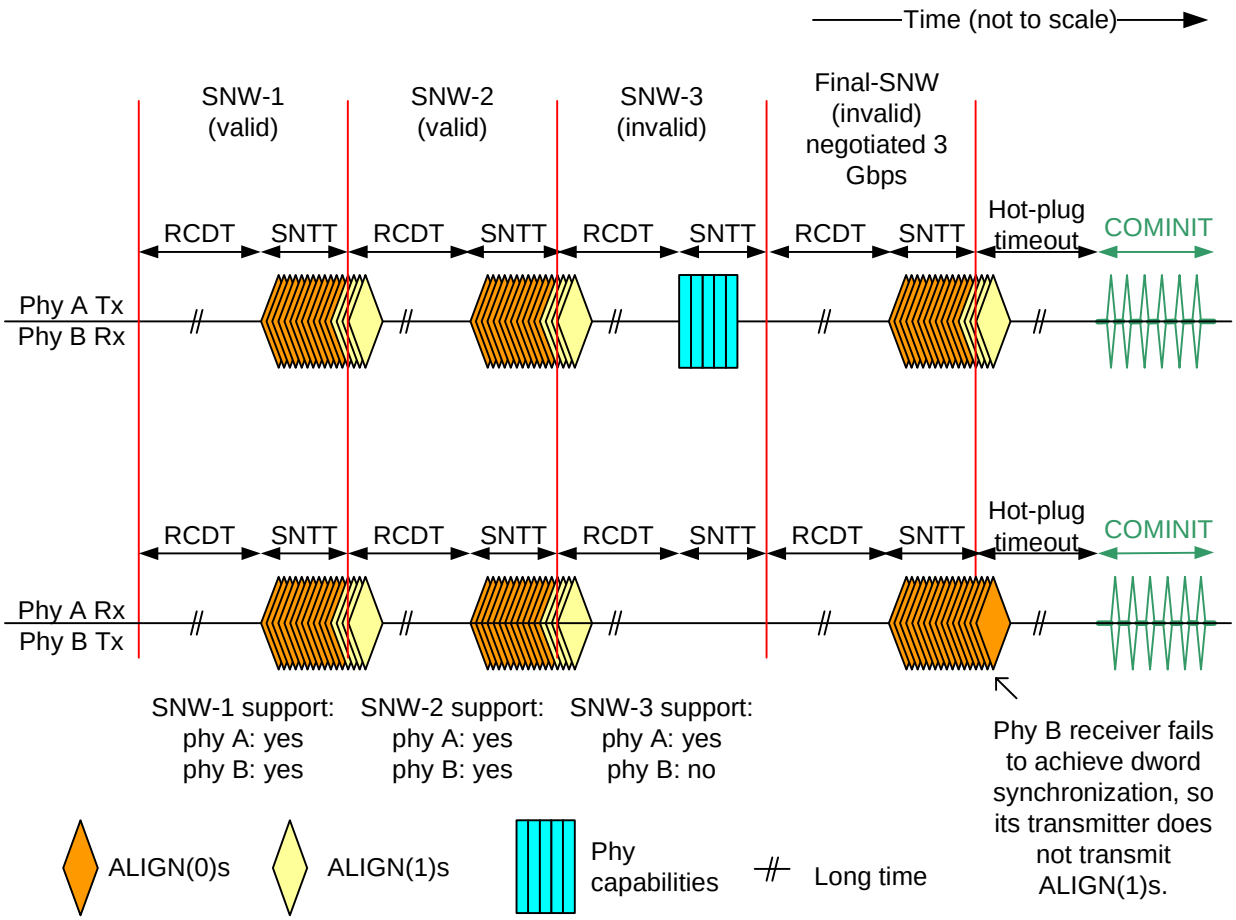

Figure 133 — SAS speed negotiation sequence - phy reset problem in Final-SNW [modified]

Figure 134 shows a speed negotiation sequence in which a phy reset problem is encountered in SNW-3 because the phys do not exchange the phy capabilities bits properly (e.g., due to a parity error).

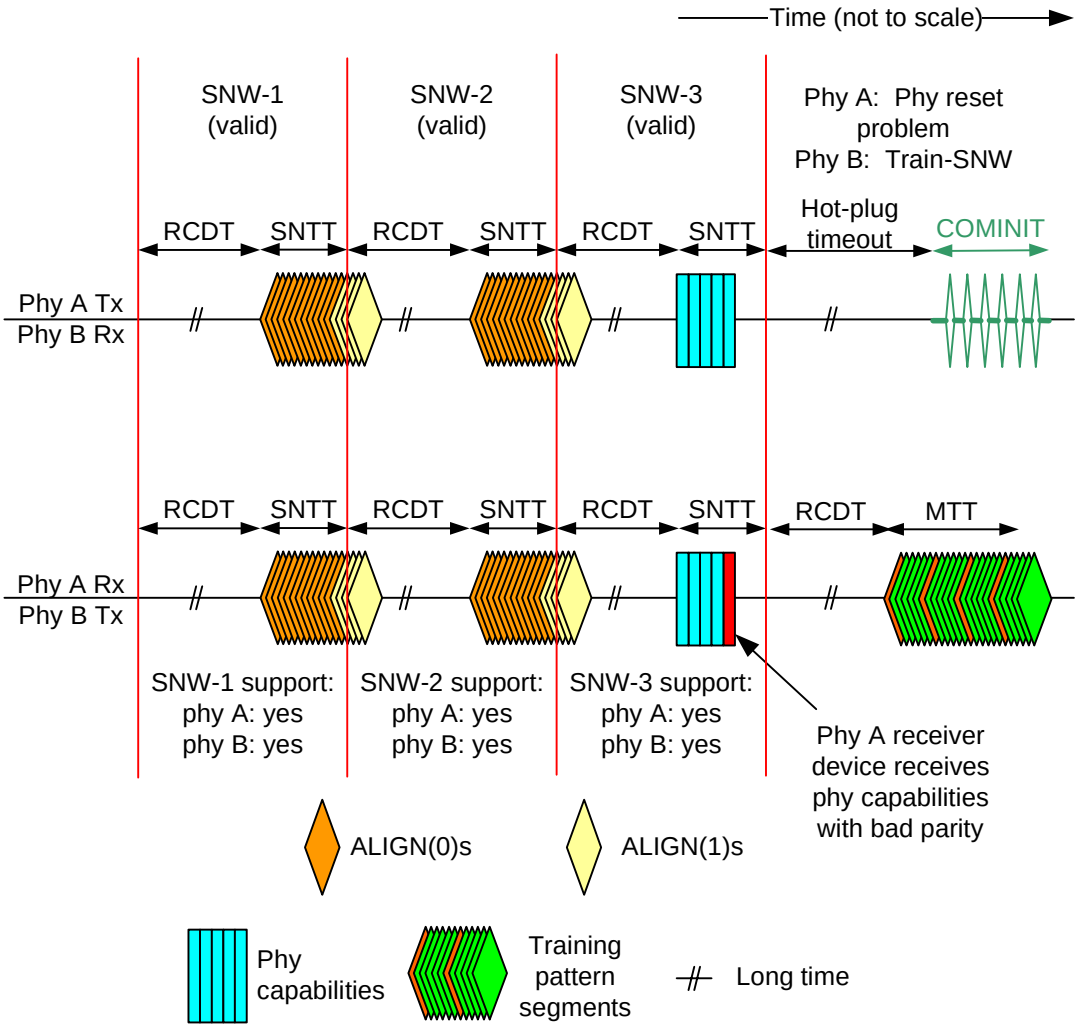

Figure 134 — SAS speed negotiation sequence - phy reset problem in SNW-3 [modified]

Figure 135 shows a speed negotiation sequence in which a phy reset problem is encountered in Train-SNW because either phy does not complete training within the MTT interval of several training windows exhausting all commonly supported settings exchanged in SNW-3.

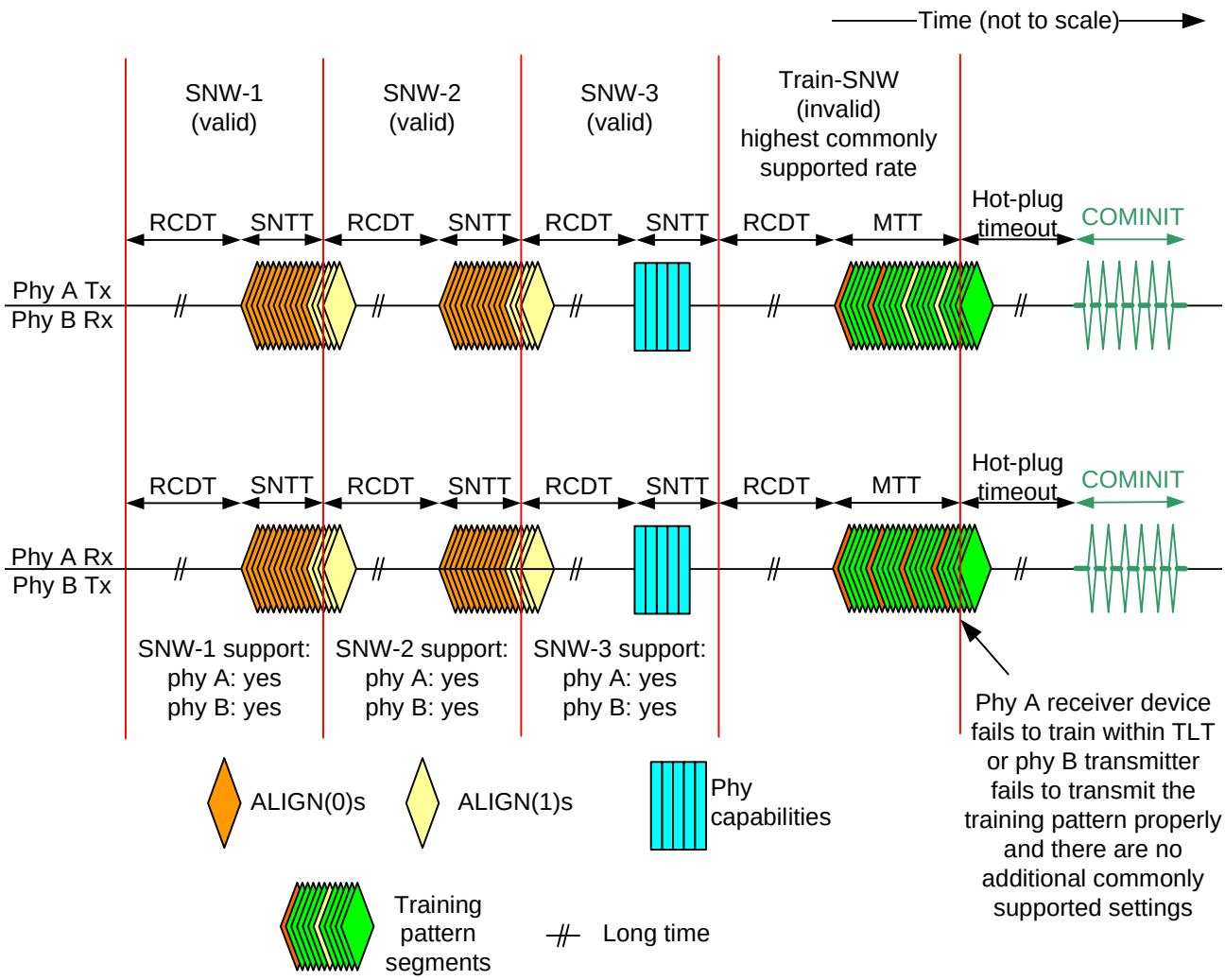

Figure 135 — SAS speed negotiation sequence - phy reset problem in Train-SNW [modified]

Figure 136 shows two Train-SNWs, if supported settings bits are exchanged that contain more than one commonly supported setting and the Train-SNW using the highest commonly supported setting is invalid, a second Train-SNW is performed using the next highest commonly supported setting.

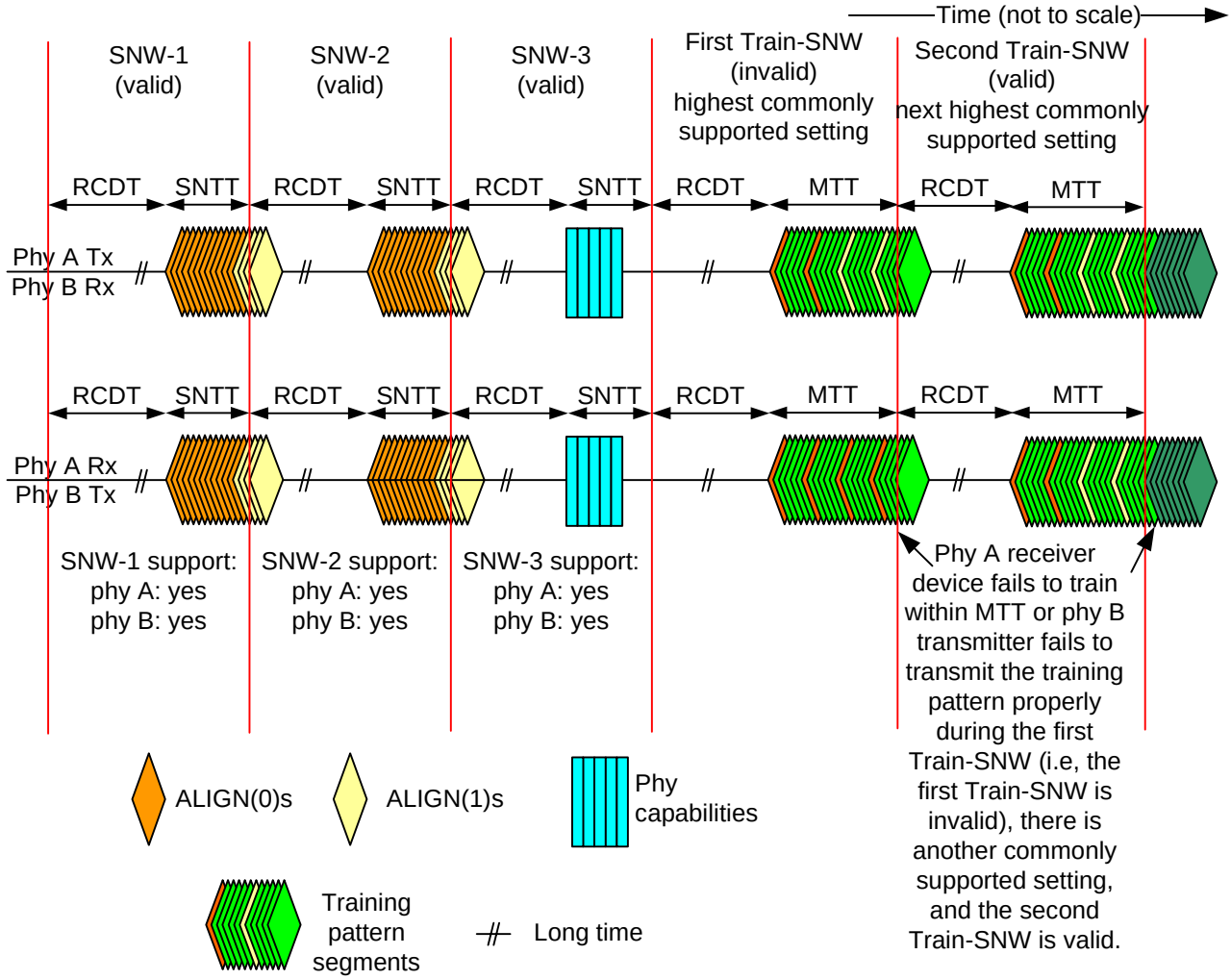

Figure 136 — SAS speed negotiation sequence - multiple Train-SNWs [modified]

For more examples of speed negotiations ~~between phys that support various speeds~~, see Annex C.

10.4.3.5 DISCOVER function

The DISCOVER function returns information about the specified phy. This SMP function provides information from the IDENTIFY address frame received by the phy and additional phy-specific information. This SMP function shall be implemented by all management device servers.

NOTE 3 - The DISCOVER LIST function (see 10.4.3.12) returns information about one or more phys.

...

Table 236 defines the response format.

Table 236 — DISCOVER response (part 1 of 3)

Byte\Bit	7	6	5	4	3	2	1	0
0	SMP FRAME TYPE (41h)							
1	FUNCTION (10h)							
2	FUNCTION RESULT							
3	RESPONSE LENGTH (17h)							
4	(MSB) EXPANDER CHANGE COUNT							
5	EXPANDER CHANGE COUNT							(LSB)
6	Reserved							
8	Reserved							
9	PHY IDENTIFIER							
10	Reserved							
11	Reserved							
12	Reserved	ATTACHED DEVICE TYPE			Reserved			
13	Reserved				NEGOTIATED LOGICAL LINK RATE			
14	Reserved				ATTACHED SSP INITIATOR	ATTACHED STP INITIATOR	ATTACHED SMP INITIATOR	ATTACHED SATA HOST
15	ATTACHED SATA PORT SELECTOR	Reserved			ATTACHED SSP TARGET	ATTACHED STP TARGET	ATTACHED SMP TARGET	ATTACHED SATA DEVICE
16	SAS ADDRESS							
23	SAS ADDRESS							
24	ATTACHED SAS ADDRESS							
31	ATTACHED SAS ADDRESS							
32	ATTACHED PHY IDENTIFIER							
33	Reserved					ATTACHED INSIDE ZPSDS PERSISTENT	ATTACHED REQUESTED INSIDE ZPSDS	ATTACHED BREAK_REPLY CAPABLE
34	Reserved							
39	Reserved							
40	PROGRAMMED MINIMUM PHYSICAL LINK RATE				HARDWARE MINIMUM PHYSICAL LINK RATE			
41	PROGRAMMED MAXIMUM PHYSICAL LINK RATE				HARDWARE MAXIMUM PHYSICAL LINK RATE			
42	PHY CHANGE COUNT							
43	VIRTUAL PHY	Reserved			PARTIAL PATHWAY TIMEOUT VALUE			
44	Reserved				ROUTING ATTRIBUTE			
45	Reserved	CONNECTOR TYPE						

Table 236 — DISCOVER response (part 2 of 3)

Byte\Bit	7	6	5	4	3	2	1	0
46	CONNECTOR ELEMENT INDEX							
47	CONNECTOR PHYSICAL LINK							
48	Reserved							
49								
50	Vendor specific							
51								
52	ATTACHED DEVICE NAME							
59								
60	Reserved	REQUESTED INSIDE ZPSDS CHANGED BY EXPANDER	INSIDE ZPSDS PERSISTENT	REQUESTED INSIDE ZPSDS	ZONE ADDRESS RESOLVED	ZONE GROUP PERSISTENT	INSIDE ZPSDS	ZONING ENABLED
61	Reserved							
62								
63	ZONE GROUP							
64	SELF-CONFIGURATION STATUS							
65	SELF-CONFIGURATION LEVELS COMPLETED							
66	Reserved							
67								
68	SELF-CONFIGURATION SAS ADDRESS							
75								
~~76~~	~~Reserved~~							
~~91~~								
76	PROGRAMMED PHY CAPABILITIES							
79								
80	CURRENT PHY CAPABILITIES							
83								
84	ATTACHED PHY CAPABILITIES							
87								
88	Reserved							
91								

Table 236 — DISCOVER response (part 3 of 3)

Byte\Bit	7	6	5	4	3	2	1	0
92	Reserved							
93								
94	Reserved			~~Reserved~~ NEGOTIATED SSC	NEGOTIATED PHYSICAL LINK RATE			
95	Reserved							HARDWARE MUXING SUPPORTED
96	(MSB)	CRC						
99								(LSB)

The SMP FRAME TYPE field shall be set to 41h.

The FUNCTION field shall be set to 10h.

The FUNCTION RESULT field is defined in 10.4.3.2.

The RESPONSE LENGTH field shall be set to 17h. For compatibility with previous versions of this standard, a RESPONSE LENGTH field set to 00h indicates that there are 12 dwords before the CRC field.

...

The SELF-CONFIGURATION SAS ADDRESS field indicates the SAS address of the SMP target port to which the self-configuring expander device established a connection or attempted to establish a connection using the specified phy and resulted in the status indicated by the SELF-CONFIGURATION STATUS field.

The PROGRAMMED PHY CAPABILITIES field indicates the SNW-3 phy capabilities bits that are going to be transmitted in the next link reset sequence containing SNW-3 as defined in table 85 in 6.7.4.2.3.3.

The CURRENT PHY CAPABILITIES field indicates the outgoing SNW-3 phy capabilities bits transmitted in the last link reset sequence as defined in table 85 in 6.7.4.2.3.3. If the last link reset sequence did not include SNW-3 or was a SATA link reset sequence, the CURRENT PHY CAPABILITIES field shall be set to zero.

The ATTACHED PHY CAPABILITIES field indicates the incoming SNW-3 phy capabilities bits received in the last SNW-3 as defined in table 85 in 6.7.4.2.3.3. If the last link reset sequence did not include SNW-3 or was a SATA link reset sequence, the ATTACHED PHY CAPABILITIES field shall be set to zero.

A NEGOTIATED SSC field set to one indicates that SSC is enabled. A NEGOTIATED SSC field set to zero indicates that SSC is disabled. The NEGOTIATED SSC field is only valid when the NEGOTIATED PHYSICAL LINK RATE field is greater than or equal to 8h.

The NEGOTIATED PHYSICAL LINK RATE field is defined in table 237 and indicate the physical link rate negotiated during the link reset sequence or other conditions of the phy. The negotiated physical link rate may be less than the programmed minimum physical link rate or greater than the programmed maximum physical link rate if the programmed physical link rates have been changed since the last link reset sequence.

Table 237 — NEGOTIATED PHYSICAL LINK RATE **field**

SP state machine ResetStatus state machine variable	Code	Description
UNKNOWN	0h	Phy is enabled; unknown physical link rate. [a]
DISABLED	1h	Phy is disabled.
PHY_ RESET_ PROBLEM	2h	Phy is enabled; a phy reset problem occurred (see 6.7.4.2.4).
SPINUP_ HOLD	3h	Phy is enabled; detected a SATA device and entered the SATA spinup hold state. The SMP PHY CONTROL function (see 10.4.3.18) phy operations of LINK RESET and HARD RESET may be used to release the phy.
PORT_ SELECTOR	4h	Phy is enabled; detected a SATA port selector. The physical link rate has not been negotiated since the last time the phy's SP state machine entered the SP0:OOB_COMINIT state. The SATA spinup hold state has not been entered since the last time the phy's SP state machine entered the SP0:OOB_COMINIT state. The value in this field may change to 3h, 8h, 9h, or Ah if attached to the active phy of the SATA port selector. Presence of a SATA port selector is indicated by the ATTACHED SATA PORT SELECTOR bit (see table 247).
RESET_ IN_ PROGRESS	5h	Phy is enabled; the expander phy is performing an SMP PHY CONTROL function (see 10.4.3.18) phy operation of LINK RESET or HARD RESET. This value is returned if the specified phy contained a value of 8h, 9h, or Ah in this field when an SMP PHY CONTROL function phy operation of LINK RESET or HARD RESET phy operation is processed.
UNSUPPORTED_ PHY_ ATTACHED	6h	Phy is enabled; a phy is attached without any commonly supported settings.
Reserved	7h	Reserved
G1	8h	Phy is enabled; 1,5 Gbps physical link rate.
G2	9h	Phy is enabled; 3 Gbps physical link rate.
G3	Ah	Phy is enabled; 6 Gbps physical link rate.
Reserved	Bh - Fh	Phy is enabled; reserved for future logical or physical link rates.

[a] This code may be used by an application client in its local data structures to indicate an unknown negotiated logical or physical link rate (e.g., before the discover process has queried the phy).

A HARDWARE MUXING SUPPORTED bit set to one indicates the phy supports multiplexing (see 6.10). A HARDWARE MUXING SUPPORTED bit set to zero indicates the phy does not support multiplexing. This value is not adjusted based on the negotiated physical link rate.

The CRC field is defined in 10.4.3.2.

10.4.3.18 PHY CONTROL function

The PHY CONTROL function requests actions by the specified phy. This SMP function may be implemented by any management device server. In zoning expander devices, if zoning is enabled then this function shall only be processed from SMP initiator ports that have access to zone group 2 or the zone group of the specified phy (see 4.9.3.2).

Table 289 defines the request format.

Table 289 — PHY CONTROL request

Byte\Bit	7	6	5	4	3	2	1	0
0	SMP FRAME TYPE (40h)							
1	FUNCTION (91h)							
2	Reserved							
3	REQUEST LENGTH (09h)							
4	(MSB)							
5	EXPECTED EXPANDER CHANGE COUNT							(LSB)
6	Reserved							
8								
9	PHY IDENTIFIER							
10	PHY OPERATION							
11	Reserved							UPDATE PARTIAL PATHWAY TIMEOUT VALUE
12	Reserved							
31								
32	PROGRAMMED MINIMUM PHYSICAL LINK RATE				Reserved			
33	PROGRAMMED MAXIMUM PHYSICAL LINK RATE				Reserved			
34	Reserved							
35								
36	Reserved				PARTIAL PATHWAY TIMEOUT VALUE			
37	Reserved							
39								
40	(MSB)							
43	CRC							(LSB)

The SMP FRAME TYPE field shall be set to 40h.

The FUNCTION field shall be set to 91h.

The REQUEST LENGTH field shall be set to 09h. For compatibility with previous versions of this standard, a REQUEST LENGTH field set to 00h specifies that there are 9 dwords before the CRC field.

The EXPECTED EXPANDER CHANGE COUNT field is defined in the SMP CONFIGURE GENERAL request (see 10.4.3.14).

The PHY IDENTIFIER field specifies the phy (see 4.2.7) to which the SMP PHY CONTROL request applies.

...

An UPDATE PARTIAL PATHWAY TIMEOUT VALUE bit set to one specifies that the PARTIAL PATHWAY TIMEOUT VALUE field shall be honored. An UPDATE PARTIAL PATHWAY TIMEOUT VALUE bit set to zero specifies that the PARTIAL PATHWAY TIMEOUT VALUE field shall be ignored.

The PROGRAMMED MINIMUM PHYSICAL LINK RATE field specifies the minimum physical link rate the phy shall support during a link reset sequence (see 4.4.1). Table 290 defines the values for this field. This value is reported in the DISCOVER response (see 10.4.3.5). If this field is changed along with a phy operation of LINK RESET or HARD RESET, that phy operation shall utilize the new value for this field. This value is reported in the DISCOVER response (see 10.4.3.5).

The PROGRAMMED MAXIMUM PHYSICAL LINK RATE field specifies the maximum physical link rates the phy shall support during a link reset sequence (see 4.4.1). Table 290 defines the values for this field. This value is reported in the DISCOVER response (see 10.4.3.5). If this field is changed along with a phy operation of LINK RESET or HARD RESET, that phy operation shall utilize the new value for this field. This value is reported in the DISCOVER response (see 10.4.3.5).

Table 290 — PROGRAMMED MINIMUM PHYSICAL LINK RATE **and** PROGRAMMED MAXIMUM PHYSICAL LINK RATE **fields**

Code	Description
0h	Do not change current value
1h -7h	Reserved
8h	1,5 Gbps
9h	3 Gbps
Ah	6 Gbps
Bh - Fh	Reserved for future physical link rates

If the PROGRAMMED MINIMUM PHYSICAL LINK RATE field or the PROGRAMMED MAXIMUM PHYSICAL LINK RATE field is set to an unsupported or reserved value, or the PROGRAMMED MINIMUM PHYSICAL LINK RATE field and PROGRAMMED MAXIMUM PHYSICAL LINK RATE field are set to an invalid combination of values (e.g., the minimum is greater than the maximum), the management device server shall not change either of their values and may return a function result of SMP FUNCTION FAILED in the response frame. If it returns a function result of SMP FUNCTION FAILED, it shall not perform the requested phy operation.

The PARTIAL PATHWAY TIMEOUT VALUE field specifies the amount of time in microseconds the expander phy shall wait after receiving an Arbitrating (Blocked On Partial) confirmation from the ECM before requesting that the ECM resolve pathway blockage (see 7.12.4.5). A PARTIAL PATHWAY TIMEOUT VALUE field value of zero (i.e., 0 µs) specifies that partial pathway resolution shall be requested by the expander phy immediately upon reception of an Arbitrating (Blocked On Partial) confirmation from the ECM. The PARTIAL PATHWAY TIMEOUT VALUE field is only honored when the UPDATE PARTIAL PATHWAY TIMEOUT VALUE bit is set to one. This value is reported in the DISCOVER response (see 10.4.3.5).

The CRC field is defined in 10.4.3.1.

Table 291 defines the response format.

Table 291 — PHY CONTROL response

Byte\Bit	7	6	5	4	3	2	1	0
0	SMP FRAME TYPE (41h)							
1	FUNCTION (91h)							
2	FUNCTION RESULT							
3	RESPONSE LENGTH (00h)							
4	(MSB)			CRC				
7								(LSB)

The SMP FRAME TYPE field shall be set to 41h.

The FUNCTION field shall be set to 91h.

The FUNCTION RESULT field is defined in 10.4.3.2.

The RESPONSE LENGTH field shall be set to 00h.

The CRC field is defined in 10.4.3.2.

Annex A
(informative)

SAS to SAS phy reset sequence examples

Figure A.1 shows a speed negotiation between a phy A that supports only SNW-1 attached to a phy B that only supports SNW-1. Both phys run:

1) SNW-1, supported by both phys; and
2) SNW-2, supported by neither phy.

Both phys then select 1,5 Gbps for Final-SNW, which is used to establish the negotiated physical link rate.

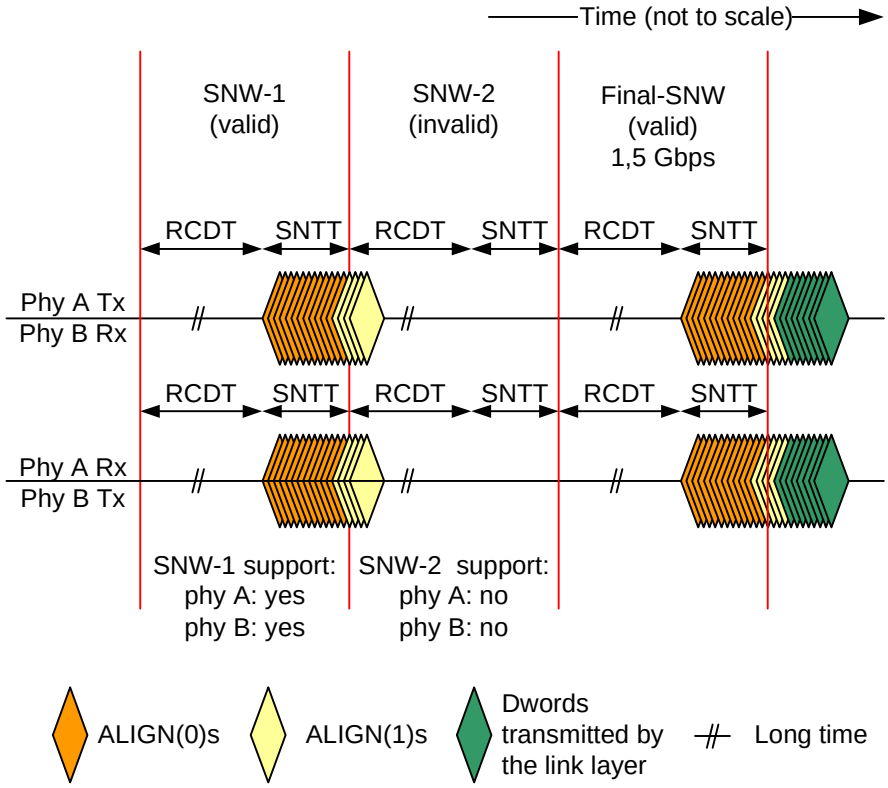

Figure A.1 — SAS speed negotiation sequence (phy A: SNW-1 only, phy B: SNW-1 only) [modified]

Figure A.2 shows a speed negotiation between a phy A that supports SNW-1 and SNW-2 attached to a phy B that supports SNW-1 and SNW-2. Both phys run:

1) SNW-1, supported by both phys;
2) SNW-2, supported by both phys; and
3) SNW-3, supported by neither phy.

Both phys then select 3 Gbps for Final-SNW, which is used to establish the negotiated physical link rate.

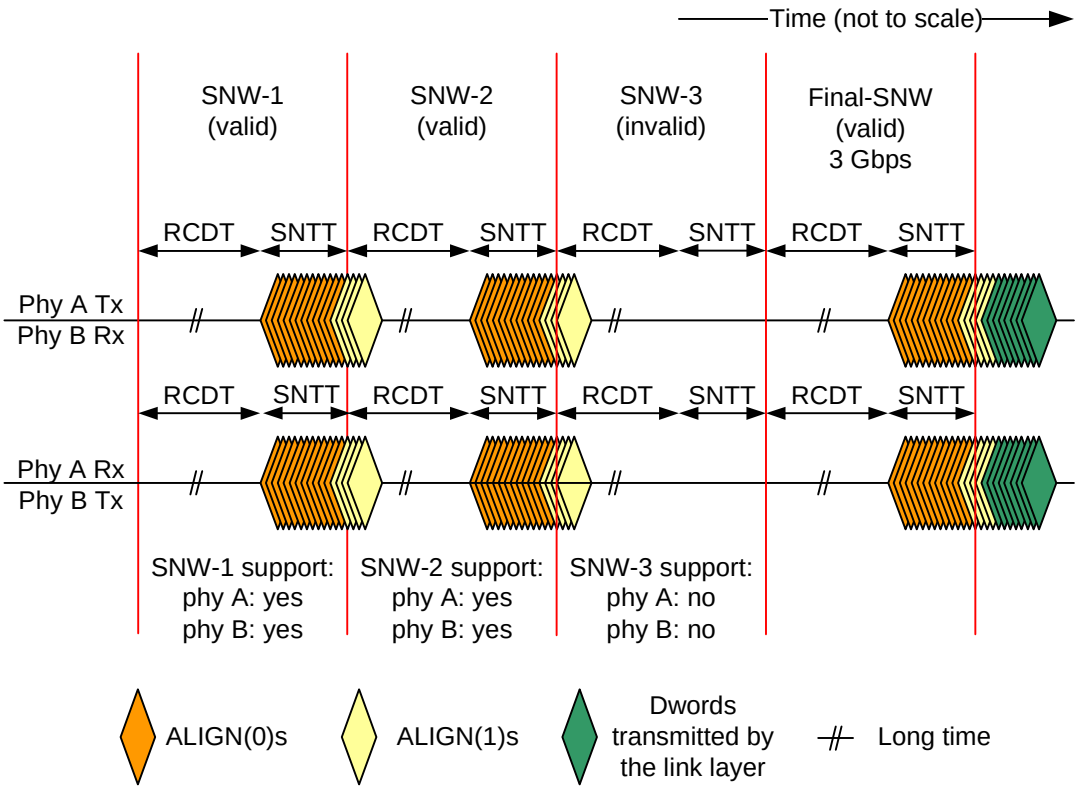

Figure A.2 — SAS speed negotiation sequence (phy A: SNW-1, SNW-2, phy B: SNW-1, SNW-2) [modified]

Figure A.3 shows a speed negotiation between a phy A that supports SNW-1 through SNW-3 attached to a phy B that only supports SNW-1 and SNW-2. Both phys run:

1) SNW-1, supported by both phys;
2) SNW-2, supported by both phys; and
3) SNW-3, supported by phy A but not by phy B.

Both phys then select 3 Gbps for Final-SNW, which is used to establish the negotiated physical link rate.

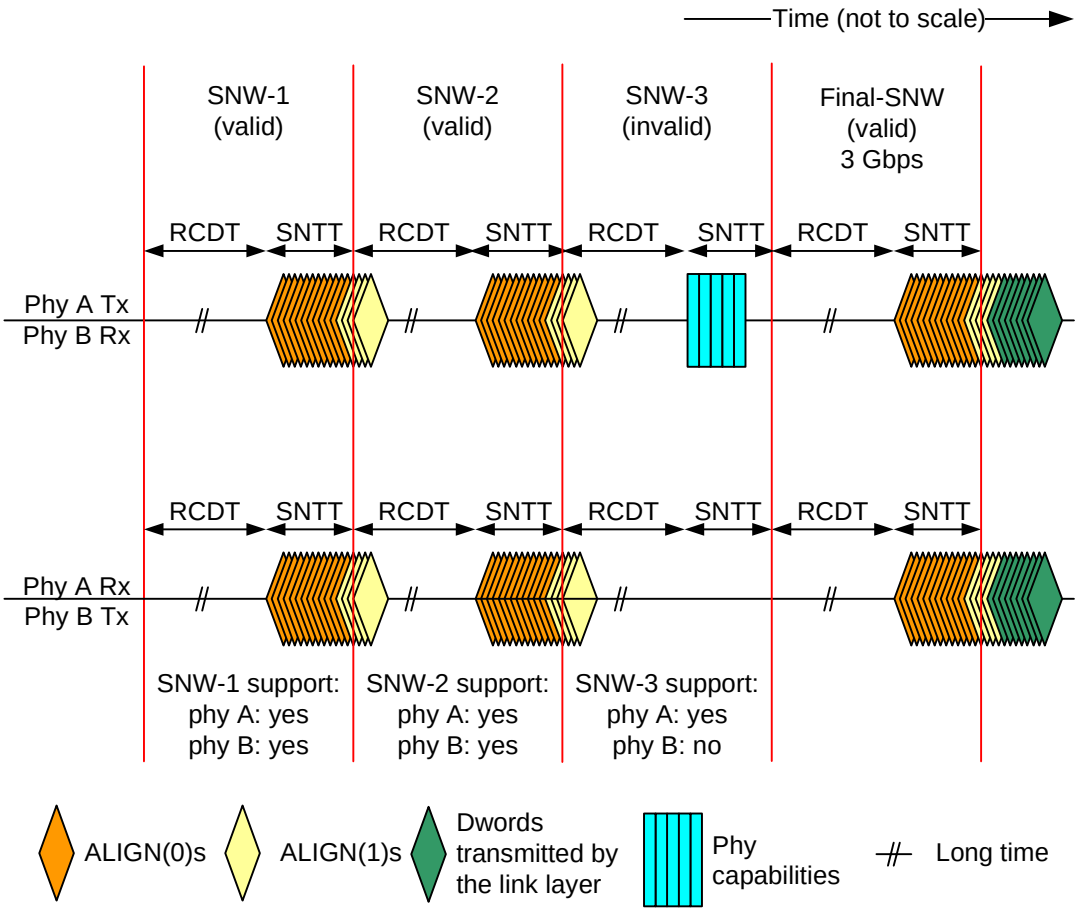

Figure A.3 — SAS speed negotiation sequence (phy A: SNW-1, SNW-2, SNW-3, phy B: SNW-1, SNW-2) [modified]

Figure A.4 shows a speed negotiation between a phy A that supports SNW-2 and SNW-3 attached to a phy B that only supports SNW-1 and SNW-2. Both phys run:

1) SNW-1, supported by phy B but not by phy A;
2) SNW-2, supported by both phys; and
3) SNW-3, supported by phy A but not by phy B.

Both phys then select 3 Gbps for Final-SNW, which is used to establish the negotiated physical link rate.

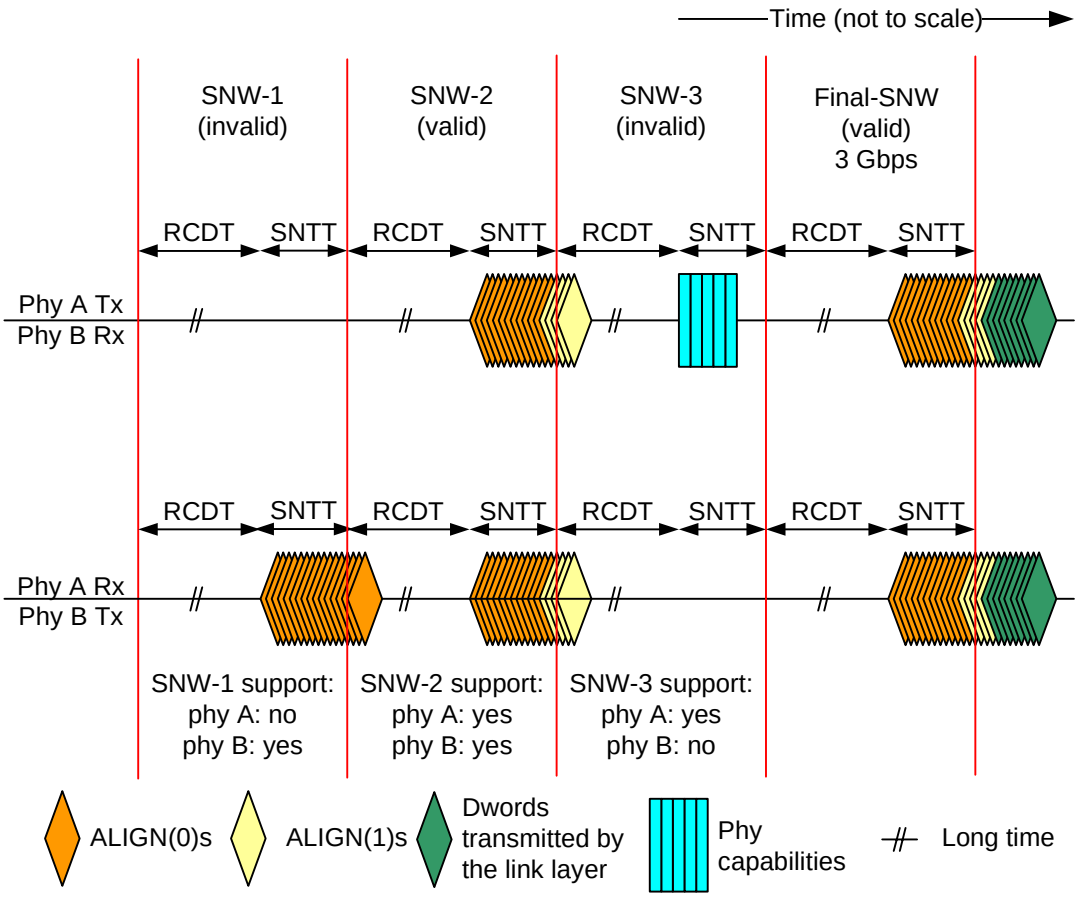

Figure A.4 — SAS speed negotiation sequence (phy A: SNW-2, SNW-3, phy B: SNW-1, SNW-2) [modified]

Figure A.5 shows a speed negotiation between a phy A that only supports SNW-1 attached to a phy B that only supports SNW-2. Both phys run:

1) SNW-1, supported by phy A but not by phy B; and
2) SNW-2, supported by phy B but not by phy A.

Phy B continues to run SNW-3, but phy A determines speed negotiation is unsuccessful and may attempt another phy reset sequence after a hot-plug timeout.

Phy B determines speed negotiation is not succeeding after SNW-3 and may retry the phy reset sequence after a hot-plug timeout.

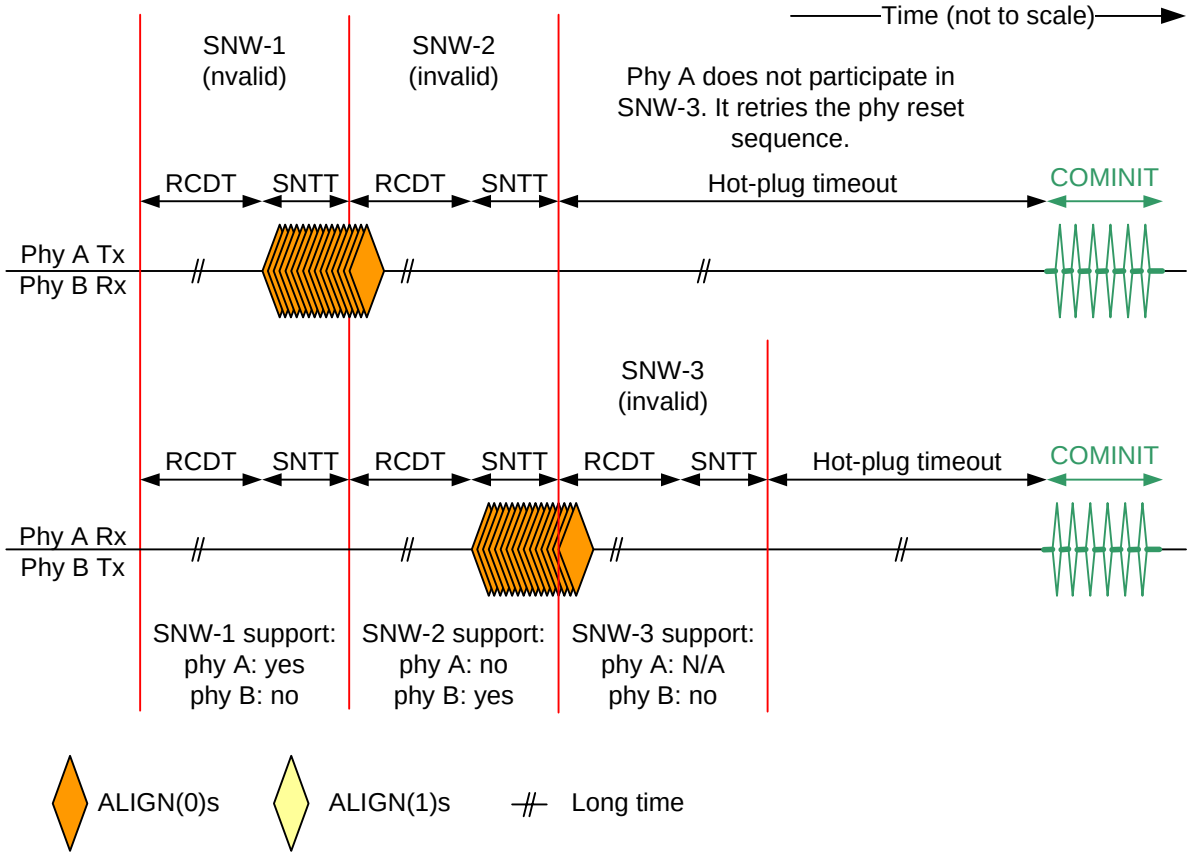

Figure A.5 — SAS speed negotiation sequence (phy A: SNW-1 only, phy B: SNW-2 only) [modified]