SAS-2 6Gbps PHY Specification T10/07-063r0

Date: February 2, 2007
To: T10 Technical Committee
From: Alvin Cox (alvin.cox@seagate.com)
Subject: SAS-2 6Gbps PHY Electrical Specification

Abstract: The attached information defines the electrical requirements for 6 Gbps transmitter devices and receiver device. In addition, updates may include reference transmitter and receiver device definitions to provide a means of determining if a channel is compliant and a cable specification section with requirements for 6Gbps usage. Editor notes are included as reminders for specification development. Revisions will not include redlines.

Revision History:
r0: Initial posting that is very preliminary and nowhere near complete, provided as a starting point and a basis to leverage the final PHY proposal from rather than a PowerPoint format.

Reference proposals:

07-037 SAS-2 Common Mode Generation Specification [Witt, Bari]
07-007 Proposed 6G SAS Phy Specs for EMI Reduction [Jenkins]
07-001 Proposal for 6G SAS Phy Specification [Jenkins]
06-419 SAS-2 Reference Transmitter and Receiver Specification Proposal [Witt]
06-206 SAS-2 Data Eyes vs. De-Emphasis [Witt]
06-053 Roadmap to SAS-2 Physical Layer Specification [Witt]
06-052 Enhanced SFF-8470, SFF-8086 and SATA Cable at 6Gbps [Witt]
06-049 Comparison of Equalization Schemes for 6Gbps SAS Channels [Caroselli]
05-204 Towards a SAS-2 Physical Layer Specification [Witt]
05-426 SAS-2 Cable Reach Objective and Crosstalk [Witt]
05-425 SAS-2 Channel Model Simulations [Witt]
05-342 SAS-2 Adaptive Equalizer Physical Layer Feasibility [Witt]
05-341 Updated Test and Simulation Results in Support of SAS-2 [Witt]
05-203 SAS-2 6Gbps Test Results [Witt]
06-496 SAS-2 Electrical Specification Proposal [Witt]

Transmitter:

Editor notes:

Rob doesn't like "transmitter device" and "receiver device" because "device" has so many meanings. I have left them in place until a viable alternative is proposed.

No maximum transition time is included since this is limited by the pk-pk voltage requirement. The minimum rise time may also be dropped as a result of the Scd22 plot. (The frequency range will probably be increased above 6GHz on this plot.)

Transmitter equalization needs to be informative rather than normative because of emphasis schemes and desire by large OEM's to have custom settings.
Use "transmitter device equalization" instead of "de-emphasis".
A default transmitter equalization value of 3 dB is currently the recommended value. In some extraordinary cases, additional equalization is recommended.

Common mode, return loss, and EMI concerns via s-parameter plots.

Jitter:
All indications are that the present measurement method using a type 1 filter with a corner frequency of fbaud/1667 will not allow measurement with SSC. Probably needs a type 2 filter, but details need to be determined. Seagate will provide an initial description.

General:
Values need some amount of description for measurement methodology similar to what was done in SATA.

Transmitter device	Min	Nominal	Max	Units
Bit Rate		6000		Mbps
Differential Voltage Swing (pk-pk) Vpk	800		1200	mV
Transition Time (20%-80%)	41.667 (0.25)			ps (UI)
Tx Equalization (informative default de-emphasis)	2	3	4	dB
Sdd22 Differential Return Loss			see Plot	dB
Scc22 Common Mode Return Loss			see Plot	dB
Reference Diff Impedance		100		ohm
Reference Common Impedance		25		ohm
Scd22 Differential to Common Mode Conversion			see Plot	dB
Random Jitter			0.15	UI
Deterministic Jitter			0.15	UI
Total Jitter			0.3	UI
AC Coupling Cap (if attaches to SATA)			12	nF

Equalization measurement

The equalization measurement shall be based on two mode measurements. The specified signal pattern has not been agreed upon. Diagnostic 2 DWORD test pattern of D30.3 (Table 215 in SAS 2 rev 8) [4/3/3/4] or possibly CJTPAT could be used. CJTPAT is available from all PHY's so it has this advantage. Text and figures below to be updated based on the pattern chosen, amount of equalization, and final methodology.

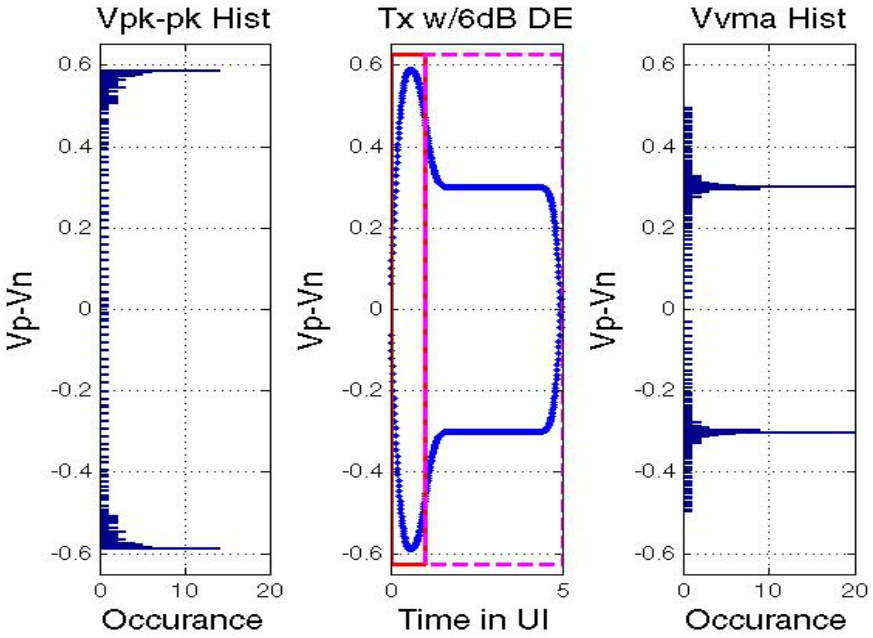
Measured into a Zero Length Test Load.

Left plot:
Sampling or Real-time scope with Histogram Function
Vpk-pk Sample Window is 1UI wide after each transition's zero crossing (first UI of middle plot). It is the first UI section of the middle plot.

Middle plot:
Illustration of a 0000011111 pattern with 6dB of de-emphasis. The total window shown is 5 UI wide.

Right plot:
Vvma Sample Window is 4UI wide 1UI after each transition's zero crossing (0000011111 pattern). It is the 1-5 UI section of the middle plot.

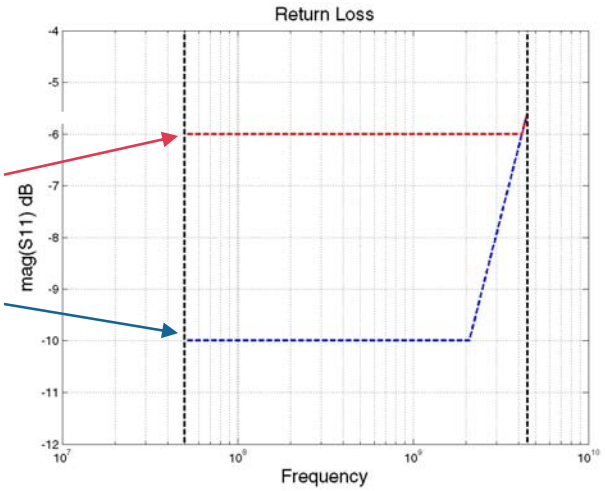
$$DE_{dB} = 20Log_{10}\left(\frac{V_{pk-pk}}{V_{vma}}\right)$$



for $50MHz < f < 6\,GHz$

$$SCC22 = \max\left\{-6, -7.9 + 13.3 * Log_{10}\left(\frac{f}{3.0G}\right)\right\}$$

$$SDD22 = \max\left\{-10, -7.9 + 13.3 * Log_{10}\left(\frac{f}{3.0G}\right)\right\}$$

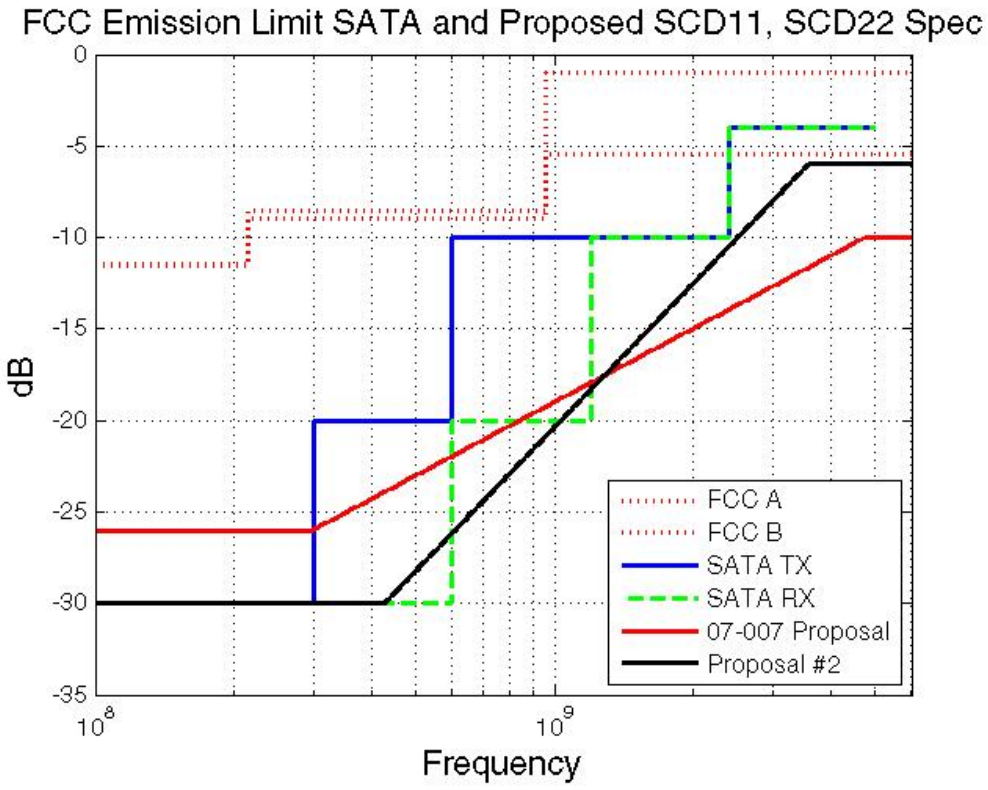


for $100MHz < f < 6GHz$

$$SCD11 < \max\left\{L, \min\left\{H, N + S * Log_{10}\left(\frac{f}{3.0G}\right)\right\}\right\}$$

$07-007\text{r}0 \quad L = -26,\ H = -10,\ N = -12.7,\ S = 13.3$

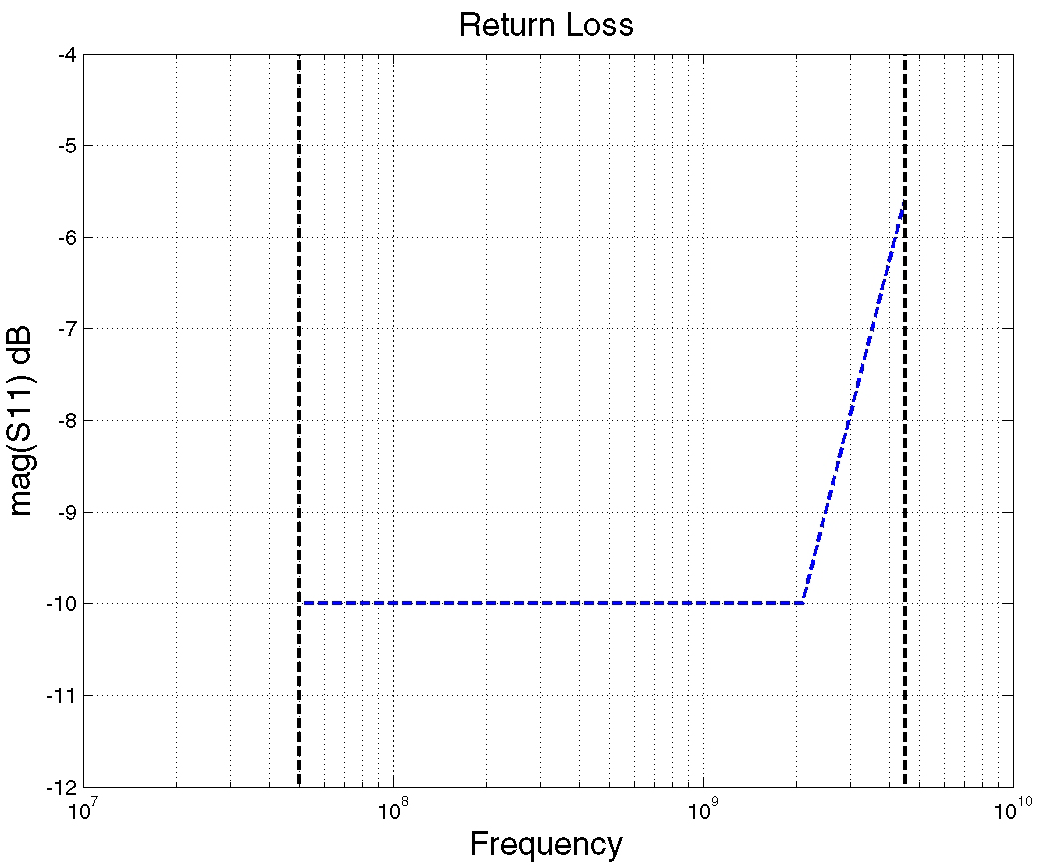
$\text{Proposal \#2} \quad L = -30,\ H = -6,\ N = -8,\ S = 26$



Receiver:

Editor's note:
There are some factors at the far end that will complicate the receiver jitter tolerance specification. Since the receiver is expected to have an equalization function, a mathematical equalization equation will probably be needed to process the received signal at the compliance point to determine the resulting jitter is proper for testing the receiver device.

Receiver	Min	Nominal	Max	Units
Sdd22 Differential Return Loss			See Plot	dB
Scc22 Common Mode Return Loss			See Plot	dB
Reference Diff Impedance		100		ohm
Reference Common Mode Impedance		50		ohm
Common Mode Tolerance (2-200MHz)	150			mV
Max Operational Input Voltage @ 6,0 GBps	1200			mV
Max Operational Input Voltage @ 1,5 and 3,0 GBps	1600			mV
Max Non-Operational Input Voltage	2000			mV



for $50MHz < f < 6.0\,GHz$

$$SCC22 = SDD22$$

$$= \max\left\{-10, -7.9 + 13.3 * Log_{10}\left(\frac{f}{3.0G}\right)\right\}$$