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06-496r3 SAS-2 Electrical Specification Proposal

Serial Attached SCSI

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SAS-2 Phy Working Group

1/16/07

YOUR PARTNER FOR SUCCESS

Overview

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- Motivation
  - Multiple SAS-2 Test Chips Have Been Built and Tested, SAS-2 Product Designs have Started
  - To Date, We Do Not Have a Electrical Specification or Outline of One.
- Goals
  - Determine a Set of Electrical Specifications that will make SAS-2 Plug-and-Play
  - Need to Select the Specifications such that the Link Margin is Maximized w/o Manual Optimization or Back Channel Communication
  - Neither Under nor Over Constrain the Tx/Rx Devices or Channels
  - Provide an Explicit Definition of Specification and Compliance Test to the Users
- Propose Initial Transmitter and Receiver Electrical Specifications
  - Definitions & Compliance Points
  - Reference Devices
  - Transmitter Device Signaling
  - Receiver Device Signaling
  - Channel Compliance
  - Incomplete list of Open Issues

References

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References:

- 07-037R0 SAS-2 Common Mode Generation Specification (Kevin Witt, Mahbubul Bari VTSS)
- 07-007R2 Proposed 6G SAS Phy Specs for EMI Reduction (Mike Jenkins LSI)
- 07-001R0 Proposal for 6G SAS Phy Specification (Mike Jenkins LSI)
- 06-419R1 SAS-2 Reference Transmitter and Receiver Specification Proposal (Kevin Witt VTSS)
- 06-206R2 SAS-2 Data Eyes vs. De-Emphasis (Kevin Witt VTSS)
- 06-053R0 Roadmap to SAS-2 Physical Layer Specification (Kevin Witt VTSS)
- 06-052R0 Enhanced SFF-8470, SFF-8086 and SATA Cable at 6Gbps (Kevin Witt VTSS)
- 06-049r1 Comparison of Equalization Schemes for 6Gbps SAS Channels (J. Caroselli LSI)
- 05-204R1 Towards a SAS-2 Physical Layer Specification (Kevin Witt VTSS)
- 05-426R0 SAS-2 Cable Reach Objective and Crosstalk (Kevin Witt VTSS)
- 05-425R1 SAS-2 Channel Model Simulations (Kevin Witt VTSS)
- 05-342R0 SAS-2 Adaptive Equalizer Physical Layer Feasibility (Kevin Witt VTSS)
- 05-341R1 Updated Test and Simulation Results in Support of SAS-2 (Kevin Witt VTSS)
- 05-203R0 SAS-2 6Gbps Test Results (Kevin Witt VTSS)

Compliance Points and Devices Should be Consistent with SAS-1

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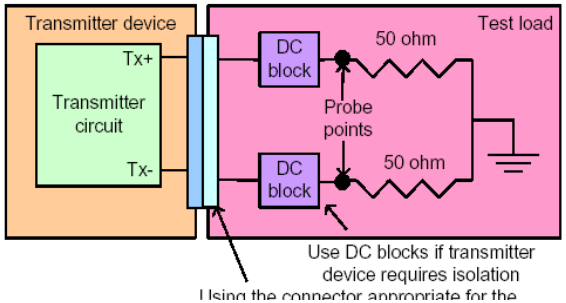
- Compliance Points (SAS1.0 see Section 5)
- Tx Device
- Rx Device
- Zero Length Tx Test Load

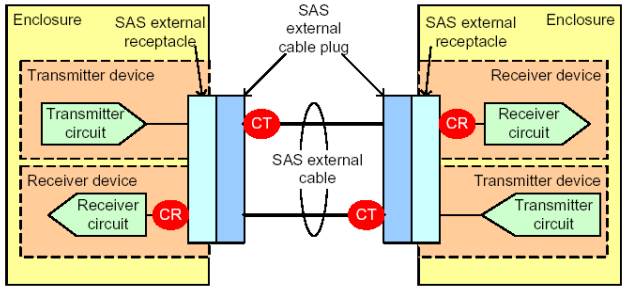
Table 33 — Compliance points

Compliance point	Type	Description
IT	intra-enclosure (i.e., internal)	The signal from a transmitter device (see 3.1.245), as measured at probe points in a test load attached with an internal connector (e.g., with a SAS plug (see 5.2.3.2.1), SAS internal cable receptacle (see 5.2.3.2.2), SAS internal cable SATA-style signal cable receptacle (see ATA/ATAPI-7 V3), SAS backplane receptacle (see 5.2.3.2.3), SAS internal wide cable receptacle (see 5.2.3.4.2), SAS internal wide plug (see 5.2.3.4.3), SAS internal compact wide cable plug (see 5.2.3.4.5), or SAS internal compact wide receptacle (see 5.2.3.4.6))
IR	intra-enclosure (i.e., internal)	The signal going to a receiver device (see 3.1.152), as measured at probe points in a test load attached with an internal connector.
CT	inter-enclosure (i.e., cabinet)	The signal from a transmitter device, as measured at probe points in a test load attached with an external connector (e.g., with a SAS external cable plug (see 5.2.3.3.2), a SAS external receptacle (see 5.2.3.3.3), a SAS external compact cable plug (see 5.2.3.3.5), or a SAS external compact receptacle (see 5.2.3.3.6)).
CR	inter-enclosure (i.e., cabinet)	The signal going to a receiver device, as measured at probe points in a test load attached with an external connector.

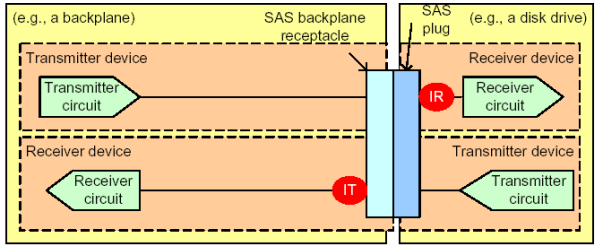


Examples

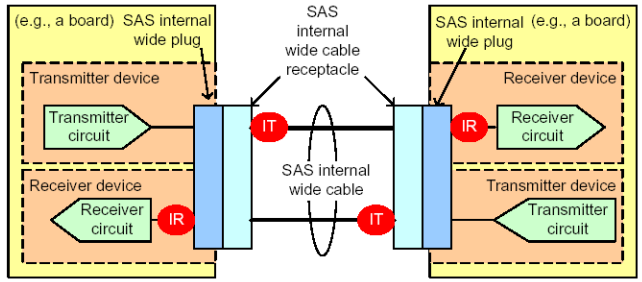
External receptacle/external cable plug



Backplane receptacle/SAS plug



Internal wide cable receptacle/internal wide cable plug



Zero Length Load test Load

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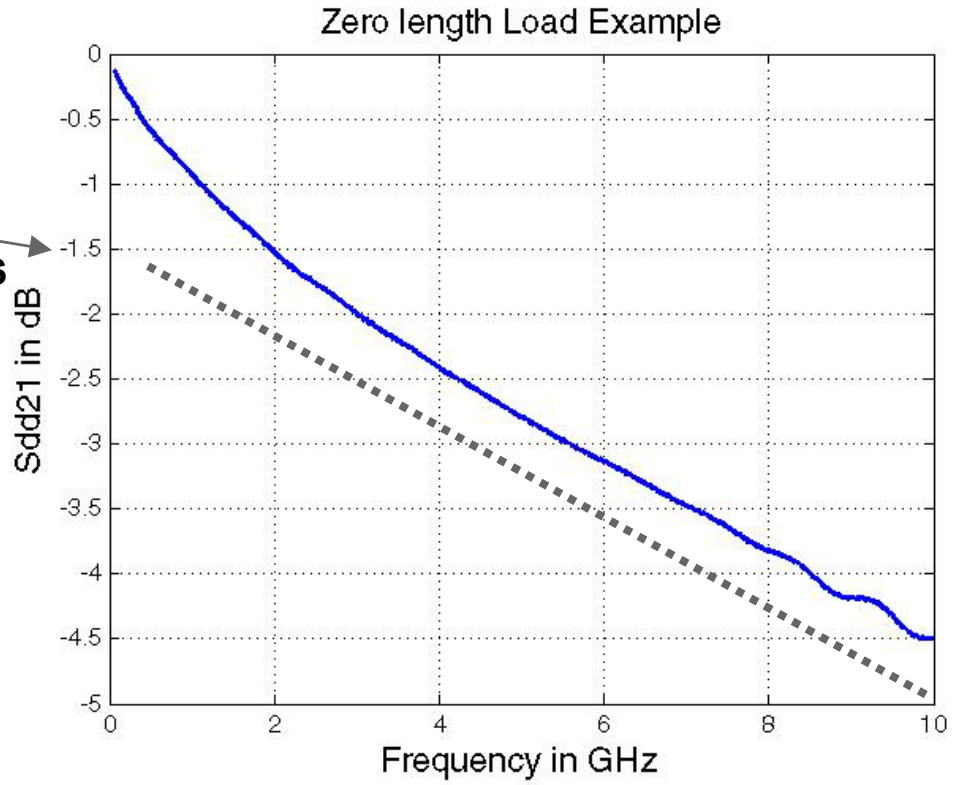
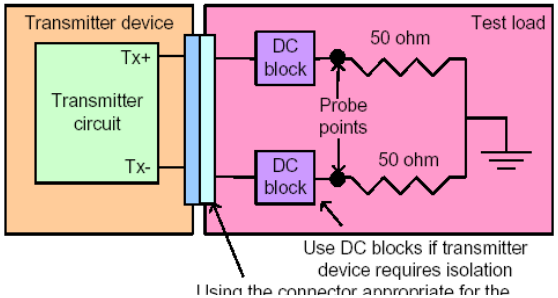
- Propose a limit on insertion loss to normalize test
  - Example load, 24” R/A Co-ax and 2 SMA connectors

Example Insertion loss limit





Reference Devices

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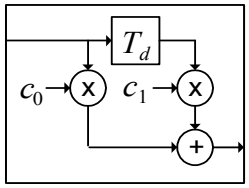
- The Tx and Rx Reference Devices (see T10-419r1)
  - Used for Link Simulation and Channel Compliance
  - Not a Design Guideline, actual Designs must exceed the Performance of these Reference Devices

Reference Transmitter

Reference Transmitter		Units
Ref Tx # Taps De-Emphasis	2	Taps
Ref Tx De-Emphasis	-6	dB
Ref Tx De-Emphasis Tap Spacing	1	UI

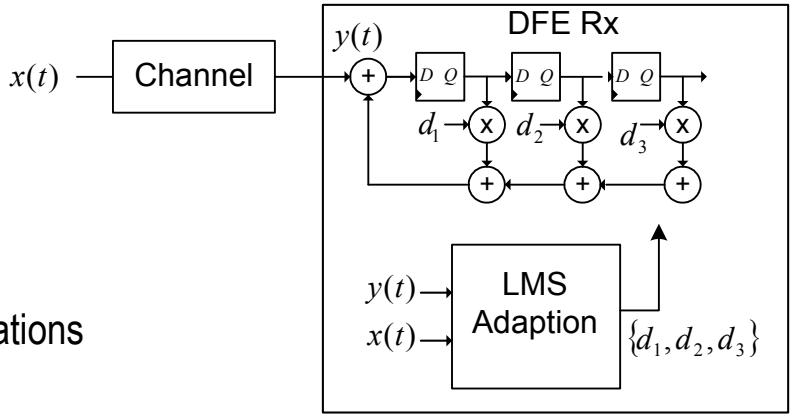


$$DE_{dB} = 20Log_{10}\left(\frac{c_0 + c_1}{c_0 - c_1}\right)$$

$$c_0 = 0.7488 \quad c_1 = -0.2488$$

- Reference Receiver

Receiver		Units
Reference Rx # DFE Taps	3	taps
DFE Tap Spacing	1	UI
Coefficient Adaptation Agorithm	LMS*	



* See Lee and Messerschmitt, Digital Communications

SAS-2 Transmitter Device Proposed Numbers

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Transmitter Device Signal Characteristics

- Measured into a Zero Length Test Load (CT and IT)
- Through a Mated Connector

	SAS-2			
Transmitter	Min	Nominal	Max	Units
Bit Rate		6000		Mbps
Differential Voltage Swing (pk-pk) Vpk	800		1200	mV
Transition Time (20%-80%)	0.25 / 41.667		0.45 / 75	UI /ps
Tx De-Emphasis	-5		-7	dB
Sdd22 Differential Return Loss			see Plot	dB
Scc22 Common Mode Return Loss			see Plot	dB
Sdd22,Scc22 Reference Diff Impedance		100		ohm
Scd22 Differential to Common Mode Conversion			see Plot	dB
Random Jitter			0.15	UI
Deterministic Jitter			0.15	UI
Total Jitter			0.3	UI
AC Coupling Cap			12	nF

Transmitter Device Return Loss SDD11 & SCC11

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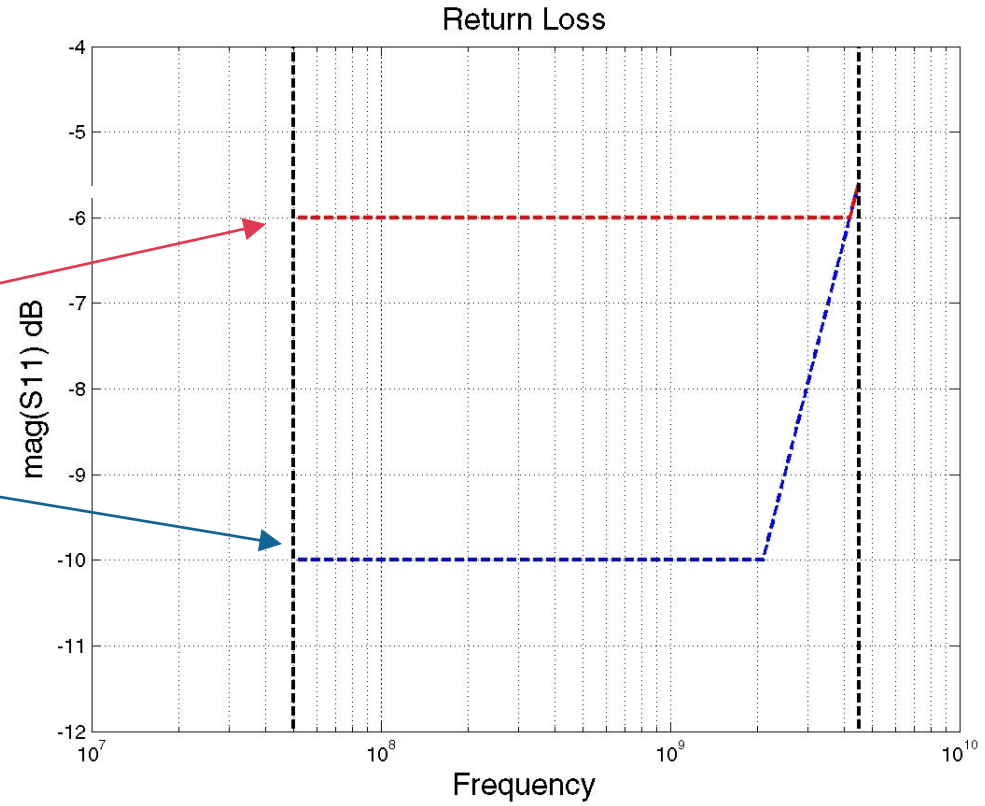
- Based on 8G Fiber Channel (Similar to 10GBase–KR and PCIE 2.0)

for $50MHz < f < 4.5GHz$

$$SCC22 = \max\left\{-6, -7.9 + 13.3 * Log_{10}\left(\frac{f}{3.0G}\right)\right\}$$

$$SDD22 = \max\left\{-10, -7.9 + 13.3 * Log_{10}\left(\frac{f}{3.0G}\right)\right\}$$



Transmitter Device SDC11

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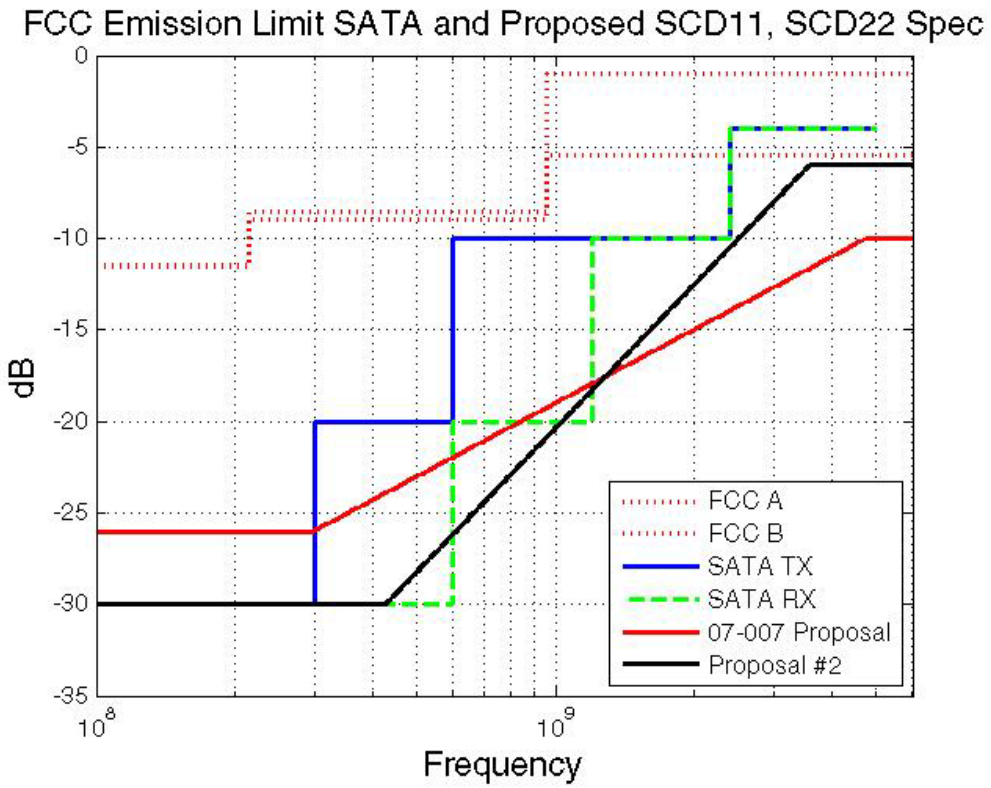
- See 07-007r1 & 07-037r0
- Test Setup
  - Output Active
  - Pattern 1100…
  - TDR or VNA amplitude -8dB of Tx amplitude if adjustable?

$$\text{for } 100MHz < f < 6GHz$$

$$SCD11 < \max\left\{L, \min\left\{H, N + S * Log_{10}\left(\frac{f}{3.0G}\right)\right\}\right\}$$

$07-007\text{r}0 \quad L = -26,\ H = -10,\ N = -12.7,\ S = 13.3$

$\text{Proposal } \#2 \quad L = -30,\ H = -6,\ N = -8,\ S = 26$



Transmitter Device DE and Max Voltage Swing

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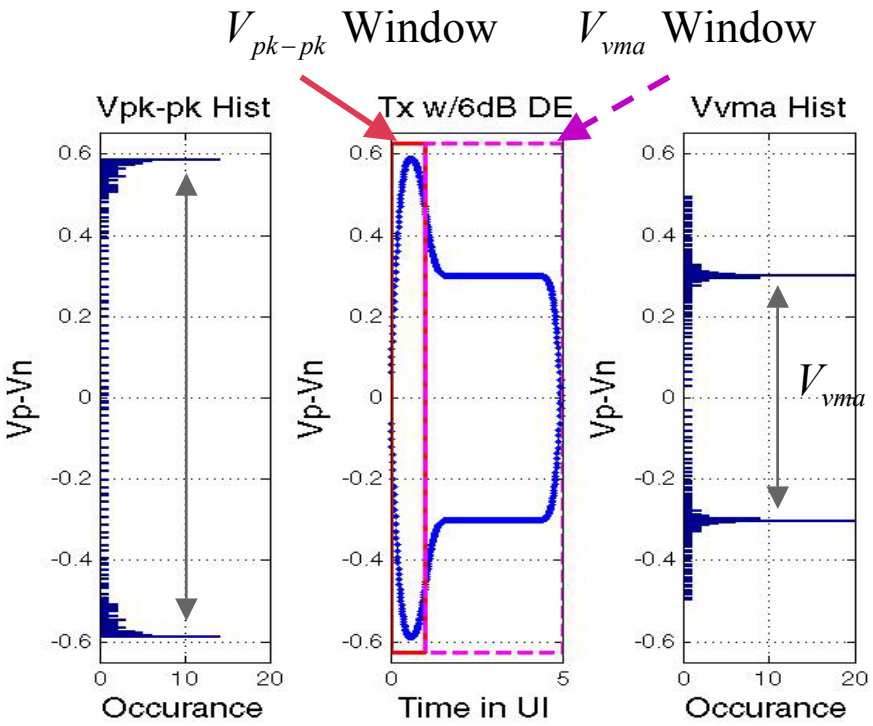
Test Setup Overview

- Measured with Zero Length Test Load
  - CT and IT
- Sampling or Real-time scope with Histogram Function
  - Vpk-pk Sample Window is 1UI wide after each transition's zero crossing
  - Vvma Sample Window is 4UI wide 1UI after each transition's zero crossing
  - Vvma is based on Peak Position in Histogram
- 0000011111 Pattern



$$DE_{dB} = 20Log_{10}\left(\frac{V_{pk-pk}}{V_{vma}}\right)$$

Transmitter Device DE and Max Voltage Swing

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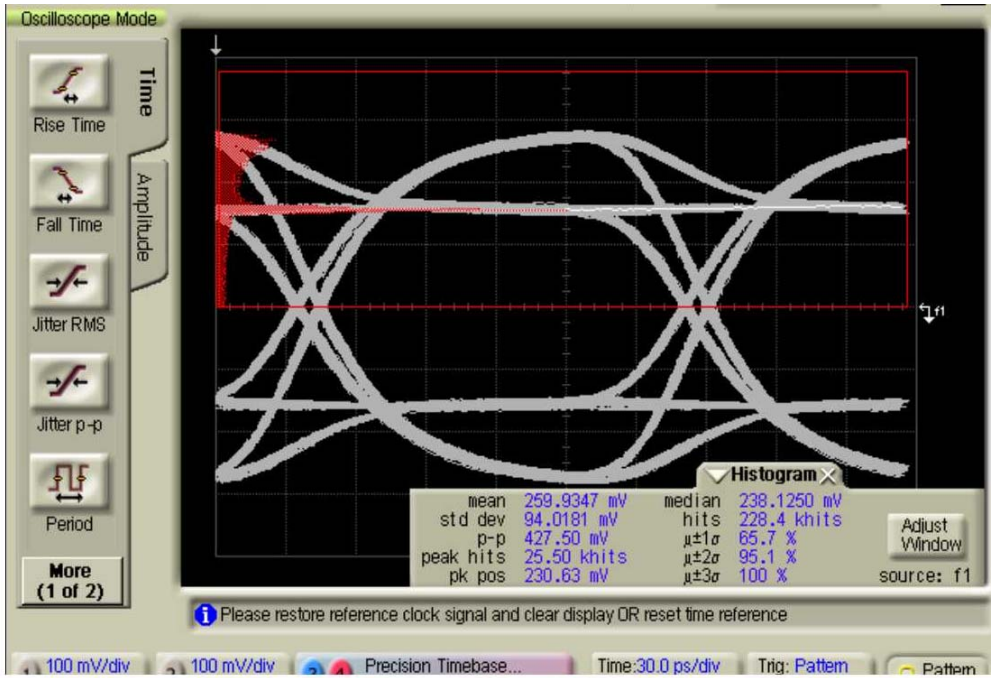
- Compliant Tx Device Example (w/ CJTPAT)
  - From T10 07-001r1
  - 2 Histograms taken {0→ Vmax and 0→ Vmin}



V_{pk-pk}

V_{vma}

$$V_{pk-pk} = 955mV$$

$$V_{vma} = 461mV$$

$$DE_{dB} = 20Log_{10}\left(\frac{V_{pk-pk}}{V_{vma}}\right)$$

$$DE_{dB} = 20Log_{10}\left(\frac{955}{461}\right) = 6.3dB$$

$$427mV \le V_{vma\_spec}(V_{pk-pk} = 955mV) \le 537mV$$

- V_{vma} = Peak position 1s - Peak position 0s

Vpk-pk mV	Vvma mV	DE (dB)	DE Vtol	DE Vtol %
955	537	-5		
955	479	-6	110	23%
955	427	-7		

Response to Concerns in 07-001r1 "Reasons not to Specify TX De-emphasis"

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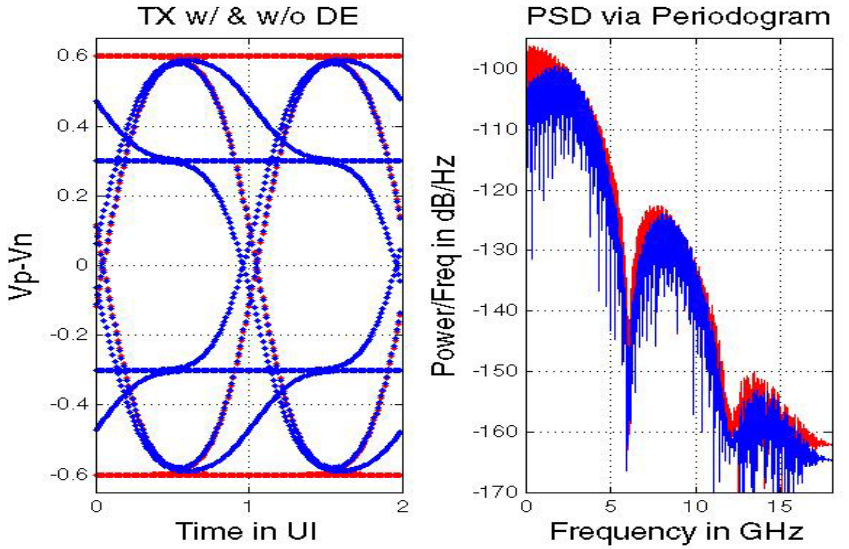
- Concern: "Mandates a high EMI TX waveform even if it isn't needed"
- Response: For a given Tx Amplitude the PSD of a De-Emphasized Waveform has a Lower PSD and thus lower EMI.
- Detail:
  - Our assumption on EMI reduction is that radiated energy is proportional to SCD11 (07-007 page 4) and the transmitted waveform shape.

$$\left|EMI(f)\right|^2 \sim K \cdot \left|SCD_{11} \cdot Tx(f)\right|^2$$

  - For a Given Peak to Peak Amplitude the PSD of a PRBS7 Waveform has Lower Energy at all Frequencies.



$$\left|Tx(f)\right|^2$$

Response to Concerns in 07-001r1 "Reasons not to Specify TX De-emphasis"

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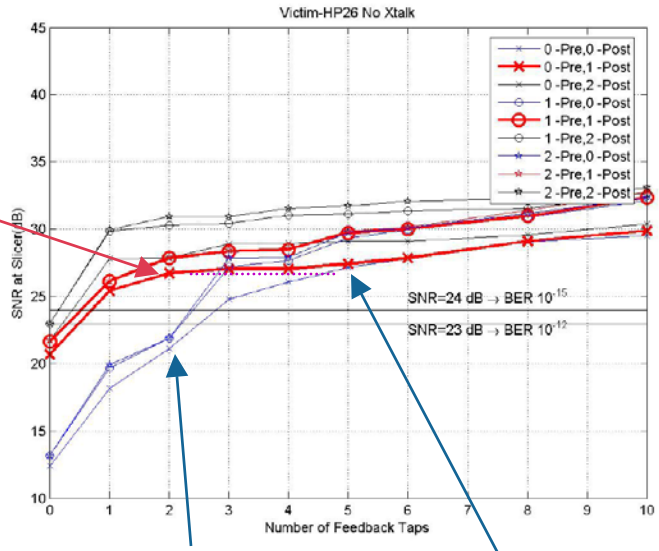
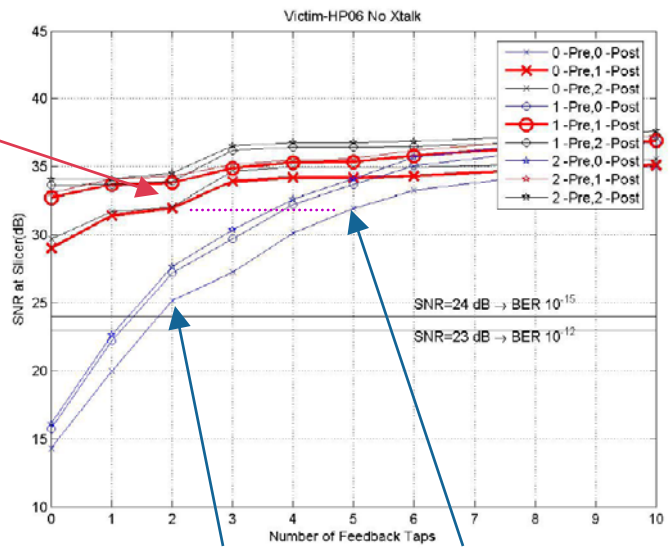
- Concern: "RX equalization (DFE) is equal to or better performance compared to TX emphasis"
- Response: This is not true for all T10 channels and the proposed reference DFE receivers.
- Detail: Examples from LSI analysis in 06-049r1, LSI Reference Rx = 2 tap DFE (07-001r1)



2 tap DFE w/o DE

2-Tap DFE w/o DE

5-Tap DFE w/o DE = 2tap w/ DE



2 tap DFE w/o DE

2-Tap DFE w/o DE

5-Tap DFE w/o DE = 2tap w/ DE

Response to Concerns in 07-001r1 "Reasons not to Specify TX De-emphasis"

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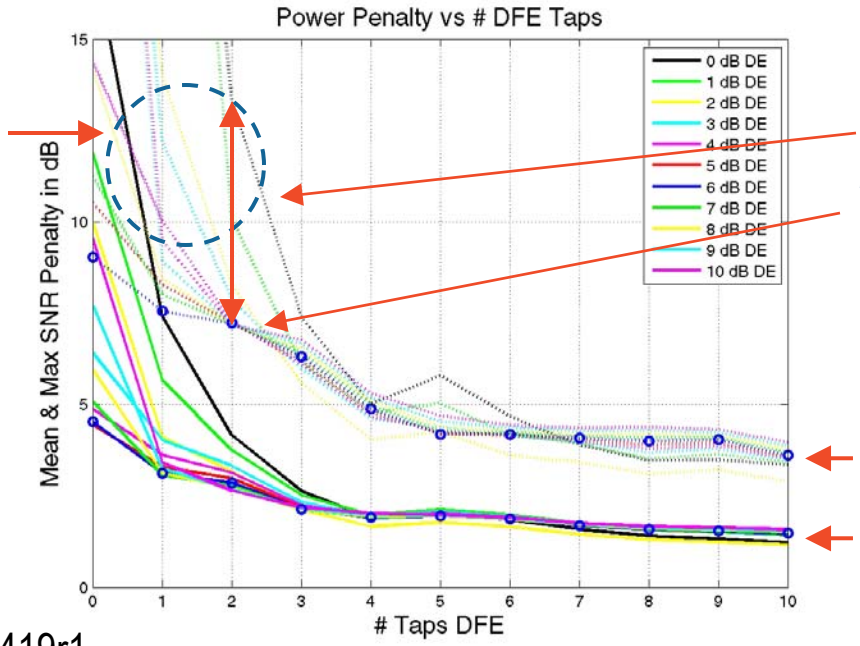
- Concern: "RX equalization (DFE) is equal to or better performance compared to TX emphasis"
- Response Continued: We need to look at all channels and optimize the link margin hence minimize the theoretical power penalty.
- Detail: SAS-2 Links will have more ensemble average and worst case link margin with De-Emphasis than without.

Need to Avoid this Area to Avoid Interoperability Issues



Benefit of De-Emphasis
1) Reduction in PP
2) Reduction in PP slope

Max (dash)

Mean (solid)

From T10 06-419r1

Response to Concerns in 07-001r1 "Reasons not to Specify TX De-emphasis"

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- Concern: "Details of waveform depend on details of TX-to-compliance point path 2-3 "FR-4 take "
- Response: This is an issue with all the transmitter device specifications. I'm not opposed to budgeting for IC to compliance point.

Response to Concerns
"Verbal Concern"

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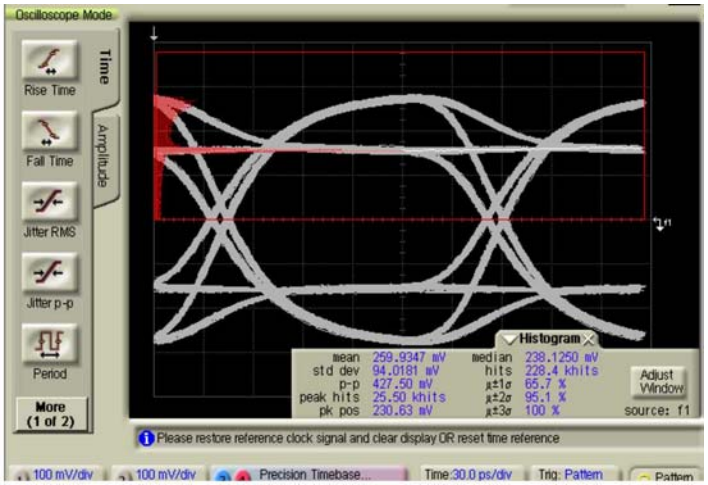
- Concern: "De-Emphasis Penalizes Short Links"
- Response:
  - We have seen no issues with short links in our lab or in simulations.
  - For example, the waveform below has a 430mV inner eye opening. Our adaptive and limit amplifier based CDRs have no issues with this kind of waveform.
  - These channels will operate with more link margin than the most stressful links and should not drive the specification.



SAS-2 Receiver Device Proposed Numbers

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Receiver Device Signal Characteristics

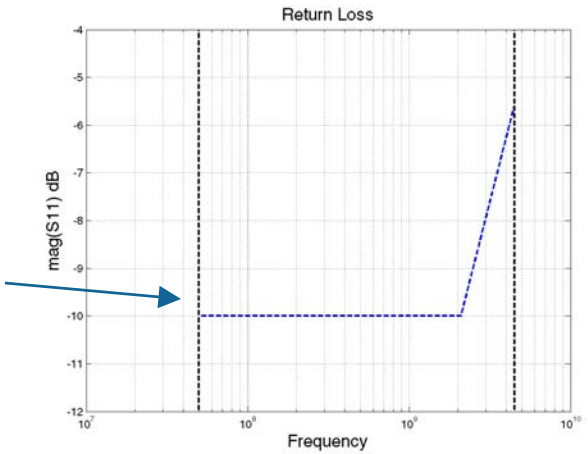
- Measured at (CR and IR)

	SAS-2			
Receiver	Min	Nominal	Max	Units
DC Differential Impedance		100		ohm
DC Common Mode Impedance		50		ohm
Differential Return Loss			See Plot	
Common Mode Return Loss			See Plot	
Common-Mode Tolerance (2-200MHz)	150			mV
Max Operational Input Voltage @ 6GBps	1200			mV
Max Non-Operational Input Voltage	2000			mV

for $50MHz < f < 4.5GHz$

$$SCC22 = SDD22$$

$$= \max\left\{-10, -7.9 + 13.3 * Log_{10}\left(\frac{f}{3.0G}\right)\right\}$$



Jitter Tolerance Mask TBD

Rev 3 Changes:
1) Used Mikes Formula, same curve

Receiver Device SDC11

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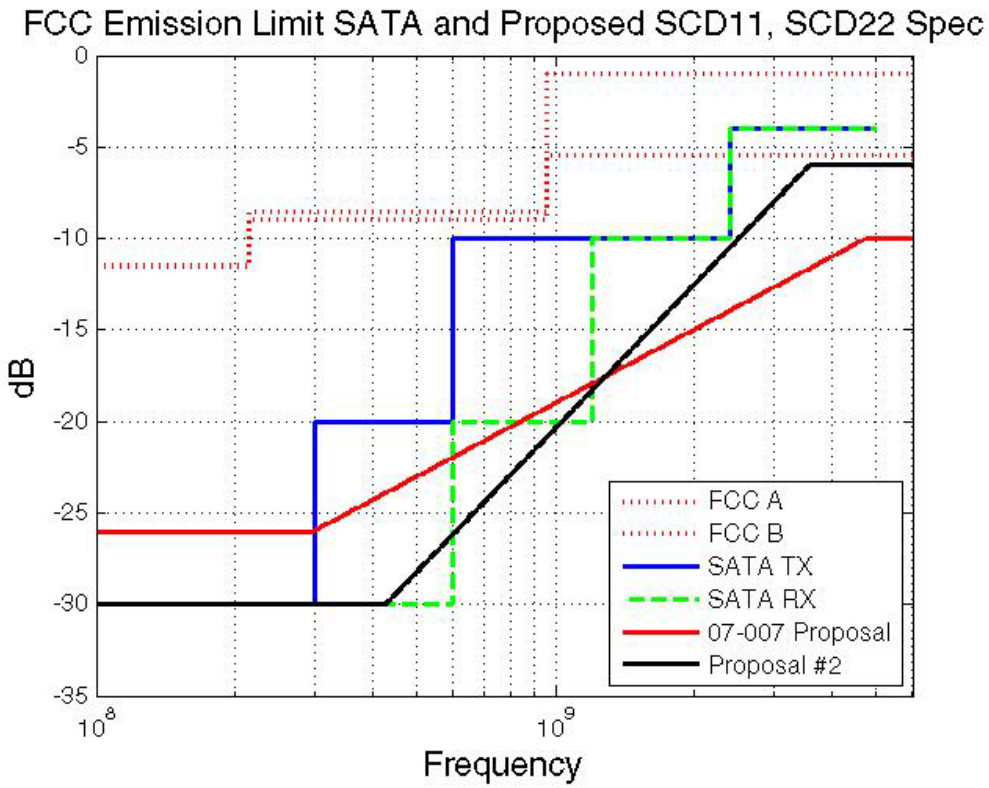
- See 07-007r1 & 07-037r0
- Test Setup
  - Rx Power Enabled (SAS-2 Data Mode)
  - TDR amplitude ?

$$\text{for } 100MHz < f < 6GHz$$

$$SCD11 < \max\left\{L, \min\left\{H, N + S * Log_{10}\left(\frac{f}{3.0G}\right)\right\}\right\}$$

$07-007r0 \quad L=-26,\ H=-10,\ N=-12.7,\ S=13.3$

$\text{Proposal \#2} \quad L=-30,\ H=-6,\ N=-8,\ S=26$



SAS-2 Channels

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- A Compliant Channel
  - Any Channel Which Will Operated at 1e-12 With the Given Reference Transmitter and Receiver Device.
  - Operation is Defined as Passing Link Analysis at the TBD Worst Case Corner.
  - Simulation Methodology is up to the User, but is Expected to be Based on Estimated/Measured S-Parameters and Digital Communication Analysis Techniques.
- SAS-2 S-Parameter Models Posted to the T10 Serve as Guidance

Incomplete List of Issues

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- Tx Jitter Generation
  - SSC Causes Measurement Issues
    - Waiting for presentation on SATA approach.
  - Tx De-Emphasis
    - Causes DJ Which Needs to be Removed Before Jitter Generation Can Be Estimated?
    - Could use 1010, 1100 & 11110000 patterns
- Rx Compliance Test.
  - We should have one, it could be a normative test.
- Rx Jitter tolerance
  - Need proposal on mask, channel, test configuration…

Summary

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- Electrical Transmitter and Receiver Device Specifications Provided

Additional Information

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- Power Penalty Analysis of T10 Links w/ and w/ De-Emphasis
- Rx Compliance Test ISI Generator (From 06-053r0)

Behavior Simulation Methodology

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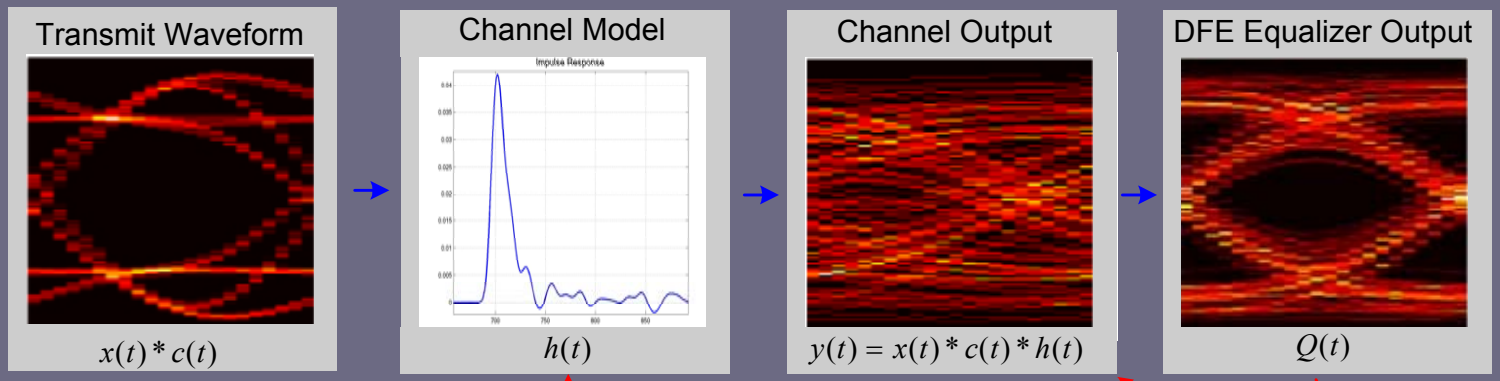
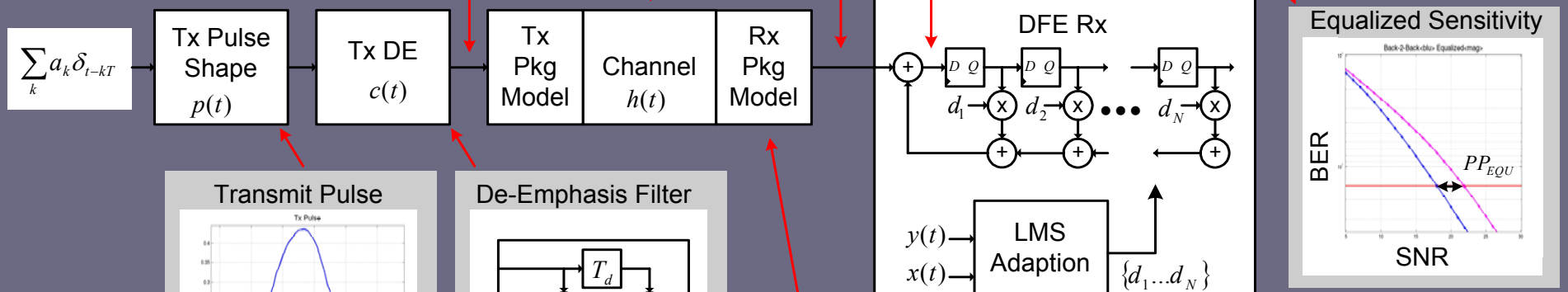
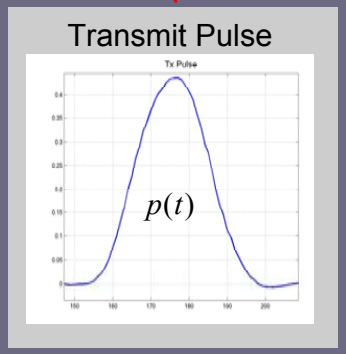
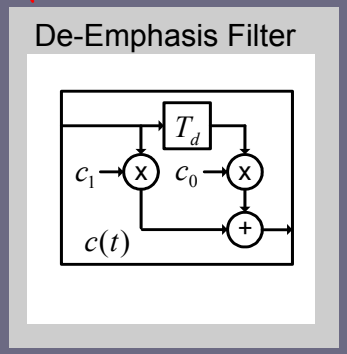
S-Parameter Based Channel Mode









Pulse Shape Based on Test Chip

Mellitz Capacitive Package Mode RL~ 7dB @3GHz

Semi-Analytic BER Used to Estimate Sensitivity Plot

Visual Check of Simulation Methodology

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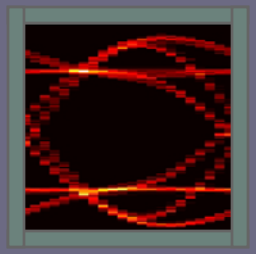
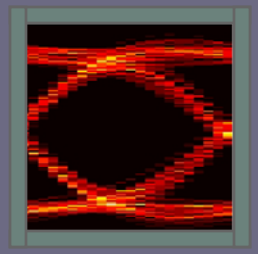
- Simulation vs. Measured
  - 6 Gbps Output Driver Test Chip
  - 6dB 2 Tap De-Emphasis
- Good Agreement With Measured
  - Eye Opening and Eye Shape
  - Jitter at Zero Crossing

6dB De-Emphasis Simulated Eyes

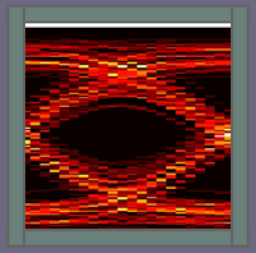
1m



6m



10m



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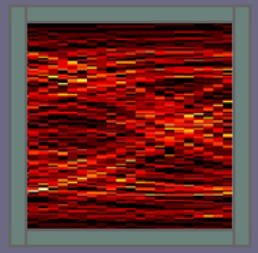
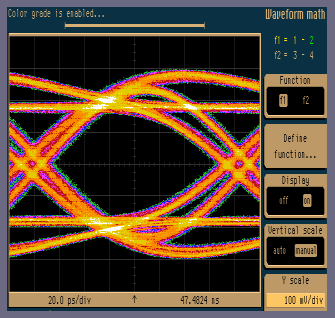


6dB De-Emphasis Measured Eyes

1m



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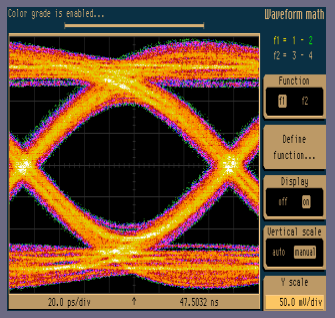
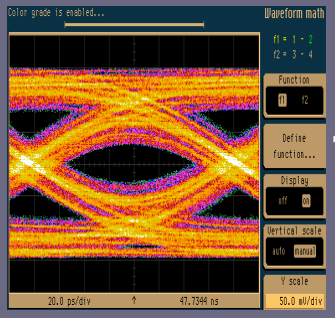
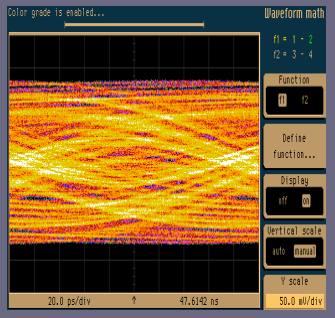


10m



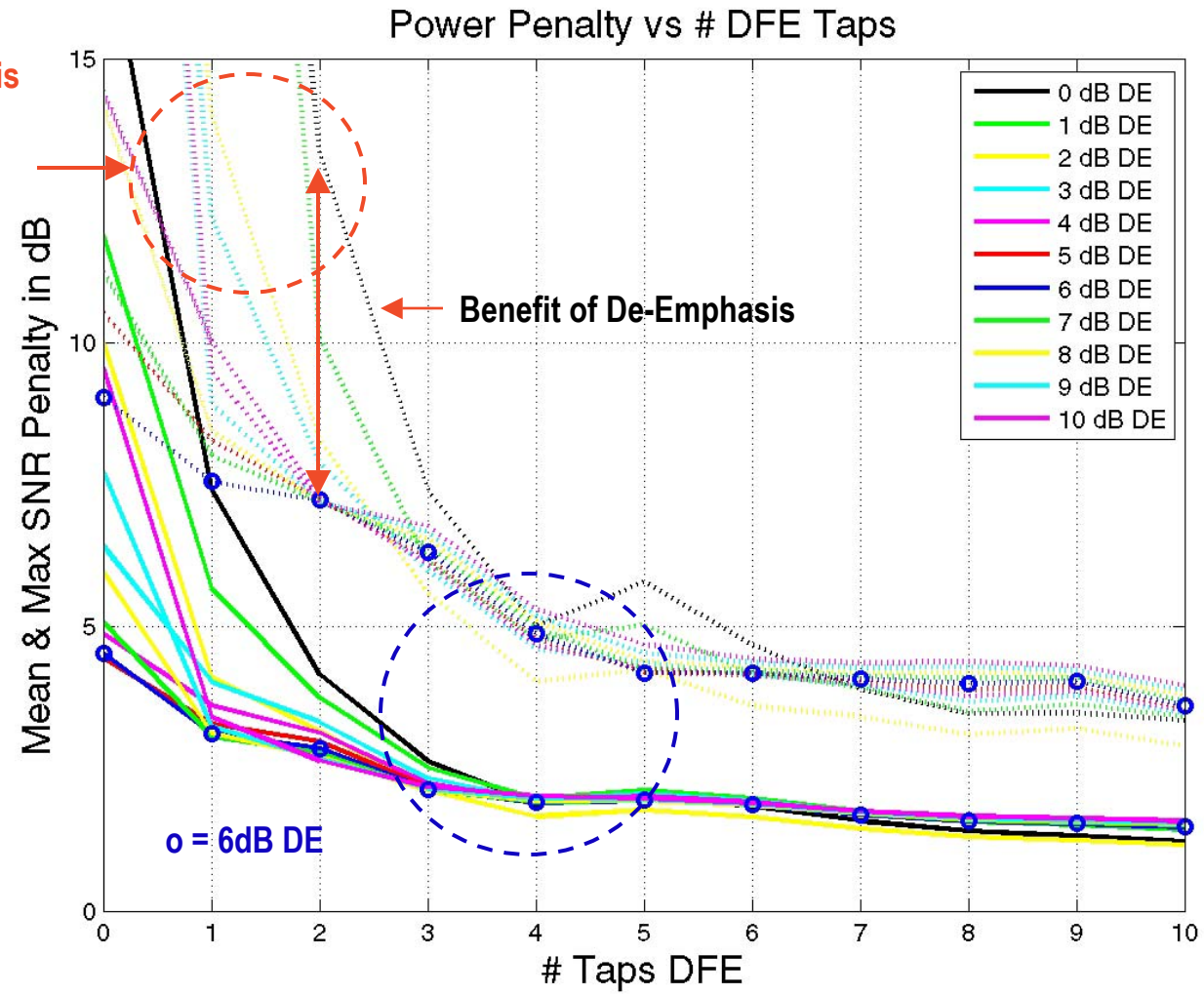
15m



What is the Optimal # DFE Taps & DE Setting?

VITESSE

- Look at all 3388 Power Penalty Results as a Family of Curves vs. # DFE Taps
  - From T10 06-419r1



3 or 4 Tap DFE
6 dB DE
Appears to Be a Reasonable Reference Rx/Tx

Max (dash)

Mean (solid)

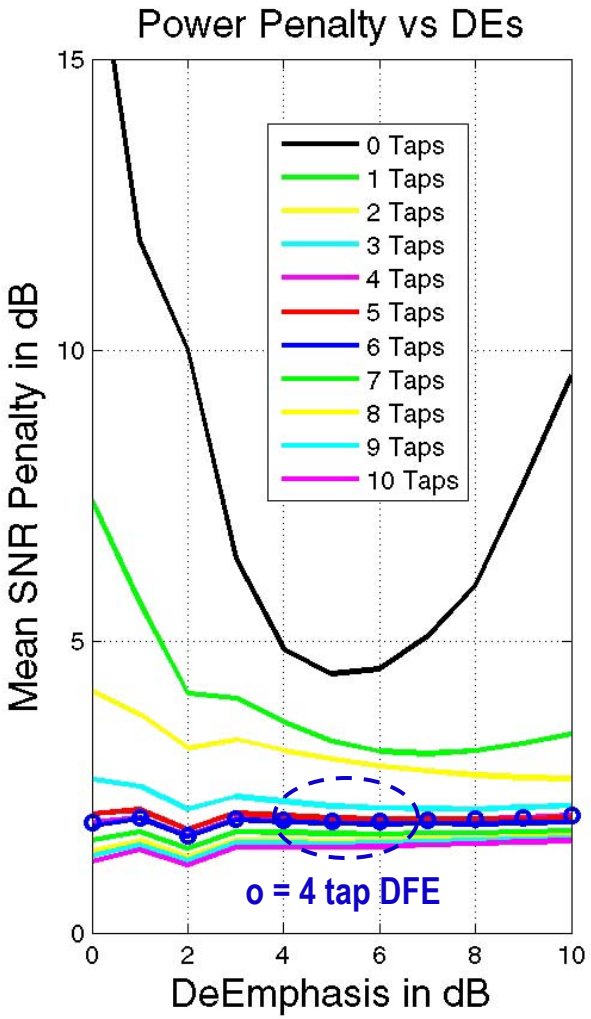
Slice the Results the Other Way

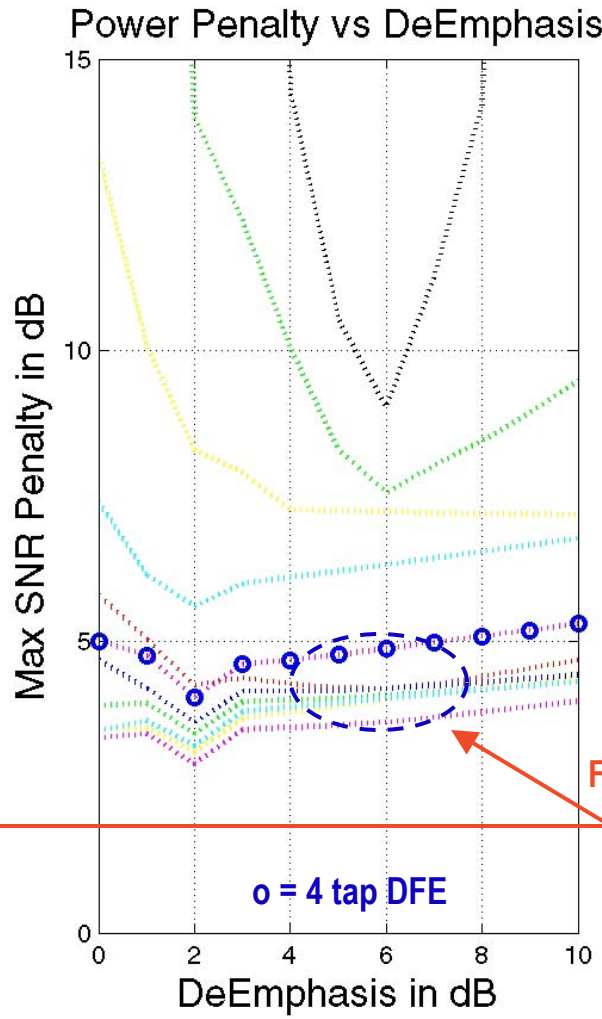
VITESSE

- Look at all 3388 Power Penalty Results as a Family of Curves vs. De-Emphasis
  - From T10 06-419r1

With Enough DFE We Do Not Need De-Emphasis
But the Link Would Be More Susceptible to DFE Error Propagation

Increasing # DFE Taps





3 or 4 Tap DFE
6 dB DE
Appears to Be a
Reasonable
Reference Rx/Tx

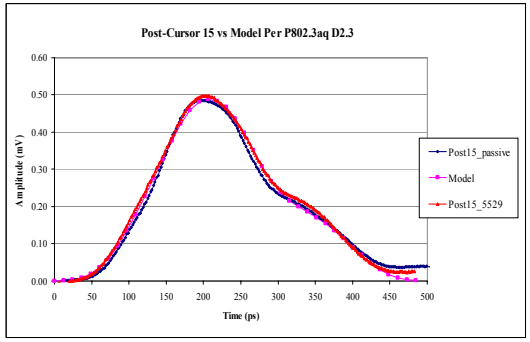
Flatness Indicates No Need to Over Constrain the De-Emphasis

SAS-2 Receiver Compliance Test Hardware See 06-053r0

VITESSE

- Receiver Compliance w/ Jitter, Crosstalk and Interference (same as OIF-CEI, & 10GBase-KR)
- Standardize Test Setup based on 10GBase-LRM ISI Generator
  - Generate ISI coefficients for channels of Interest
  - Calibrate and Test Through Mated Connector
  - Emulate Tx DE, C_{TX} & C

10GbE MMF Example



Needs Mod for SSC