



A Look At COMWAKE For Use In SNW3

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The Transmitter

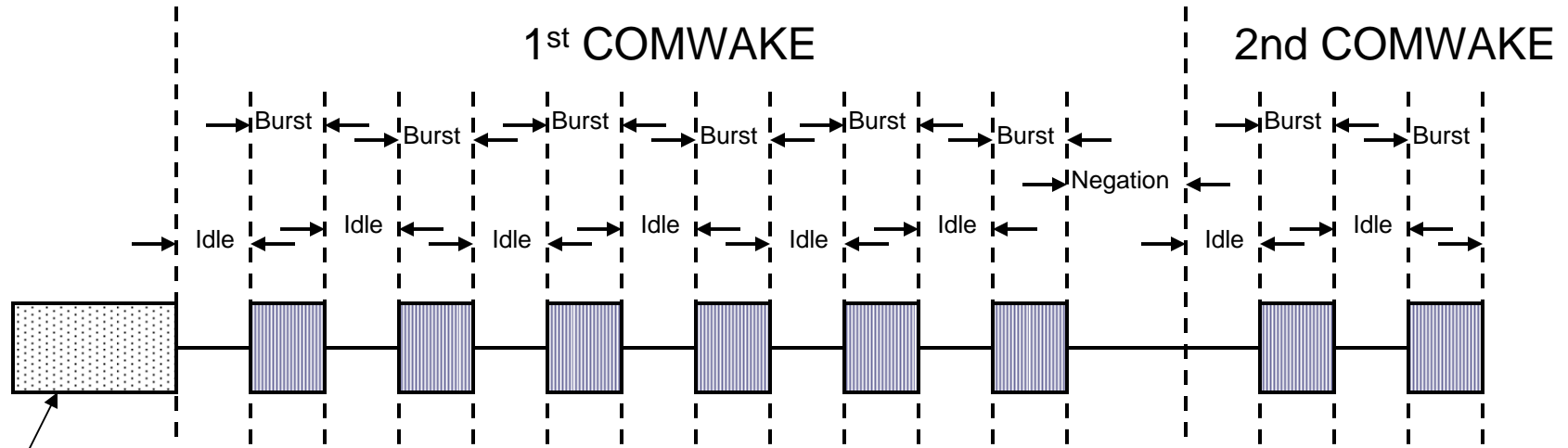
▣ Transmitters send COMWAKEs with precise timing

▣ A COMWAKE is

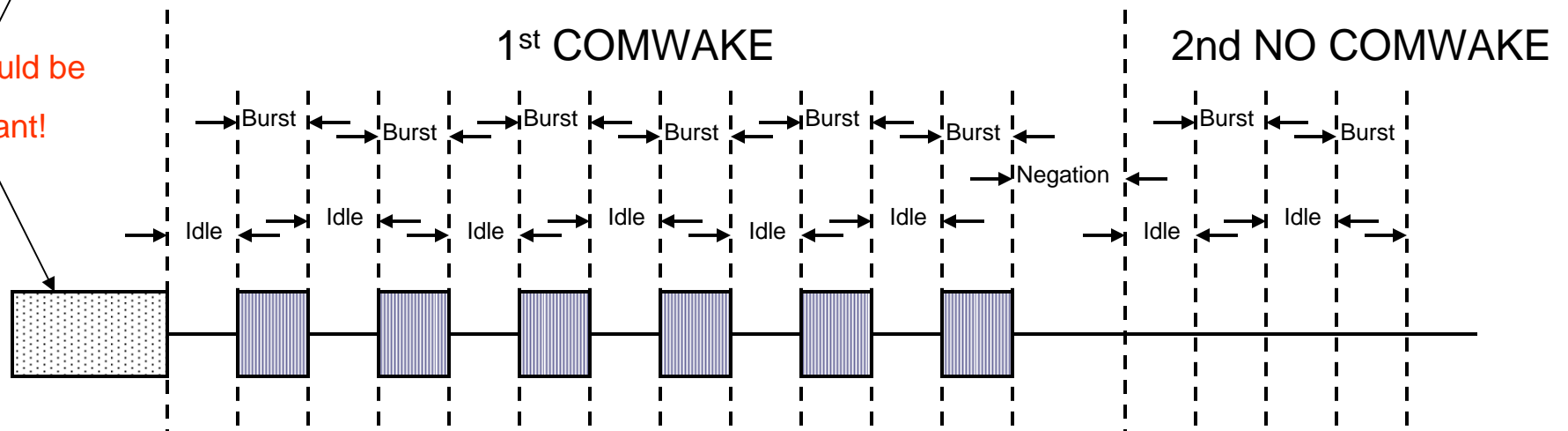
- Gap	160 OOBIs	(106.666 ns)
- Burst	160 OOBIs	(106.666 ns)
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- Gap	160 OOBIs	(106.666 ns)
- Burst	160 OOBIs	(106.666 ns)
- Negation Gap	280 OOBIs	(186.666 ns)
TOTAL	2200 OOBIs	(1466.666 ns)

▣ For each “bit window” the transmitter either sends this sequence

Transmitted COMWAKE



These could be
Important!



Receiver COMWAKE Requirement

- Detection of a COMWAKE requires detection of 4 consecutive Idle time/Burst time pairs. (Idle first, then Burst)

COMWAKE Detection

- A receiver “may detect” a Burst with as little as one transition.
 - No minimum detected Burst time specified
 - Shall at 100 ns
 - No maximum Burst time specified
 - But transmitter must send it right!
- A receiver must wait for the next Burst to start to determine if an Idle time is of the proper size.
 - There is a maximum Idle Time that must be met to declare the Idle time a valid COMWAKE Idle time.

COMWAKE Detection Uncertainty

□ From the time that the beginning of a COMWAKE appears at the input of the Receiver to the time that the Receiver signals the detection of the COMWAKE is:

Earliest: 1280 OOBIs (746.66 ns)

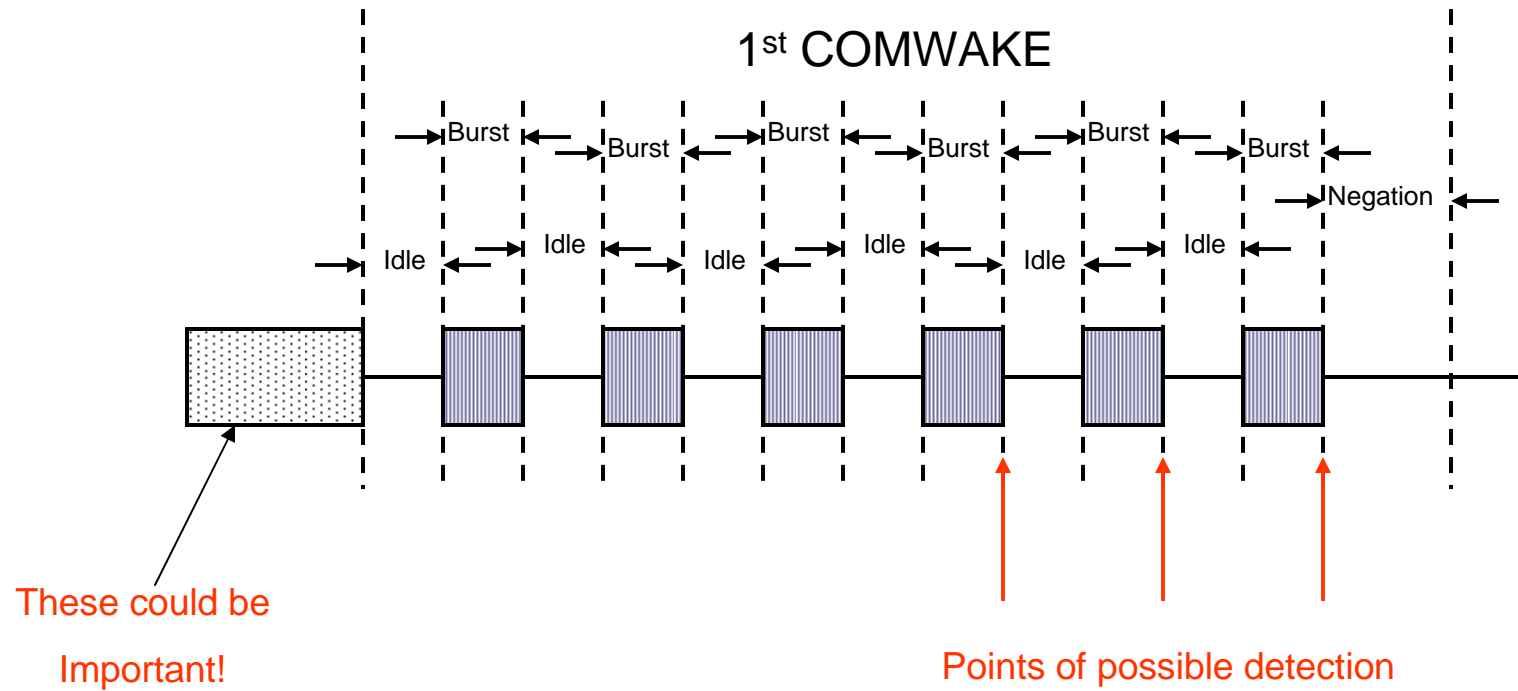
4 Idle times plus 4 Burst times

Latest: 1920 OOBIs (1280.00 ns)

Detect at the end of the last Burst.

□ Uncertainty: 640 OOBIs (426.66 ns)

Receiving COMWAKE



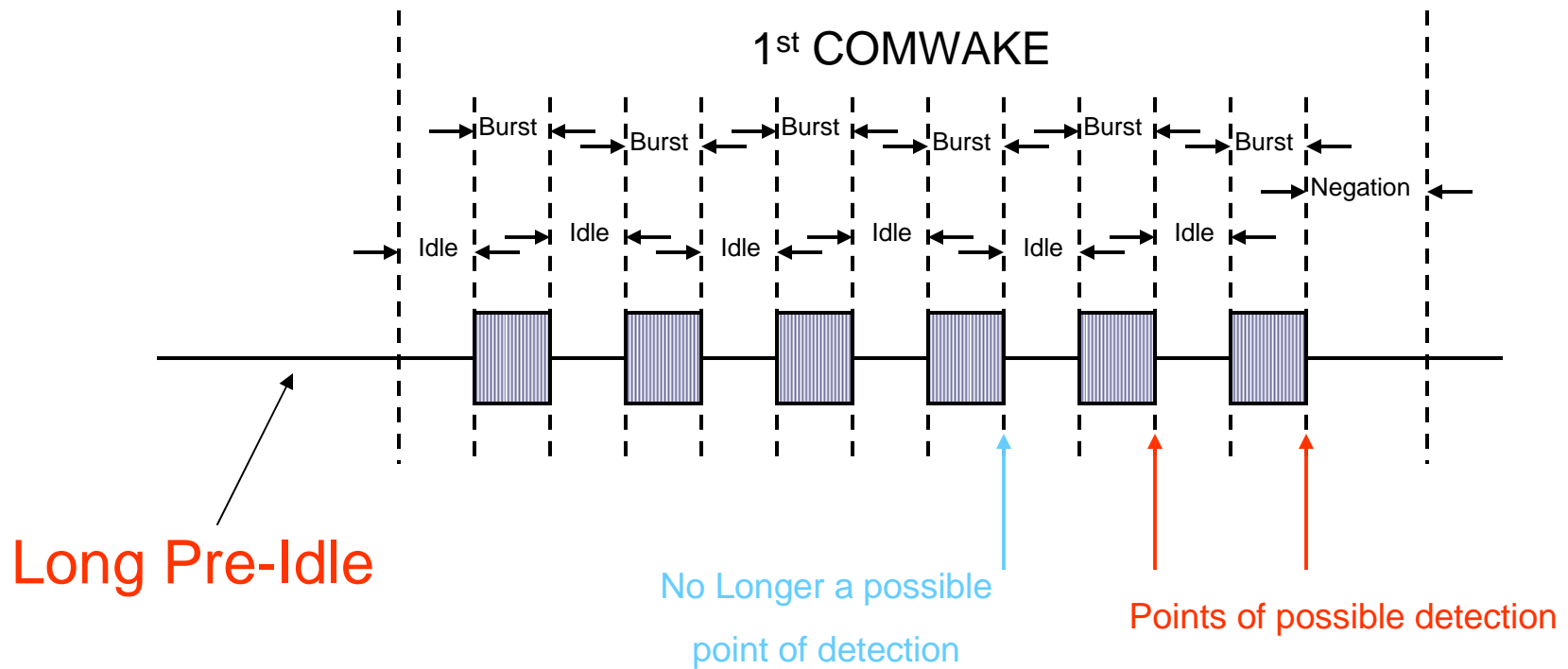
Not Quite So Uncertain

- ▣ If the COMWAKE is preceded by more 68.67 ns of idle time, then the first Idle time/Burst time pair are disqualified because the Idle time exceeds the “shall not detect” time.

Shall not detect:		175.00 ns
Transmitted time	-	106.66 ns
		<hr/>
Maximum “pre-idle”		68.67 ns

- ▣ This WILL occur for each “bit time” other than the first.
 - The COMWAKE negation time insures it.
- ▣ We can require it before the first COMWAKE

Not Quite So Uncertain



COMWAKE Detection Uncertainty With Long Pre-Idle

□ From the time that the beginning of a COMWAKE appears at the input of the Receiver to the time that the Receiver signals the detection of the COMWAKE is:

Earliest: 1600 OOBIs (960.00 ns)

5 Idle times plus 5 Burst times.

Latest: 1920 OOBIs (1280.00 ns)

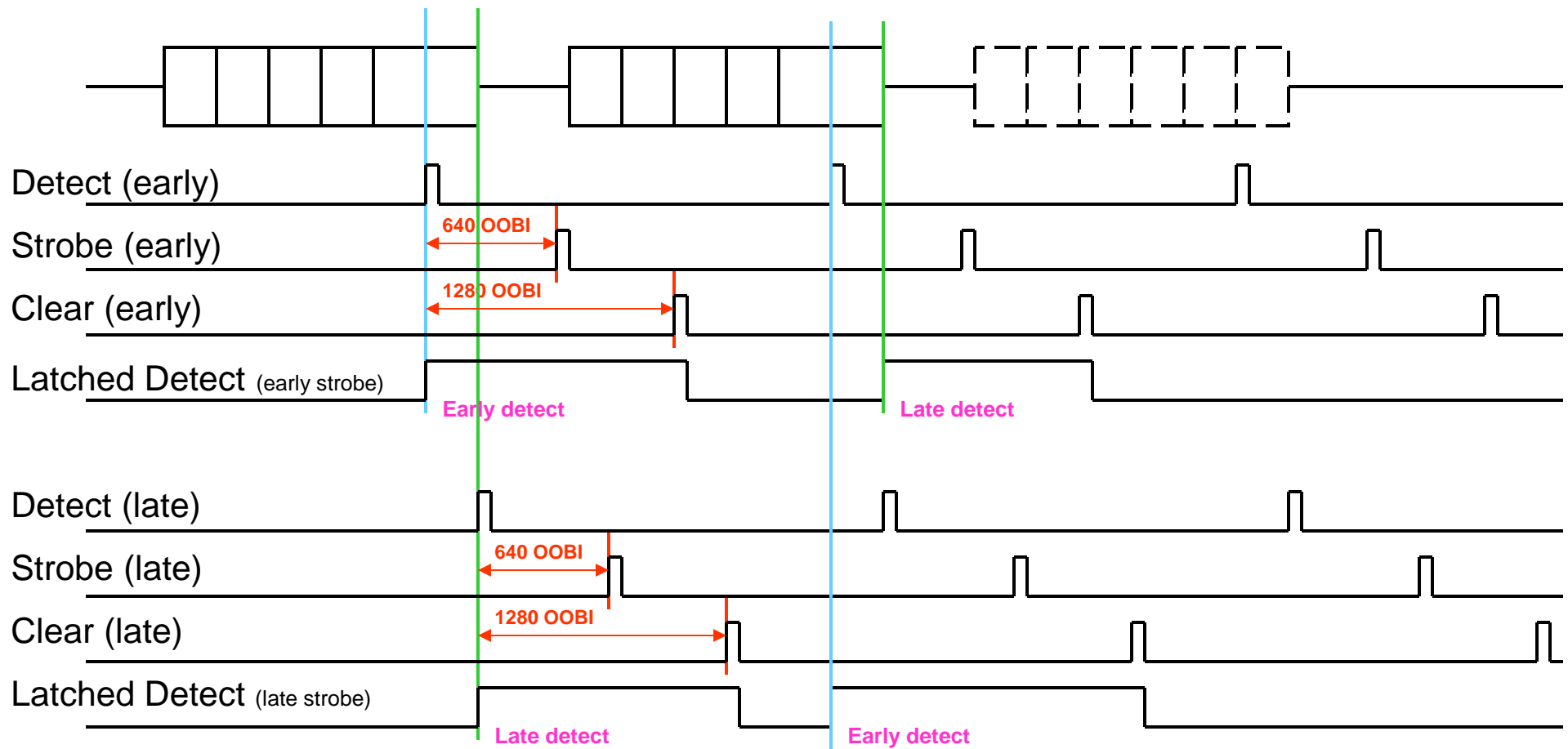
Detect at the end of the last Burst.

□ Uncertainty: 320 OOBIs (213.33 ns)

Sampling Is Easy And Accurate

- ▣ Detect the first COMWAKE.
- ▣ Use this as the time reference
- ▣ Generate a Strobe 640 OOBIs after the first detect and every 2200 OOBIs after that.
- ▣ Generate a Clear 1280 OOBIs after the first detect and every 2200 OOBIs after that.
- ▣ Set a flop every time a COMWAKE is detected.
- ▣ Sample the flop on every Strobe
- ▣ Clear the flop on every Clear.

Sampling Is Easy And Accurate



Reference Clock Tolerance

- ▣ We will have to consider the Reference Clock tolerance (+/- 100 ppm).
- ▣ If the transmissions are limited to the 109 usec SNTT time, and we use 2 times the clock tolerance as the difference between the transmitters frequency and the receivers frequency,
then the maximum clock delta is less than 33 OOB.
- ▣ We have nearly 10 times that in window opening

Conclusions

- It can be done, easily.
- One simple solution can be shown. Many other implementations are possible.
- The only requirement is that the transmitter keep the bus Idle for a minimum of 68.67 ns before sending the sequence of bits.
- If we keep the requirements for RCDT field, this requirement is met.

A Look At The Effect Of SSC

- Assume SSC is at the slowest modulation rate
 - 30KHz =
 - 33.33 usec =
 - 50,000 OOBIs (33.33 us / .666 ps)
- Assume a worst case modulation technique of a square wave
 - Modulation must be balanced, so only
 - 16.66 usec at one extreme, 16.66 at the opposite extreme
 - Gives 25,000 OOBIs during the extreme period
- Assume both sides have worst case in opposite directions
- Assume one side is +2500 ppm, the other -2500 ppm
 - 5000 ppm total difference
- $25,000 \text{ OOBIs} * 5000/1000000 = 250 \text{ OOBIs maximum drift}$

A Look At The Effect Of SSC

- ▣ We have a 320 OOB1 margin built in using to described solution
 - Without trying to optimize the Strobe and Clear positions
- ▣ The selection of the Strobe point was arbitrary
 - It could be moved to one clock before the Clear
 - And would improve margin
- ▣ Conclusion: NO ISSUES

Another Look At The Effect Of SSC

- ▣ Assume worst case clock difference for the entire 32 bit sequence: 5000 ppm clock difference
- ▣ One COMWAKE is 2200 OOBIs
- ▣ 32 COMWAKEs is 70,400 OOBIs
- ▣ 5000 ppm on 70,400 = 352 OOBIs
- ▣ We have a built in 640 OOBIs optimal margin
- ▣ Results: Over a 200 OOBIs actual margin

For The Non-Believers

- I ran a simulation with two clocks
 - Base frequency 1.5GHz
 - Transmitter +2500 ppm fixed
 - Receiver -2500 ppm fixed
 - And a second simulation with the clocks reversed
- Generating the Strobe and Clear signals as defined
- Using a range of initial clock phase relationships
 - All relationships in 1 fs steps
- With All 1's, All 0's and alternating 1's and 0's patterns.
 - The exception is that the start bit was 1 in all patterns
- Verifying the data.
- Simulation passed.
 - Measurement of window margin on 32nd bit confirms that margin is over 200 OOB