To: T10 Technical Committee
From: Rob Elliott, HP (elliott@hp.com)
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Subject: 06-363r0 SAS-2 SNW-3 bit definitions

Revision history
Revision 0 (2 August 2006) First revision

Related documents
sas2r05a - Serial Attached SCSI - 2 (SAS-2) revision 5a
05-397 SAS-2 Start-up training sequence (Harvey Newman, Infineon)
06-263 SAS-2 Spread-spectrum clocking (Rob Elliott, HP)
06-295 SAS-2 Speed negotiation (Amr Wassal and Robert Watson, PMC-Sierra)
06-354 SAS-2 Startup training sequence proposal (Steve Finch, ST Microelectronics)
06-355 SAS-2 SNW-3 Definition (Amr Wassal and Robert Watson, PMC-Sierra)

Overview
06-355 defines a new format for the G3 speed negotiation window (renamed SNW-3) that exchanges phy capability information using OOB signals.

The format of that information needs to be defined.

Suggested changes

[to be placed in the SNW-3 description area]

The phy shall negotiate to the highest commonly supported settings based on the outgoing and incoming SNW-3 supported settings bits. The Table 1 defines the priority of the SNW-3

Table 1 — SNW-3 negotiation priority of supported settings

Priority	Supportd setting
Highest	G3 with SSC
...	G3 without SSC
...	G2 with SSC
...	G2 without SSC
...	G1 with SSC
Lowest	G1 without SSC

If a phy reset problem occurs (i.e., the phy does not successfully negotiate the highest commonly supported setting in the final SNW), if the next link reset sequence include a SNW-3, the phy shall disable the highest commonly supported setting and any higher priority settings and set the DEGRADED bit to one (e.g., if a phy supports G1, G2, G3 without SSC, and G3 with SSC, and it fails to negotiate G3 without SSC in the final SNW, it shall disable G3 without SSC and G3 with SSC during the next link reset sequence).

Table 2 defines the SNW-3 bits.

Table 2 — SNW-3 bit definitions

Bit	Description
0	START bit
1	DEGRADED bit
2	CURRENT TX SSC bit
3	TX SSC TYPE bit
4 to 7	Reserved
Supported settings	
8	G1 WITH SSC SUPPORTED bit
9	G2 SUPPORTED bit
10	G2 WITH SSC SUPPORTED bit
11	G2 SUPPORTED bit
12	G3 WITH SSC SUPPORTED bit
13	G3 SUPPORTED bit
14 to 63	Reserved
64 to 71	CRC field
[a] x means don't care (i.e., one or zero)	

The START bit shall be set to one. The phy's receiver shall use this bit to establish the timing for the subsequent bits.

A DEGRADED bit set to one indicates that the phy is performing a link reset sequence after encountering a phy reset problem. A DEGRADED bit set to zero indicates that the phy is not performing a link reset sequence after encountering a phy reset problem.

A CURRENT TX SSC bit set to one indicates that the phy's transmitter is currently transmitting with SSC. A CURRENT TX SSC bit set to zero indicates that the phy's transmitter is not currently transmitting with SSC.

NOTE 1 - This bit is informative, and is not expected to be used by a phy's receiver.

A TX SSC TYPE bit set to one indicates that the phy's transmitter uses center-spreading SSC when SSC is enabled. A TX SSC TYPE bit set to zero indicates that the phy's transmitter uses down-spreading SSC when SSC is enabled, or that the phy does not support SSC.

NOTE 2 - The phy receiver may use the TX SSC TYPE bit to optimize its CDR circuitry. This bit indicates the type of SSC used when attached to a SAS phy or an expander phy; if a phy supports center-spreading when attached to a SAS phy or an expander phy and down-spreading when attached to a SATA phy, it sets the TX SSC TYPE bit to one.

The G<GENERATION NUMBER> WITH SSC SUPPORTED bits and G<GENERATION NUMBER> WITH SSC SUPPORTED bits indicate the physical link rates and SSC options the phy is attempting to negotiate.

A G1 WITH SSC SUPPORTED bit set to one indicates that the phy supports G1 (i.e., 1,5 Gbps) with SSC. A G1 WITH SSC SUPPORTED bit set to zero indicates that the phy does not support G1 with SSC.

A G1 SUPPORTED bit set to one indicates that the phy supports G1 without SSC. A G1 SUPPORTED bit set to zero indicates that the phy does not support G1 without SSC.

A G2 WITH SSC SUPPORTED bit set to one indicates that the phy supports G2 (i.e., 3 Gbps) with SSC. A G2 WITH SSC SUPPORTED bit set to zero indicates that the phy does not support G2 with SSC.

A G2 SUPPORTED bit set to one indicates that the phy supports G2 with SSC. A G2 SUPPORTED bit set to zero indicates that the phy does not support G2 without SSC.

A G3 WITH SSC SUPPORTED bit set to one indicates that the phy supports G3 (i.e., 6 Gbps) with SSC. A G3 WITH SSC SUPPORTED bit set to zero indicates that the phy does not support G3 with SSC.

A G3 SUPPORTED bit set to one indicates that the phy supports G3 with SSC. A G3 SUPPORTED bit set to zero indicates that the phy does not support G3 without SSC.

The CRC field contains an 8-bit CRC of the SNW-3 information bits.

Editor's Note 1: CRC-8 polynomials that are popular include: x8 + x2 + x + 1 (ATM), x8 +x7 + x3 + x2 + 1 (CCITT), and x8 + x7 + x6 + x4 + x2 + 1

Editor's Note 2: Other related changes to eventually make: Add the incoming values to the SMP DISCOVER response (including all the reserved bits). Add controls for the outgoing values to the SMP PHY CONTROL request (which currently has programmable minimum and maximum link rates, but does not have SSC controls). Add the outgoing values to the DISCOVER response so software can figure out why the the phy negotiated to a degraded mode.