Spread Spectrum Clocking Considerations
T10/06-192r0

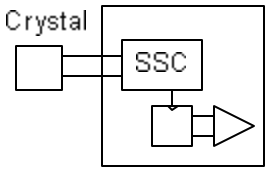
April 6, 2006

ADS

Infineon

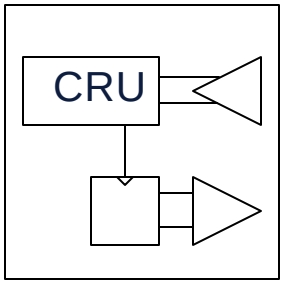
Never stop thinking

Spread Spectrum Clock Considerations

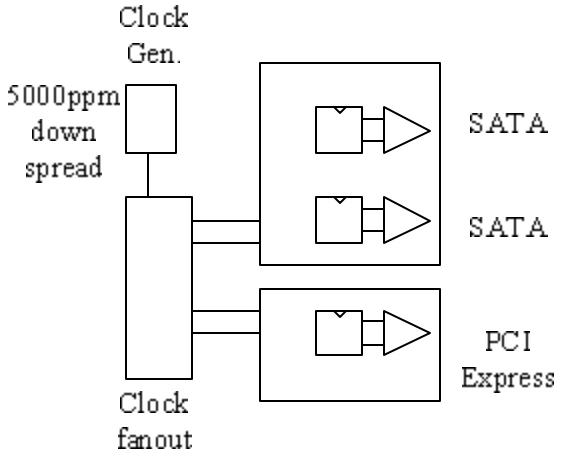


SSC internally generated

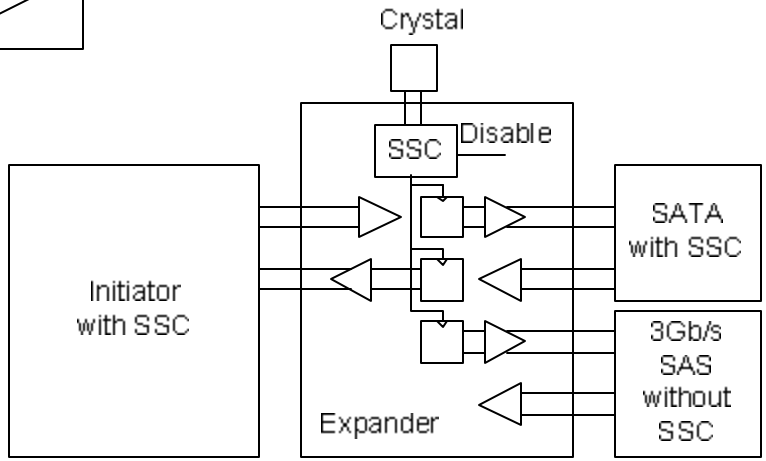
SATA allows Tx clock from Rx clock recovery for device.



SSC input will generate SSC out, no SSC in then no SSC out.



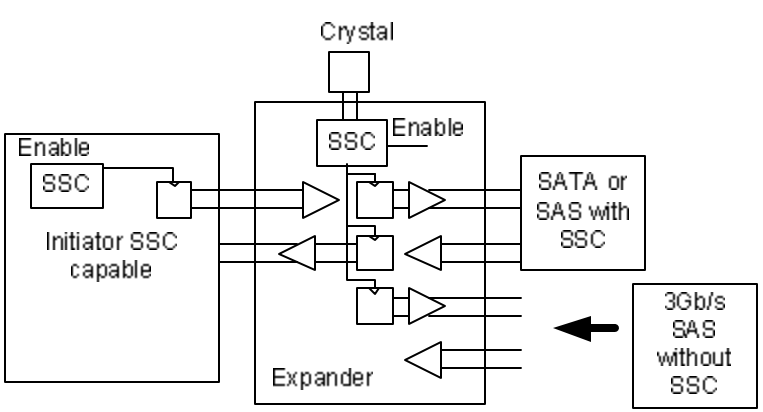
Distributed system clock

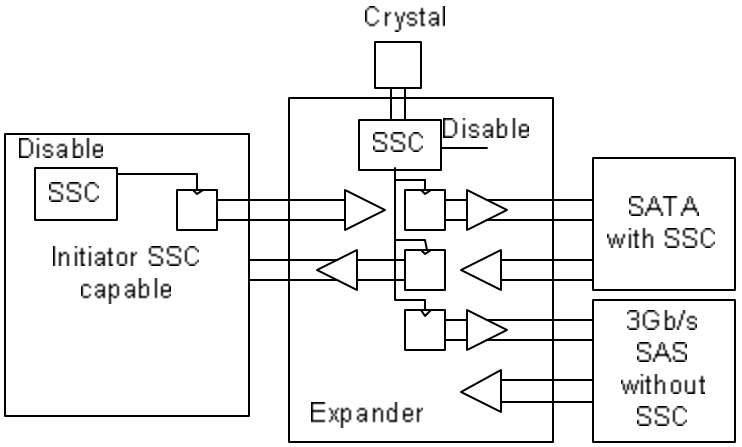


Expander with common clock.

Spread Spectrum Clock Considerations

All or nothing issue: If an expander expects to use a common clock with SSC enabled or disabled and legacy SAS can not tolerate SSC then entire domain must disable SSC when a legacy device is detected.



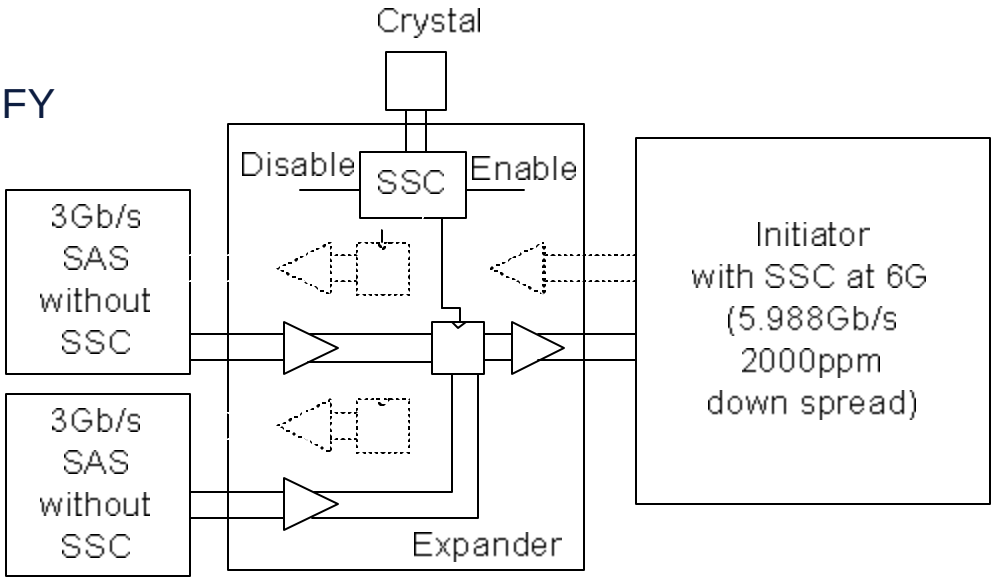


Expander with common clock.
All or none for SSC Tx. How to enable/disable?

Spread Spectrum Clock Considerations

Interleaving issue: If 6Gb/s is down spread.
The number of ALIGN primitives in the legacy SAS does not allow enough elasticity buffer management.

Legacy ALIGN and/or NOTIFY insertion rate is 2 per 4096.



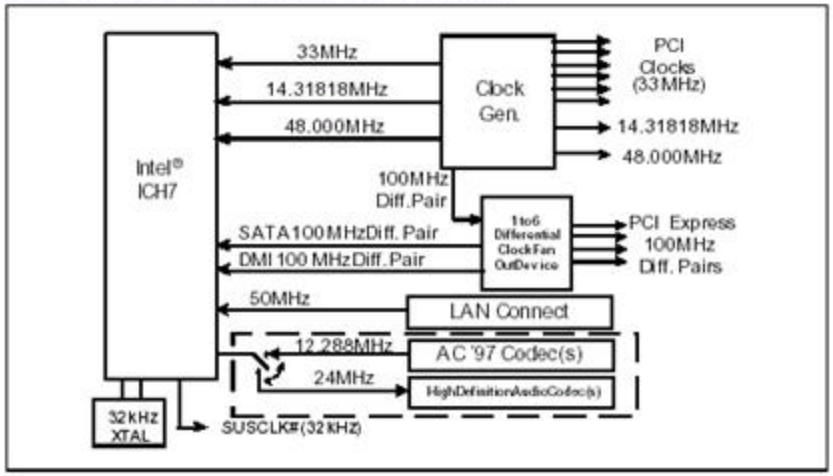
In at 2 * 3Gb/s = 6Gb/s out at 5.988Gb/s with 2000ppm down spread.

Buffer the difference?

Clock Generator is common between SATA & PCI Express. Spread Spectrum Clocking is 5000ppm down spread.

Intel© ICH7 and System Clock Domains

Figure 4-1. Desktop Only Conceptual System Clock Diagram



ftp://download.intel.com/design/chipsets/datashts/30701302.pdf
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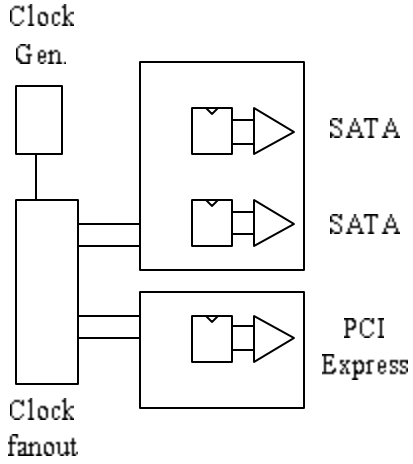

SSC on system clock.
SATA will likely have 5000ppm down spread at 6Gb/s due to this architecture and feedback from SATA phy call April 5th