Spread Spectrum Clocking Considerations
T10/06-192r0

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ADS
Spread Spectrum Clock Considerations

SSC input will generate SSC out, no SSC in then no SSC out.

SATA allows Tx clock from Rx clock recovery for device.

SSC internally generated

Expander with common clock.

Distributed system clock
Spread Spectrum Clock Considerations

All or nothing issue: If an expander expects to use a common clock with SSC enabled or disabled and legacy SAS cannot tolerate SSC then the entire domain must disable SSC when a legacy device is detected.

Expander with common clock. All or none for SSC Tx. How to enable/disable?
Interleaving issue: If 6Gb/s is down spread. The number of ALIGN primitives in the legacy SAS does not allow enough elasticity buffer management.

Legacy ALIGN and/or NOTIFY insertion rate is 2 per 4096.


Buffer the difference?
Clock Generator is common between SATA & PCI Express. Spread Spectrum Clocking is 5000ppm down spread.

SSC on system clock. SATA will likely have 5000ppm down spread at 6Gb/s due to this architecture and feedback from SATA phy call April 5th.