

Current specification requirements:

Initiator and expander that connect to SATA shall tolerate.

Not a device or non-SATA requirement. (Backwards compatibility consideration.)

SATA chose 30kHz – 33kHz to keep above the audible range.

5000 ppm was used for SATA 1.5Gbps. Could be 1250 or 1000 ppm for 6 Gbps since it is proportional to frequency? Barry will provide additional data on SATA open box at 3Gbps and various ppm values at the March PHY working group meeting.

Most implementations have the capability to switch SSC on and off so it should not be an issue to turn off for slower speeds and to have off during training/OOB.

BUT:

Is SSC off during OOB and speed negotiation?

What if two different speeds were used in the same device, initiator, or expander? This may cause the data clock issues if a common clock is used for multiple ports and they are running at different rates where some of the rates cannot include SSC.

How is the SSC switched on and off?

Will a drive, expander, or initiator at 3Gbps that is SAS only accept SSC at 3Gbps?

Require turning off to measure jitter? In most cases SSC adds some amount of jitter in addition to what is already there.

SSC appears to be an “all or none” proposition unless the clock design in the silicon allows differentiation. Need feedback from expander designers.

Does capability to turn on and off introduce an EMI compliance issue, especially if a 1.5 or 3G device present would cause it to be turned off for all devices on a given expander?

How to handle aggregation? Data stream coming in with no SSC versus going out with SSC would not have enough aligns to allow the output to be slowed by SSC. This may be able to be controlled by the SAS credits for flow management, but how complicated is the control scheme to implement?