VITESSE

06-053r0 Roadmap to SAS-2 Physical Layer Specification

Serial Attached SCSI

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SAS-2 PHY Working Group

January 9, 2006

YOUR PARTNER FOR SUCCESS

Proposed Road Map

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- Establish General Link Assumptions & Goals
  - Based on Market need (STA) and technical contributions to date
- Compare to some other Relevant Specifications
  - See 06-011r1 & May 2005 Meeting Post
- Propose a set of Electrical Specifications & Compliance test for discussion
  - Encourage Counter Proposals or Proposal Modifications (started in 06-011r1)
  - Form a consensus on what will be specified, <<= This is the focus of this presentation
- Identify Specifications & Compliance Test which will need additional work and research
  - Recruit Technical Contributors
- Draft Document

Outline

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- Specification Goal
- Specification Usage Models
  - Application Based Perspective
- Proposed Outline of Specification
- Specification Usage Models (Continued)
  - Design and Test Perspective
- First Pass Target Specification Numbers
- Open Item & Discussion

Specification Goal

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Draft a Specification which will Meet All Users' Requirements

1. System Users (End Users)
   - Meet Objectives set by STA
   - Provide a Robust Interface
   - Support Interoperability at the System Level
2. System Designer (Server & Storage System Builders)
   - Enable System Designers to Design and Predict if the Design will be Compliant
   - Enable System Designers to Test a System and Determine if it is Compliant
   - Support High Port-Count Applications (Low Power/ Small Phy.),
   - Support Interoperability at the Component Level (Drives, Cables…)
3. Component Supplier (Drives, ASIC, Connector & Cable Vendors)
   - Provide Compliance Test which Enable Component Supplier to Test Product

SAS-2 Specification Usage Models To Consider

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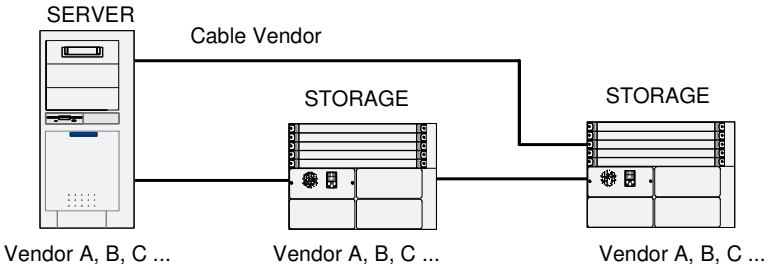
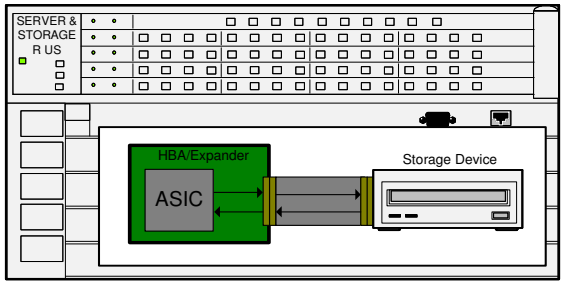
1. System User's Perspective
   - Standard Interfaces Chassis-to-Chassis or Intra-Chassis
   - Interoperability of different Vendors Required

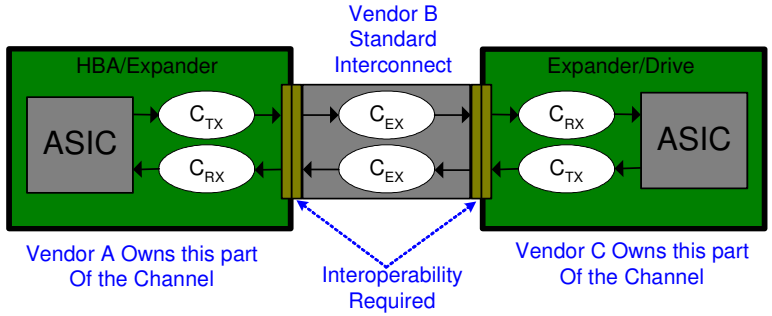
User Models



or



Channel Model Has 3 Major Sections, two connector interfaces



C_{EX} = External Channel
C_{TX} = Tx Channel
C_{RX} = Rx Channel
$C = C_{TX}C_{EX}C_{RX}$ = Composite Channel

C_{TX} & C_{RX} includes Mated Connector

SAS-2 Specification Usage Models To Consider

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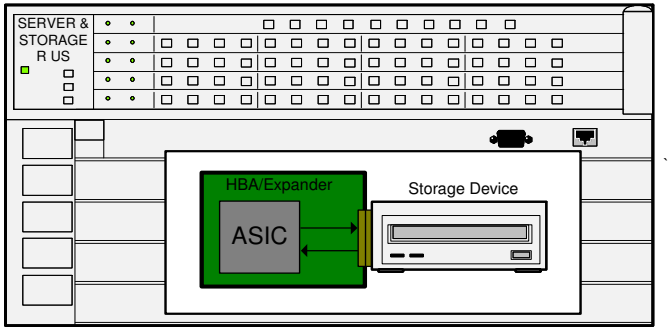
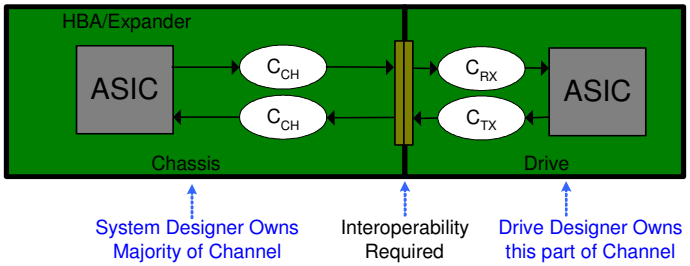
2. System Designers' Perspective (1 of 2)

- Single Standard Interface, Intra-Chassis Multi-Vendor

User Models



Channel Model has two Major Sections, one connector interfaces



C_{CH} = Chassis Channel
$C_1 = C_{CH}C_{RX}$ = Composite Rx Channel
$C_2 = C_{CH}C_{TX}$ = Composite Tx Channel

C_{TX} & C_{RX} includes Mated Connector

SAS-2 Specification Usage Models To Consider

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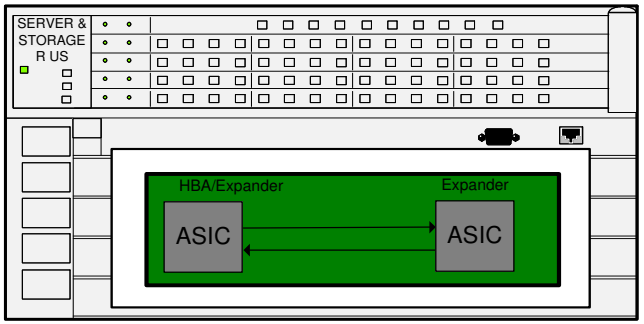
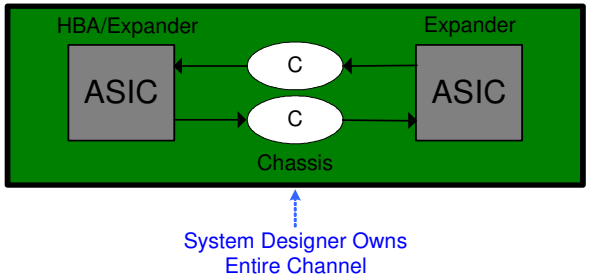
3. System Designers' Perspective (2 of 2)

- No Standard Interfaces
- Intra-Chassis Self Contained, System Designer Owns Entire Channel
- PCB, connectors, backplanes, cables ….

User Models



Channel Model is a Single Section, zero connector interfaces



SAS-2 Specification Proposal (Modified CEI)

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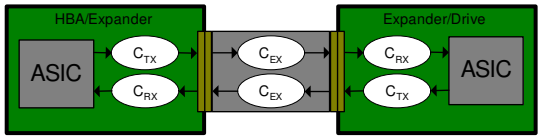
1. **Specify a Reference Transmitter based on Target Channels**
   - Swing, De-emphasis, jitter, Output Impendence ….
   - ASIC Designed to Exceed the Reference Transmitter Specification
2. **Specify a Reference Receiver based on Target Channels**
   - # DFE taps (Design must be as good as, not defining the implementation)
   - Return loss, Jitter tolerance ….
   - ASIC Designed to Exceed the Reference Receiver Specification

? Why Not just Use CEI Standard ?

1. Does Not Support Connector Interfaces
2. Unbounded Receiver Compliance Testing
3. 8B/10B Encoding
4. Reference Tx & Rx should match SAS Channel

3. **Specify a Reference ASIC to Standard Interface Channel based on Current Design Practices**
   - Assumed to be Small Part of the Worst Case Channel
   - C_{TX}, C_{RX} (Based on T11 work, T11/05-346v1?)



4. **Channel Compliance Based on Above & Target BER**
   - Estimate Channel Performance via Simulation Using Predicted or Measured S-parameters of the Composite Channel.
   - Use the Composite Channel Model & StatEye Methodologies or other Communication Channels Simulation Methods.
   - Analysis Tool or Algorithm Need Not be Specified.
5. **Specify a Standard Connector-Based Transmit Eye Mask and De-Emphasis Test**
   - Based on Reference Transmitter and C_{TX}
6. **Specify Receiver Compliance Test**
   - Emulate Reference Transmitter, Channel and C_{RX}
   - Emulate zero length and Worst Case Channels
   - Specify a Jitter Tolerance Mask and Test Methodology
   - Test With Specified a Cross-talk budget

Look at Users' Application of the Specification

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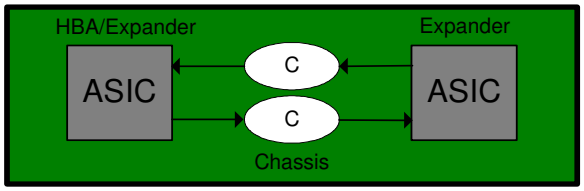
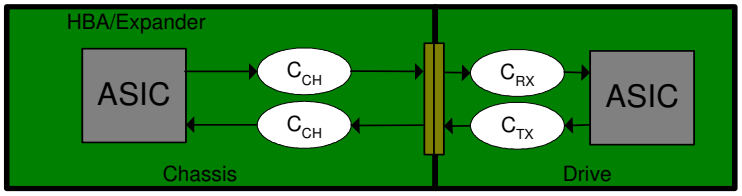
1. Self-Contained Zero-Connector system
2. One-Connector System

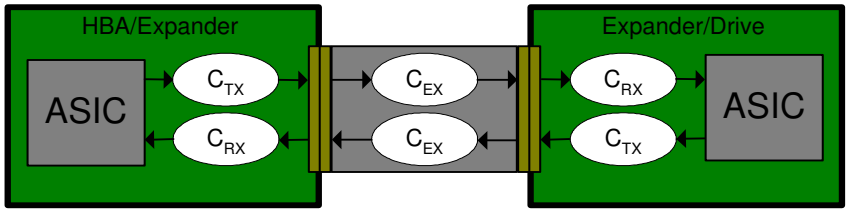
   Storage System w/ Drive Bays
3. Design with one Tx Standard Interface

   Storage Device or External Interface
4. Tx ASIC Design
5. Design with one Rx Standard Interface

   Storage Device or External Interface
6. Rx ASIC Design
7. External Cable







SAS-2 Specification Usage Models To Consider (Design and Test Perspective)

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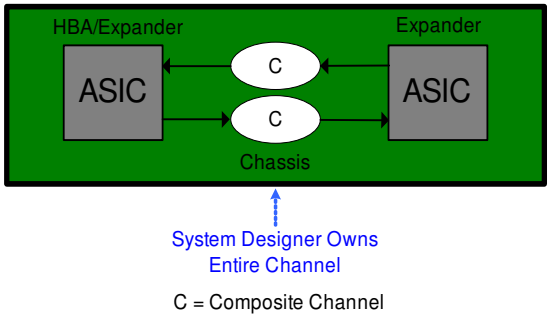
Self-Contained System Design

- Common SAS Applications



System Designer Estimate Channel Compliance via Simulation

- Assume the Reference Transmitter and Receiver
- Uses Predicted or Measured S-parameters of the Channel,C, C_{RX} & C_{TX}
- StatEye Methodologies or other Communication Channels Simulation Methods.

SAS-2 Specification Usage Models To Consider (Design and Test Perspective)

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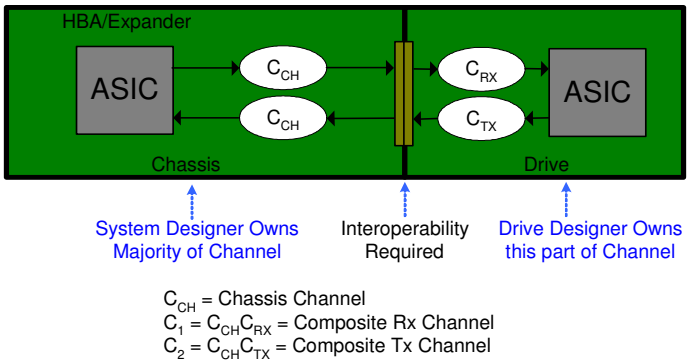
- One Connector System Design and Test Perspective



C_{CH} = Chassis Channel
$C_1 = C_{CH}C_{RX}$ = Composite Rx Channel
$C_2 = C_{CH}C_{TX}$ = Composite Tx Channel

- System Designer Estimate Channel Compliance via Simulation
  - Assume the Reference Transmitter and Receiver
  - Uses Predicted or Measured S-parameters of the Channel, C_{CH}, C_{TX}& C_{RX}
  - StatEye Methodologies or other Communication Channels Simulation Methods.

SAS-2 Specification Usage Models To Consider (Design and Test Perspective)

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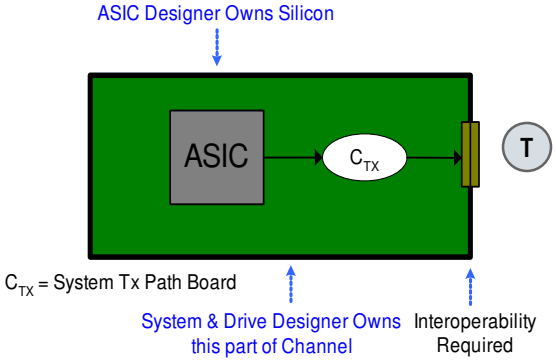
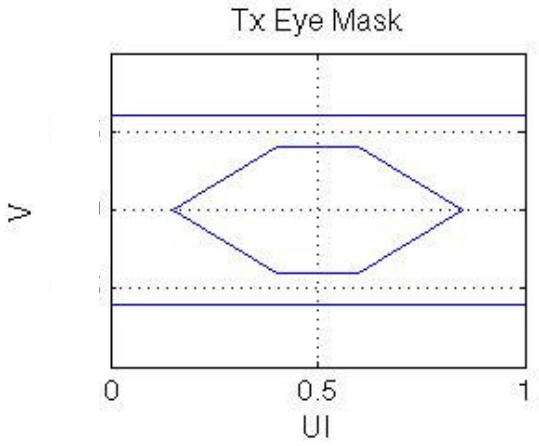
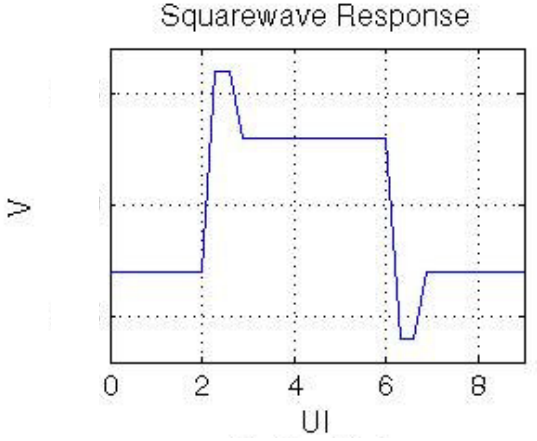
- External Transmit Interface Design and Test Perspective
  - Servers, Storage Boxes, & Storage Interface
  - ASIC and Board Design Determine Eye at Interoperability Point
- System Designer Test Compliance at the Connector Interface "T"
  - Measure Salient Specification at the Connector
    - Eye mask w/o DE, Output Impedance, De-Emphasis test
  - Specifications Based on C_{TX} and Reference Transmitter







SAS-2 Specification Usage Models To Consider (Design and Test Perspective)

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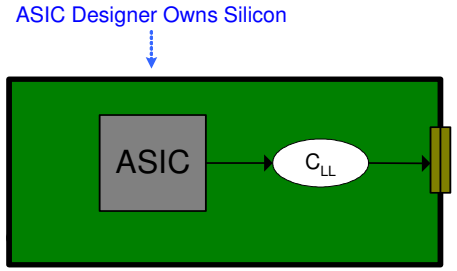
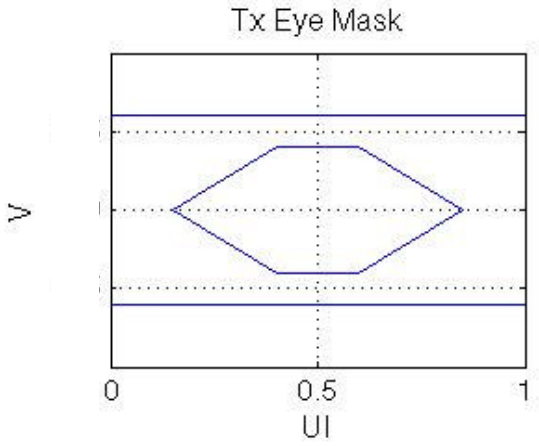
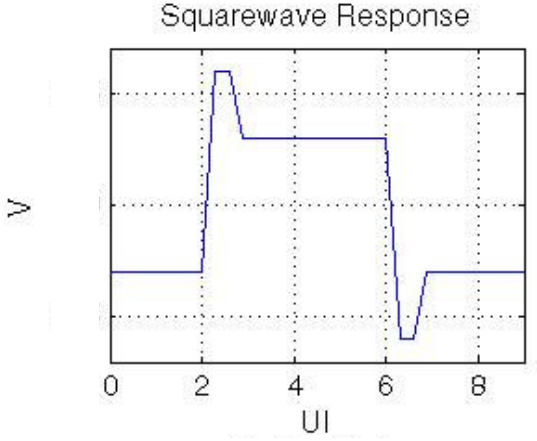
- ASIC Designer test Compliance at the ASIC Pin
  - Specification is the Reference Transmitter Specification
  - Measure Salient Specification at ASIC Pin by De-Embedding the Test Fixture
  - Eye mask, Output Impedance, De-Emphasis test



ASIC Designer Want to Characterize a Part for Compliance

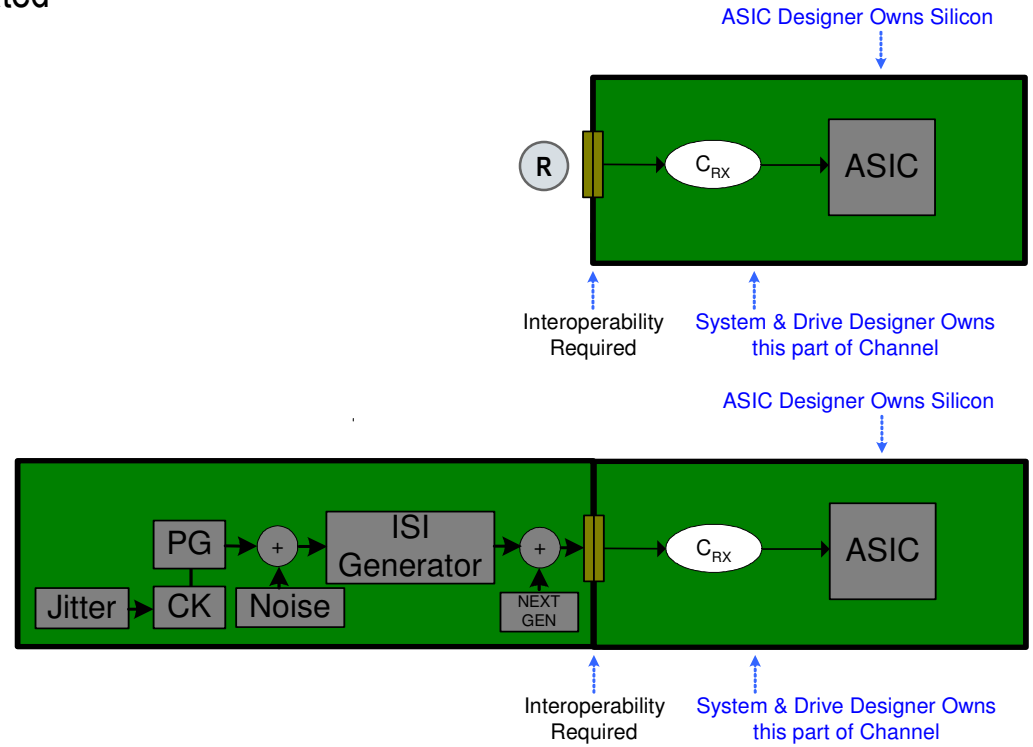




SAS-2 Specification Usage Models To Consider (Design and Test Perspective)

VITESSE

- External Receive Interface Design and Test Perspective
  - Servers, Storage Boxes, & Storage Interface
  - External Channel Determines Eye at Interoperability Point
- System Designer Test Compliance at the Connector Interface "R"
  - ISI Generator Emulates Reference Transmitter, C_{TX}, Jitter, Channels of interest
  - Test Channels Emulated
    - Zero length
    - Worst Case
    - Others



SAS-2 Specification Usage Models To Consider (Design and Test Perspective)

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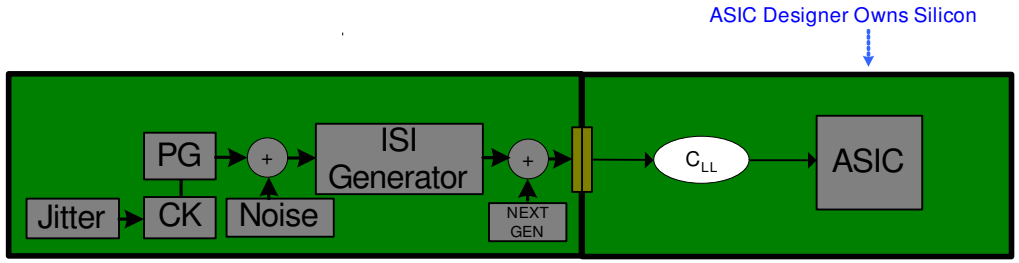
Receive ASIC Design and Test Perspective

- Test Receiver with low-loss test fixture w/o C_{RX}
- ISI Generator Emulates Reference Transmitter, C_{TX}, C_{RX}, Jitter, Channels of interest
- Test Channels Emulated
  - Zero length
  - Worst Case based on S-Parameter Data base
  - Other



SAS-2 Receiver Compliance Test Hardware

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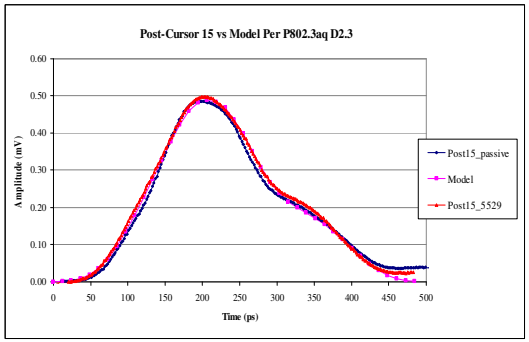
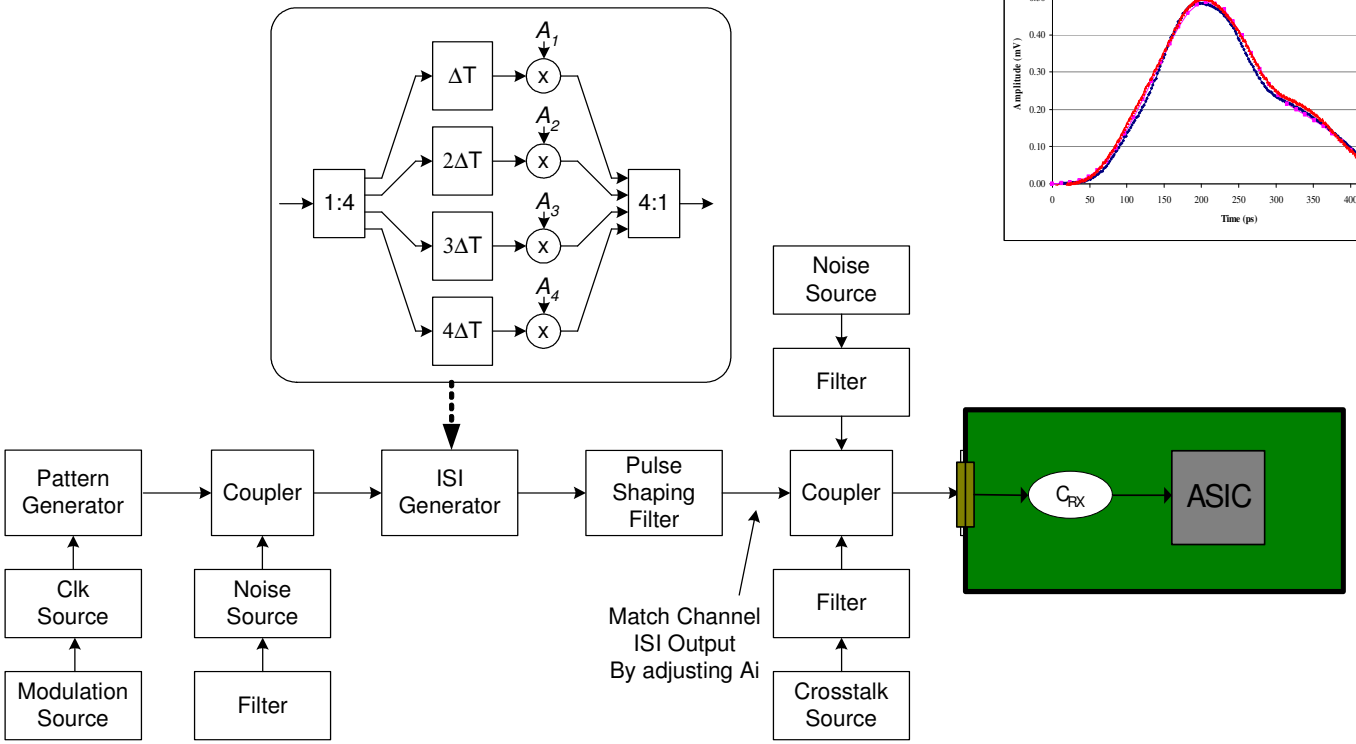
- Receiver Compliance w/ Jitter, Crosstalk and Interference (same as OIF-CEI, & 10GBase-KR)
- Standardize Test Setup based on 10GBase-LRM ISI Generator
  - Generate ISI coefficients for channels of Interest
  - Calibrate and Test Through Mated Connector
  - Emulate Tx DE, C_{TX} & C

10GbE MMF Example





SAS-2 Receiver Compliance Test Hardware

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- Potential Rx Compliance Test Channels
  - Zero Length
  - Worst Case ISI (based on PIE-D) with low Attenuation (Intra Chassis)
  - Worst Case ISI (based on PIE-D) with High Attenuation (Long External Cable)
  - Others ?
- IEEE References on ISI Generator
  - http://www.ieee802.org/3/10GMMFSG/public/mar04/witt_1_0304.pdf
  - http://www.ieee802.org/3/aq/public/jan05/popescu_1_0105.pdf
  - http://www.ieee802.org/3/aq/public/mar05/mcvey_1_0305.pdf
  - http://www.ieee802.org/3/aq/public/sep05/mcvey_1_0905.pdf
  - Many more just look for TP3 in title

SAS-2 Specification Usage Models To Consider (Design and Test Perspective)

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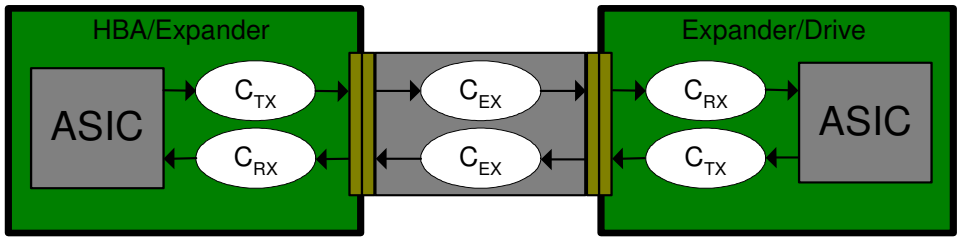
- Cable Connector Design and Test Perspective
- Potential Issue w/ Connector Allocation
  - C_{TX} and C_{RX} are through matted connector
  - C_{EX} is based on De-Embedded Connectors
- System Designer Estimate Channel Compliance via Simulation
  - Assume the Reference Transmitter and Receiver
  - Uses Predicted or Measured S-parameters of the Channel, C_{EX}, C_{TX}& C_{RX}
  - StatEye Methodologies or other Communication Channels Simulation Methods.



SAS-2 Specification First Pass Numbers

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Reference Transmitter

	Typical SAS-1		SAS-2	Units
General				
Bit Rate	1.5 +/- (a)	3 +/- (a)	6 +/- (a)	Gbps
BER	1.00E-12	1.00E-12	1.00E-15	
Transmitter				
Differential Voltage (pk-pk)	1600	1600	800 -> 1200	mV
Min. Transition Time (20%-80%)	67	67	50	ps
Max Transition Time (20%-80%)	273	137	90	ps
Output Impedance	60 min/ 115 max	60 min/ 115 max	60 min/ 115 max	ohm
Output Impedance Mismatch	5	5	5	ohm
Common Mode Impedance	15 min/ 40 max	15 min/ 40 max	15 min/ 40 max	ohm
Max. Intra-Pair Skew	20	15	15	ps
Random Jitter	0.2	0.2	0.15	UI
Deterministic Jitter	0.35	0.35	0.15	UI
Total Jitter	0.55	0.55	0.3	UI
# De-Emphasis	N.A.	N.A.	2	Taps
Min De-Emphasis	N.A.	N.A.	0	dB
Max De-Emphasis	N.A.	N.A.	6	dB

SAS-2 Specification First Pass Numbers

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- Reference Receiver

	Typical SAS-1		SAS-2	Units
Receiver				
Reference Rx # DFE Taps	N.A.	N.A.	TBD	taps
Differential Impedance	100+/- 15%	100+/- 15%	100+/- 15%	ohm
Differential Impedance Mismatch	5	5	5	ohm
Common Mode Impedance	20 min/ 40 max	20 min/ 40 max	20 min/ 40 max	ohm
Common-Mode Tolerance (2-200MHz)	150	150	150	mV
Max Operational Input Voltage	1600	1600	1200	mV
Max Non-Operational Input Voltage	2000	2000	2000	mV
Differential Return Loss	N.A.	N.A.	TBD 10GBase-KR?	dB

Notes:

1) Receiver implementation is not limited to DFE architecture, however, its' equalization capability must at least be equivalent to the reference receiver.

2) Complexity of the Reference Should be adequate SAS Channel library and SAS-2 external cable reach objective.

SAS-2 Specification TBD Numbers

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- External Interface Reference Transmit Path Model (C_{TX})
  - Does the T11 Model Match the SAS-2 Application
  - Is a Single Model Adequate or do we Need Two or More?
    - Short trace Model w/ SAS connector for model for Drives
    - Long Trace Model w/ External Connector for External Cable Connections
- External Interface Reference Receive Path Model (C_{TX})
  - Same as Tx Path
- Jitter Tolerance Mask and Test Methodology
  - Need Proposals
- Cross-Talk Specification
  - Need Proposals
- Others?

Summary

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- A Modified version of the OIF-CEI Specification is Proposed for SAS-2.
  - Extends the CEI approach to support Standardized interfaces
  - Narrows the Receiver Compliance Test to Finite Number of Test
- The Proposal Attempts to Address the Needs of all Users of the Physical Layer Specification.