

# Comparison of Equalization Schemes for 6Gbps SAS Channels

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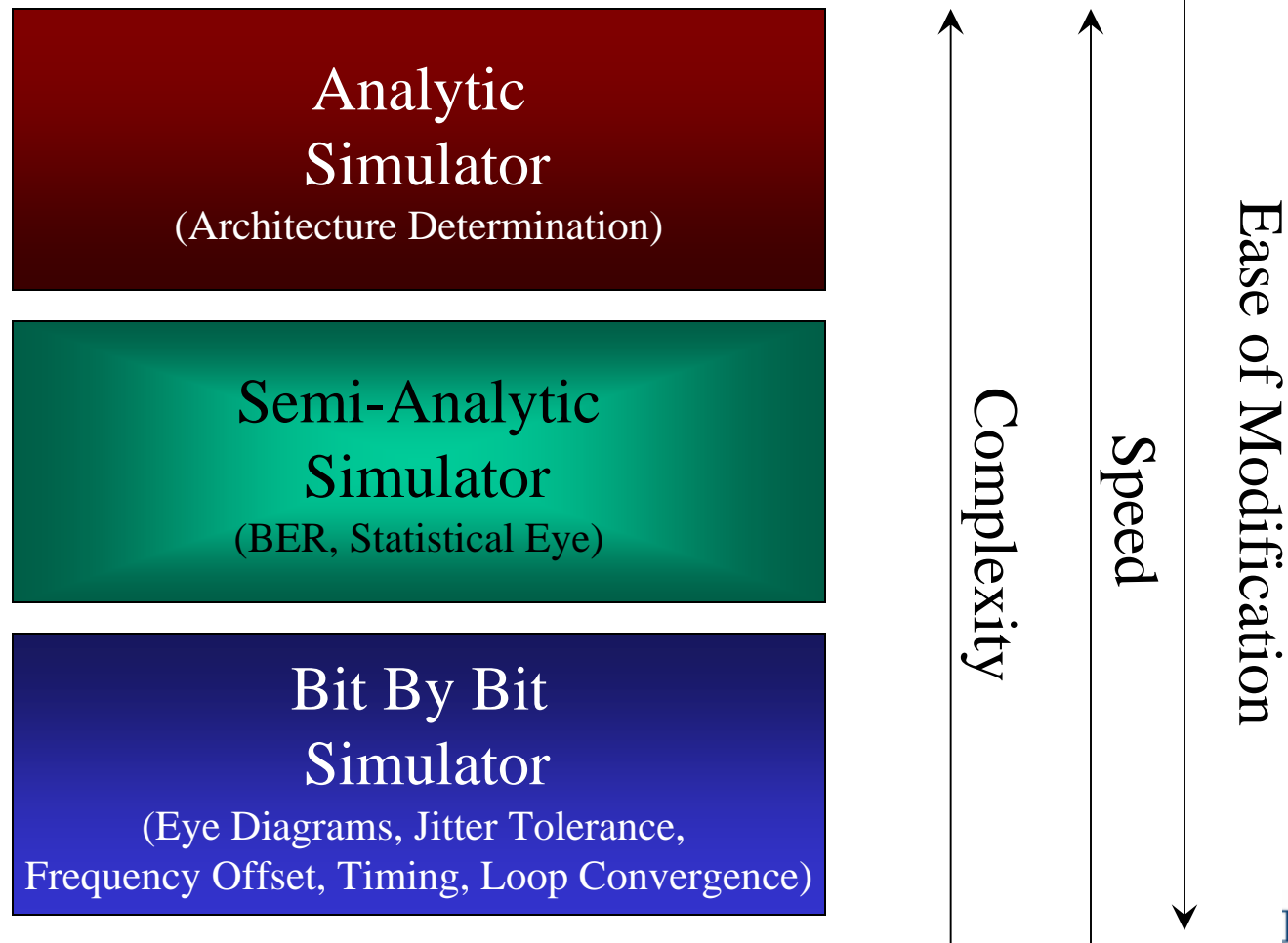
# Introduction

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- Review of simulator and parameters
- Overview of channels
- Presentation of results

# Simulator Review

# Three System Model Approach



# Analytic Model

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- Includes
  - Intersymbol Interference
  - Tx Jitter
  - Electronics (White) Noise
  - Crosstalk
- Does Not Include
  - Receiver Sensitivity
  - Duty Cycle Distortion
  - Other Sources of DJ

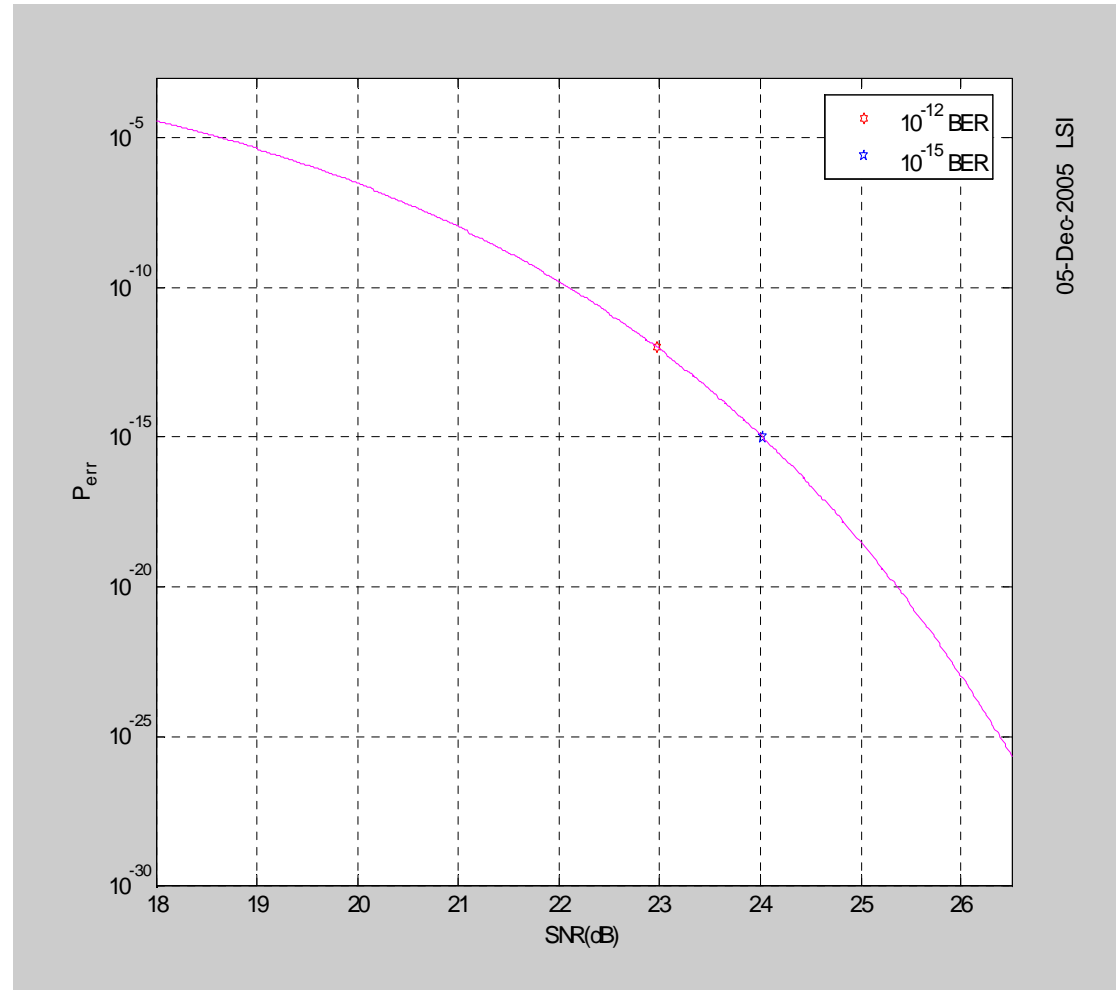
# Required SNR

## SNR Required at Slicer for $10^{-15}$ BER

$$SNR = \frac{d_{\min}^2}{\sigma^2}$$

$$Pr_{err} \approx \frac{1}{2} \operatorname{erfc} \left( \frac{\sqrt{SNR}}{2\sqrt{2}} \right)$$

- Approximately 24dB is required for an error rate of  $10^{-15}$



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# Overview of Simulations

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- Equalization architectures with a linear FIR feedforward (FF) filter in the TX, and a decision feedback (FB) equalizer in the Rx are compared.
- The number of taps in the feedforward and feedback equalizers are varied.
- The effect of one near-end crosstalk aggressor is considered.
- A simple RC model with pole at  $0.75 \times \text{baud rate}$  is used for the transmitter.
- Mellitz capacitor-like package model included on both transmitter and receiver.

# Parameters Used

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- Only DJ is from ISI
  - No DCD, PJ included
- $0.010UI \sigma$  RJ added
- Signal-To-Electronics Noise Ratio 45dB
- Crosstalk added as noted
- Ideal receiver sensitivity assumed

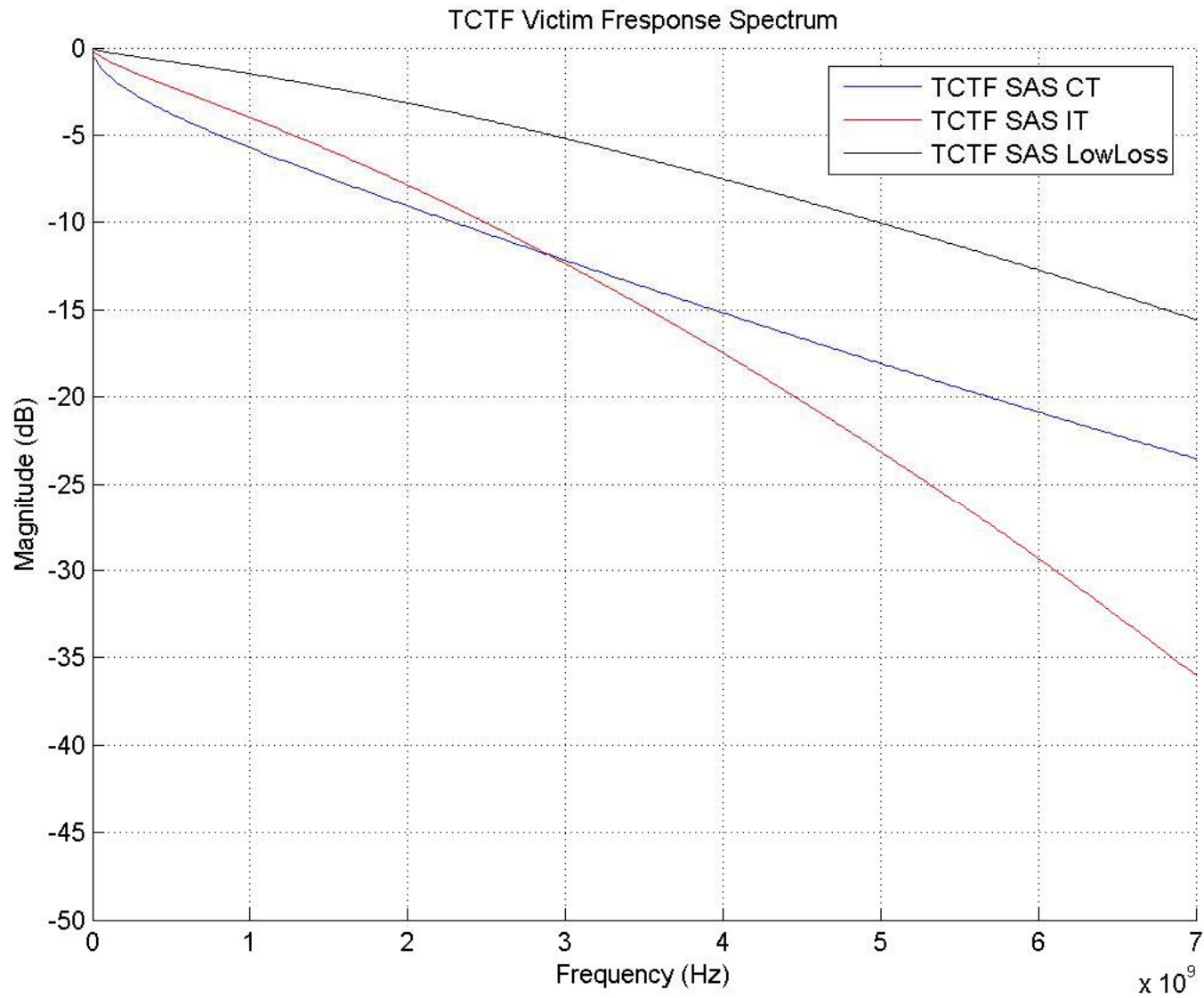


# Description of Results

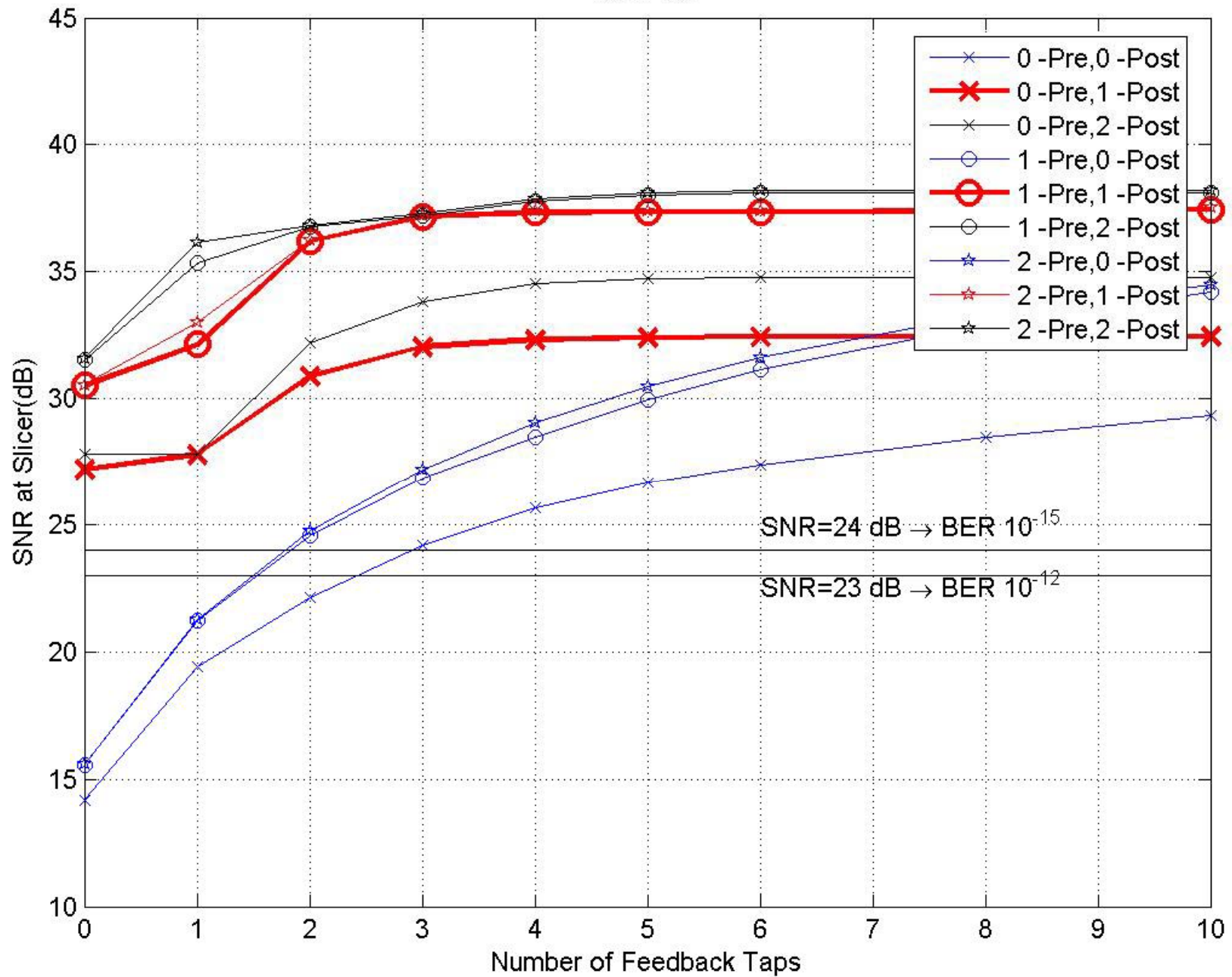
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- SNR at optimal sampling point is shown. No measurement of horizontal eye opening is presented.
- x-axis shows number of DFE taps used
- Each line represents a different number of feed-forward (FF) equalizer taps used in the TX
- Crosstalk is assumed to occur at the same frequency as the signal. The worst case crosstalk phase at the ideal sampling point is selected.
- All tap values are ideal.

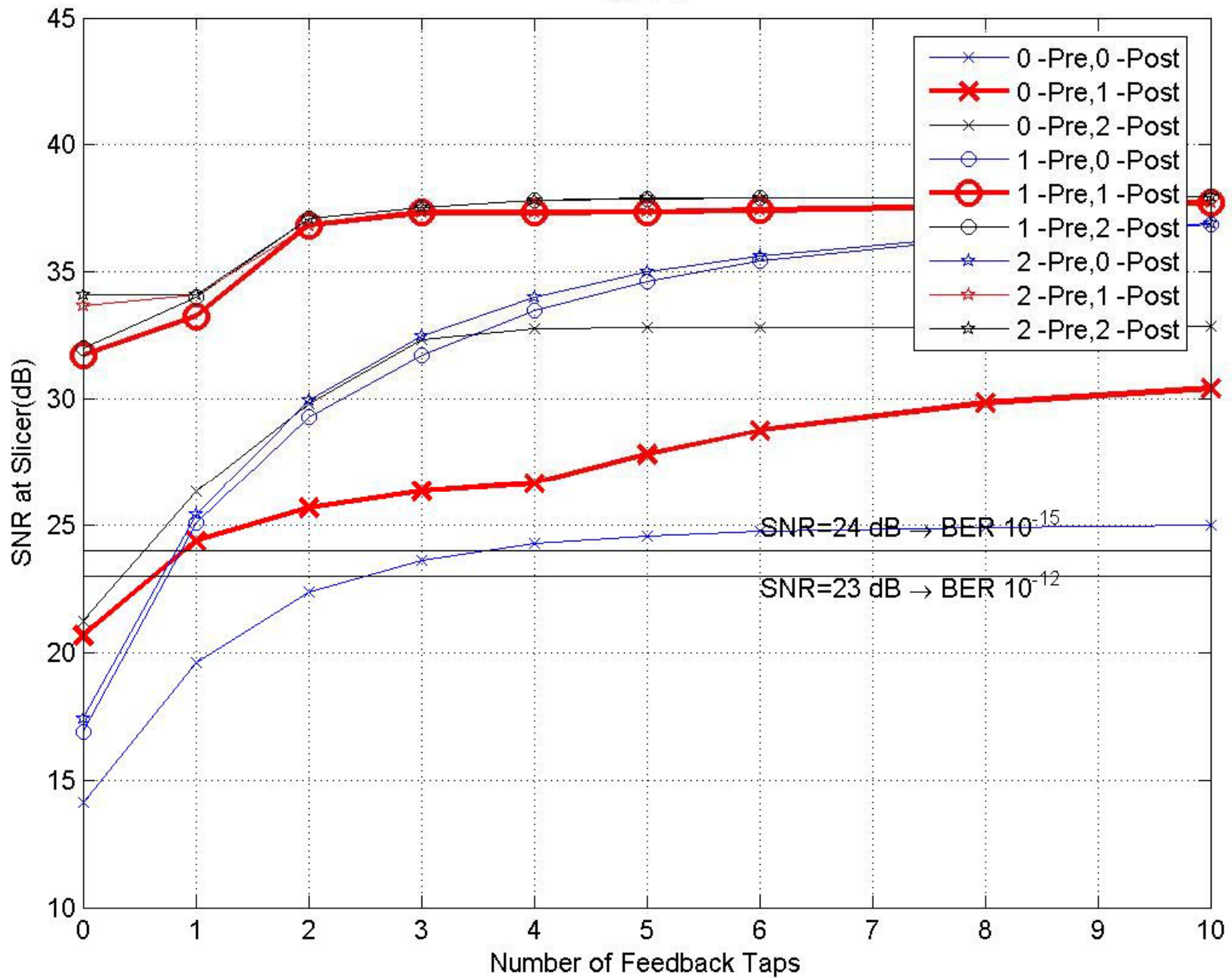
# TCTF Backplanes



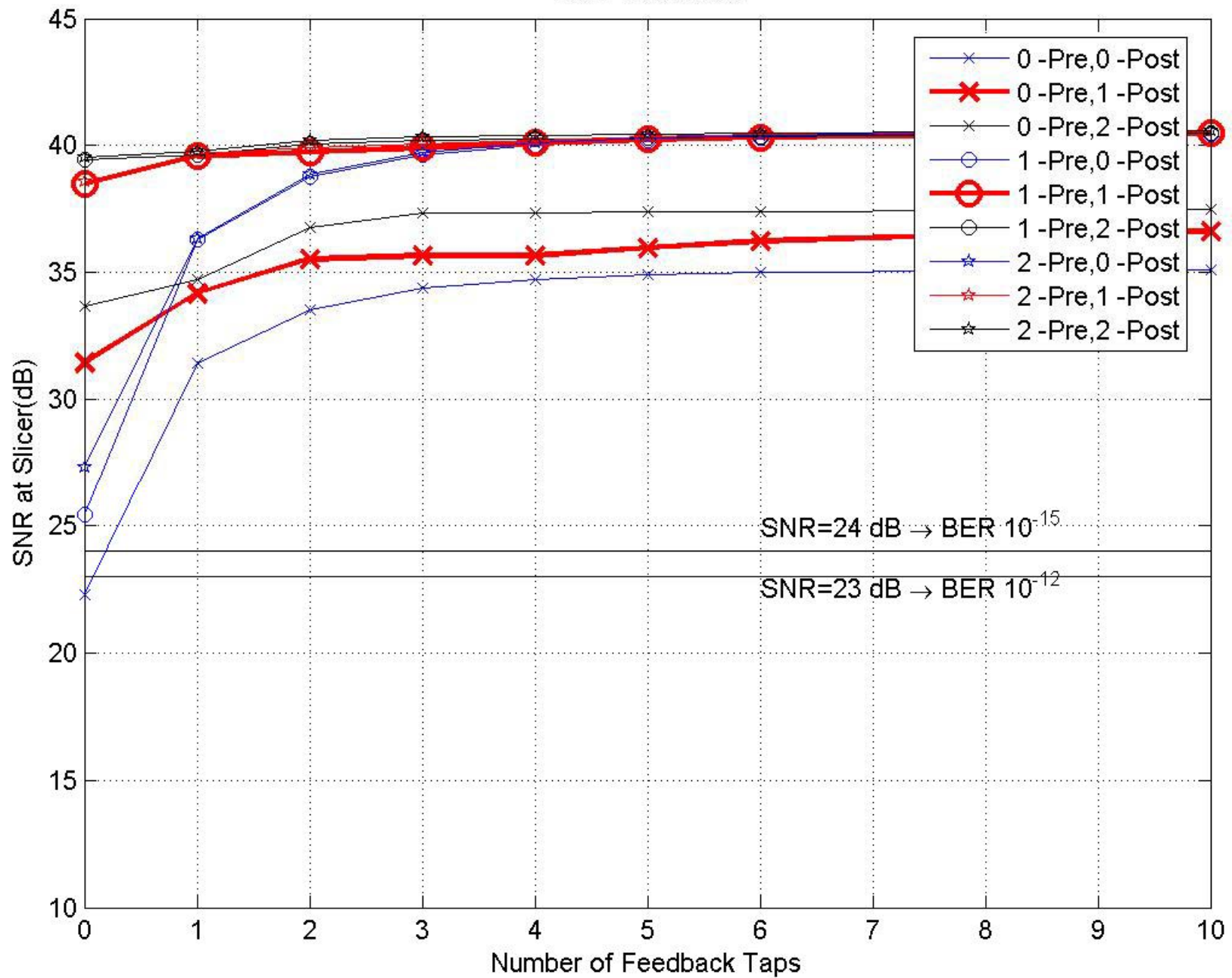
### TCTF CT



### TCTF IT



TCTF Low Loss



# Comparison to T10/05-428r0 Vertical Eye Opening

	6dB FFE No DFE	0dB FFE 5-tap DFE	# of taps for 1e-15 No xtalk	# of taps for 1e-15 HP15	# of taps for 1e-15 HP16	# of taps for 1e-15 HP17	# of taps for 1e-15 HP18	# of taps for 1e-15 HP19
HP01	0.10	0.20	1	1	2	1	8	30
HP02	0.10	0.22	1	2	2	1	6	20
HP03	0.12	0.25	5*	5*	5*	5*	8*	20*
HP04	0.13	0.25	4*	4*	4*	4*	6*	10*
HP05	0.11	0.22	1	1	2	1	4	20
HP06	0.09	0.18	1	1	2	1	20	1000
HP07	0.11	0.21	2	2	2	2	5	10
HP08	0.11	0.19	1	1	1	1	6	30
HP09	0.03	0.12	8					
HP10	Closed	0.11	4					
HP11	0.01	0.11	20					
HP12	0.13	0.22	0					
HP13	0.12	0.24	0					
HP14	0.09	0.21	1					

\* These channels were simulated at 6.25 Gb/s to cause worst case performance due to anti-resonance at ~3.125GHz. Simulated at 6.00 Gb/s, the required # of taps reduced to 2 for HP03 and 1 for HP04.



# Conclusions

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- Dell, Molex and TCTF require no DFE or 1-tap DFE
- HP Channels require more DFE compensation and the DFE requirements vary significantly depending on the victim and the aggressor. (See following detailed results)
- A reasonable compromise between chip area & power and the number of channels that can be supported is:
  - Reference TX: 1 post-cursor FFE tap (plus possibly one pre-cursor FFE tap)
  - Reference RX: 2 (or possibly 1) DFE taps
- Performance of channels is *strongly* a function of the frequency of significant anti-resonances