Comparison of Equalization Schemes for 6Gbps SAS Channels

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Introduction

- Review of simulator and parameters
- Overview of channels
- Presentation of results
Simulator Review
Three System Model Approach

Analytic Simulator
(Architecture Determination)

Semi-Analytic Simulator
(BER, Statistical Eye)

Bit By Bit Simulator
(Eye Diagrams, Jitter Tolerance, Frequency Offset, Timing, Loop Convergence)

Ease of Modification

Complexity

Speed
Analytic Model

• Includes
  – Intersymbol Interference
  – Tx Jitter
  – Electronics (White) Noise
  – Crosstalk

• Does Not Include
  – Receiver Sensitivity
  – Duty Cycle Distortion
  – Other Sources of DJ
Required SNR

SNR Required at Slicer for $10^{-15}$ BER

\[ \text{SNR} = \frac{d^2_{\text{min}}}{\sigma^2} \]

\[ \text{Pr}_{\text{err}} \approx \frac{1}{2} \text{erfc} \left( \frac{\sqrt{\text{SNR}}}{2\sqrt{2}} \right) \]

- Approximately 24dB is required for an error rate of $10^{-15}$
Overview of Simulations

- Equalization architectures with a linear FIR feedforward (FF) filter in the TX, and a decision feedback (FB) equalizer in the Rx are compared.
- The number of taps in the feedforward and feedback equalizers are varied.
- The effect of one near-end crosstalk aggressor is considered.
- A simple RC model with pole at 0.75*baud rate is used for the transmitter.
- Mellitz capacitor-like package model included on both transmitter and receiver.
Parameters Used

• Only DJ is from ISI
  – No DCD, PJ included
• 0.010UI $\sigma$ RJ added
• Signal-To-Electronics Noise Ratio 45dB
• Crosstalk added as noted
• Ideal receiver sensitivity assumed
Description of Results

- SNR at optimal sampling point is shown. No measurement of horizontal eye opening is presented.
- x-axis shows number of DFE taps used
- Each line represents a different number of feed-forward (FF) equalizer taps used in the TX
- Crosstalk is assumed to occur at the same frequency as the signal. The worst case crosstalk phase at the ideal sampling point is selected.
- All tap values are ideal.
TCTF Backplanes
## Comparison to T10/05-428r0 Vertical Eye Opening

<table>
<thead>
<tr>
<th>Channel</th>
<th>6dB FFE No DFE</th>
<th>0dB FFE 5-tap DFE</th>
<th># of taps for 1e-15 No xtalk</th>
<th># of taps for 1e-15 HP15</th>
<th># of taps for 1e-15 HP16</th>
<th># of taps for 1e-15 HP17</th>
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<td>5*</td>
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</table>

* These channels were simulated at 6.25 Gb/s to cause worst case performance due to anti-resonance at ~3.125GHz. Simulated at 6.00 Gb/s, the required # of taps reduced to 2 for HP03 and 1 for HP04.
Conclusions

• Dell, Molex and TCTF require no DFE or 1-tap DFE

• HP Channels require more DFE compensation and the DFE requirements vary significantly depending on the victim and the aggressor. (See following detailed results)

• A reasonable compromise between chip area & power and the number of channels that can be supported is:

  • Reference TX: 1post-cursor FFE tap (plus possibly one pre-cursor FFE tap)

  • Reference RX: 2 (or possibly 1) DFE taps

• Performance of channels is strongly a function of the frequency of significant anti-resonances