DFE Error Burst Analysis

Considerations for SAS 2.0

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T10/05-263r1

Introduction

- A contribution to the T10 SAS Ad hoc meeting (Houston – May 2005) states that a "CRC-32 can protect up to burst error of 3"
  - "IEEE 802.3ap 'Backplane Ethernet' Overview," from A. Ghiasi of Broadcom
- On this basis, strict limitation are proposed on the use of decision feedback equalizer (DFE) receivers
- Analysis in other standards bodies indicates that this view of the CRC-32 error burst capabilities is far too pessimistic
- This contribution analyzes the ability of the current CRC-32 to detect DFE-induced error bursts (including 8B/10B decoding effects)

Technical background - 1

- DFE receivers use multi-tap feedback in order to equalize channel frequency response without amplifying noise (especially noise due to crosstalk)
- Feedback can result in an incorrect equalizer decision propagating to create an error burst
- Any single bit error in an 8B/10B character can be converted to a burst due to the 8B/10B decoding process
- Thus, the combination of DFE with 8B/10B decoding can stretch the error burst
- An inherent property of a CRC-32 is that it can detect any burst error up to 32 bits in length

Technical background - 2

- Definition of a burst:
  - sequence of bits that begins with a bad bit and end with another bad bit
  - the intervening bits do not need to be bad
  - a burst straddling a packet boundary is split into 2 bursts
- Example : (B=bad bit, G=good bit)
  - BGGGBGB is a 7 bit burst
  - BBBBGGB is a 7 bit burst
  - BGGGGGB is also a 7 bit burst

OIF analysis

- The Optical Internetworking Forum (OIF) studied legacy backplanes at 5/6 Gb/s in Common Electrical Interface (CEI) Implementation Agreement (OIF-CEI-02.0)
  - OIF defines a CEI compliant channel as one that can be equalized to BER=10^{-15} using a 5-tap DFE
  - An analysis the OIF used in developing CEI showed that with a 5-tap DFE, the probability of a burst length longer than 7 bits is no greater than the natural occurrence of a second error due to noise
    - I.e., the maximum burst length from a 5-tap DFE is effectively 7 bits.
    - Analysis for DFE with up to 10 taps was contained in OIF2003.267.02 from J. Hamstra of Flextronics. (See appendix.)

OIF analysis for a 5-tap DFE (10^{-12} BER)

Burst	P = Prob Error	Gain in Prob due to DFE	Error rate due to DFE	
1	1	0	0	<- Error injection site
2	0.018559815	1.85068E+10	0.018559815	
3	1.92979E-12	1.924277649	9.26925E-13	
4	1.00286E-12	1	0	
5	1.15258E-10	114.9285952	1.14255E-10	
6	8.90643E-09	8.88099E+03	8.90542E-09	
7	1.20615E-12	1.202701207	2.03282E-13	
8	1.00286E-12	1	0	
9	1.00286E-12	1	0	
10	1.00286E-12	1	0	
11	1.00286E-12	1	0	

- Searched all tap configurations (tap weights from OIF, see Appendix). Longest burst when we have taps at positions 1, 4 and 5, none at 2 and 3
- DFE has measurable effect on Prob(error) only at burst length <= 7
- Spreadsheet here is data-mined from OIF2003.267.02

OIF analysis for a 5-tap DFE (10^{-15} BER)

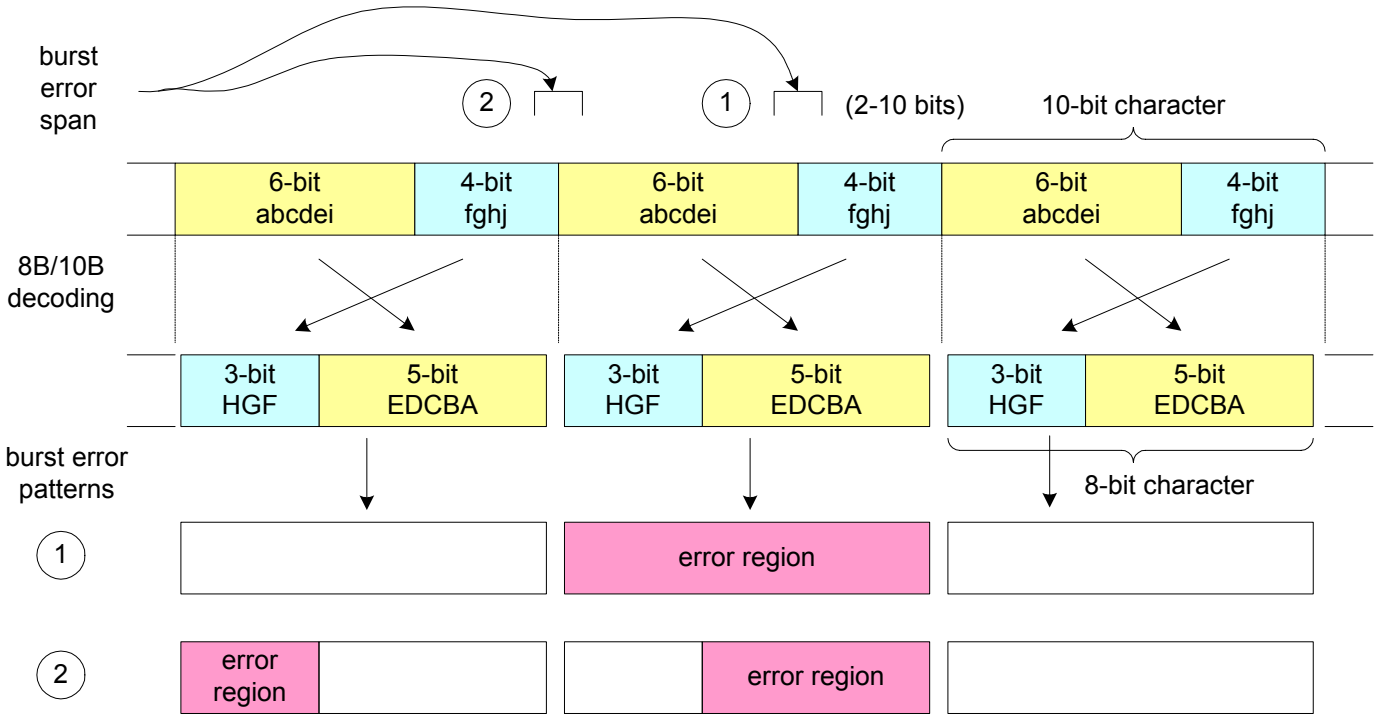
Burst	P = Prob Error	Gain in Prob due to DFE	Error rate due to DFE	
1	1	0	0	<- Error injection site
2	0.009358704	8.42957E+12	0.009358704	
3	1.66533E-15	1.5	5.55112E-16	
4	1.11022E-15	1	0	
5	4.32876E-13	389.9	4.31766E-13	
6	1.01164E-10	91120.1	1.01163E-10	
7	1.22125E-15	1.1	1.11022E-16	
8	1.11022E-15	1	0	
9	1.11022E-15	1	0	
10	1.11022E-15	1	0	
11	1.11022E-15	1	0	

- Same conclusion as for BER=10^{-12} from previous slide

RapidIO Analysis

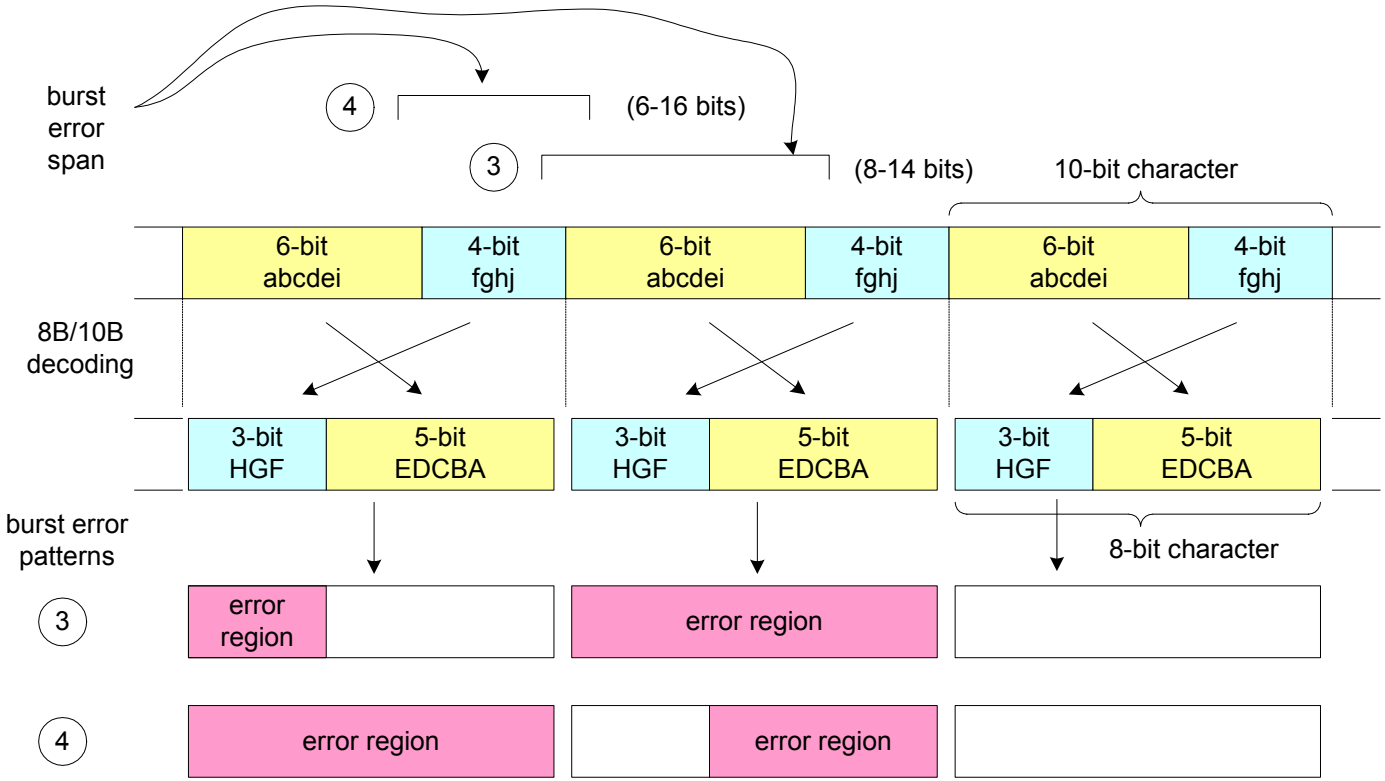
- RapidIO considered the potential error bursts that can result from the combination of DFE and 8B/10B decoders
  - "CRC-16 ability to detect burst errors in Rapid IO," from S. Gorshe of PMC-Sierra
  - Conclusion: The CRC-16 in a Rapid IO packet will detect all error bursts generated by a 5-tap DFE

Error pattern (2-5 bit bursts)



- These cases cover all 2-5 bit error bursts (including some up to 10 bits)
  - Maximum burst length = 16 bits

Error pattern (6-11 bit bursts)



- These cases cover all the additional 6-11 bit bursts (including some up to 16 bits)
  - Maximum burst length = 16 bits

Summary of Results

- The DFE analysis and enumerated error burst cases show that:
  - 5- tap DFEs produce maximum error bursts of 7 bits
  - A burst of up to 11 bits creates an error burst of no more than 16 bits in the packet after the 8B/10B decoding
  - CRC-32 can detect bursts of up to 32 bits.

Conclusions

- Limiting DFE to 2 taps is overly pessimistic
- The 5-tap DFE receiver from OIF is within the capabilities of the current CRC-32

Appendix – OIF Tap Weight Limits

(See "Reference Receiver", OIF-CEI-02.0, p.131)

- 1. Rx equalization: 5 tap DFE, with infinite precision accuracy and having the following restriction on the coefficient values:
- Let W[N] be sum of DFE tap coefficient weights from taps N through M where
  - N = 1 is previous decision (i.e. first tap)
  - M = oldest decision (i.e. last tap)
  - R_Y2 = T_Y2 = 400mV
  - Y = min(R_X1, (R_Y2 - R_Y1) / R_Y2) = 0.30
  - Z = 2/3 = 0.66667
- Then $W[N] \leq Y * Z^{(N - 1)}$
- For the channel compliance model the number of DFE taps (M) = 5. This gives the following maximum coefficient weights for the taps:
  - W[1] ≤ 0.2625 (sum of taps 1 to 5)
  - W[2] ≤ 0.1750 (sum of taps 2 to 5)
  - W[3] ≤ 0.1167 (sum of taps 3 to 5)
  - W[4] ≤ 0.0778 (sum of taps 4 and 5)
  - W[5] ≤ 0.0519 (tap 5)
  - Notes:
    - These coefficient weights are absolute assuming a T_Vdiff of 1Vppd
    - For a real receiver the restrictions on tap coefficients would apply for the actual number of DFE taps implemented (M)

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