To: T10 Technical Committee
From: Wayne Bellamy (wayne.bellamy@hp.com), Hewlett Packard
Date: June 14, 2005
Subject: T10/05-239r0 SAT - Caching mode page

Revision History

Revision 0 (June 14, 2005) first revision

Related Documents

(T10) sat-r04 – SCSI to ATA Translation (SAT), Revision 4
(T10) sbc-2r16 – SCSI Block Commands - 2, Revision 16
(T13) ata7v1r4b – AT Attachment with Packet Interface -7 Volume1, Revision 4b

Overview

1. The Caching mode page is especially critical for enabling/disabling write cache on targets. Most SCSI implementations and many popular operating systems manipulate caching (write caching) to comply with established application client requirements. Particular routines may require write caching to be enabled, whereas, other routines may require it to be disabled.
2. Complexity of the emulation is estimated to be “medium-level”.

Suggested Changes

10.1.5 Caching mode page ~~(08h)~~

The C~~c~~aching mode page (08h) defines parameters that affect the behavior of the device cache. ~~and the caching policy used.~~ (See SBC-2.)

Table 2 shows the translation of fields in the C~~c~~aching mode page.

Table 2 — Caching mode page fields

Field	SATType	Description or reference
PS ~~(Parameters Savable)~~	E~~U~~	Set to a value of 0b. A value of 1b is not supported.
PAGE CODE	I	Set to a value of 08h. This field value is specific to the Caching mode page. The SATL shall support the PAGE CODE field.
PAGE LENGTH	I	Set to 12h. Any other value is not supported.
IC ~~(initiator Control)~~	E	Set to a value of 0b. A value of 1b is not supported. ~~This bit is set to 0 and ignored. Initiator control bit set to 1 specifies that the device server use the NUMBER OF CACHE SEGMENTS or the CACHE SEGMENT SIZE, depending on the SIZE bit to control the caching algorithm.~~
ABPF ~~(Abort Prefetch)~~	E	Set to a value of 0b. A value of 1b is not supported.~~This bit is set to 0 and ignored. This bit is used in conjunction with the DRA bit and defines how prefetch operation is controlled when a new command is received.~~
CAP ~~(Caching analysis permitted)~~	E	Set to a value of 0b. A value of 1b is not supported.~~This bit is set to 0 to indicate that caching analysis is disabled and ignored for a MODE SELECT command.~~
DISC ~~(Discontinuity)~~	E	Set to a value of 0b. A value of 1b is not supported.~~This bit is set to 0~~

		~~and is ignored. This bit defines whether prefetches can be continued across discontinuities.~~
SIZE	E	Set to a value of 0b. A value of 1b is not supported.~~This bit is set to 0 and is ignored. This bit indicates whether CACHE SEGMENT SIZE field or NUMBER OF CACHE SEGMENTS field to use for caching algorithms.~~
WCE ~~(Write Cache Enable)~~	E	1) WCE value returned by the MODE SENSE command: The SATL shall determine if the non-packet device write cache is enabled or disabled from the ATA IDENTIFY DEVICE data word 85, bit 5. If the write cache is enabled the SATL shall return a value of 1b for the WCE bit. If the write cache is disabled the SATL shall return a value of 0b for the WCE bit. **(NOTE to W.G.: I don't believe that a precursory "write cache supported" check is necessary here unless T13 individuals request otherwise.)** 2) WCE value controlled by the MODE SELECT command: • If WCE is set to 0b, the SATL shall disable the non-packet device write cache by issuing an ATA SET FEATURES – Disable write cache command (EFh with Feature register value of 82h). **(Note to editor: Settings preservations must be addressed by the MODE SELECT command translation. This must be done for "software settings preservation" (SATA II Ext) in addition to "ATA SET FEATURES - Disable reverting to power-on defaults.")** • If WCE is set to 1b, the SATL shall enable the non-packet device write cache by issuing an ATA SET FEATURES – Enable write cache command (EFh with Feature register value of 02h). **(Note to editor: Settings preservations must be addressed by the MODE SELECT command translation. This must be done for "software settings preservation" (SATA II Ext) in addition to "ATA SET FEATURES - Disable reverting to power-on defaults.")** ~~By default, this bit shall be set to 1 to indicate that write caching is enabled.~~ ~~If this bit is set to 0 using a MODE SELECT command, it shall be translated into a SET FEATURES command 82h to disable write cache.~~ ~~If this bit is set to 1 using a MODE SELECT command, it shall be translated into a SET FEATURES command 02h to enable write cache.~~ ~~This bit it set to the default values after a logical unit reset or a target reset.~~
MF ~~(Multiplication Factor)~~	E	Set to a value of 0b. A value of 1b is not supported.~~This bit is set to 0 and is ignored.~~
RCD ~~(Read Cache Disable)~~	E	Set to a value of 0b. A value of 1b is not supported.~~This bit shall be set to 0 and unchangeable.~~
DEMAND READ RETENTION PRIORITY	E	Set to a value of 0h. Any other value is not supported.~~This field is set to zero and ignored.~~
WRITE RETENTION PRIORITY	E	Set to a value of 0h. Any other value is not supported.~~This field is set to zero and ignored.~~
DISABLE PRE-FETCH TRANSFER LENGTH	E	Set to a value of 0b. A value of 1b is not supported.~~This field is set to zero and ignored. This field specifies the cut off transfer length in number blocks to disable prefetch for long transfers.~~
MINIMUM PRE-FETCH	E	Set to a value of 0b. A value of 1b is not supported.~~This field is set to zero and ignored.~~
MAXIMUM PRE-FETCH	E	Set to a value of 0b. A value of 1b is not supported.~~This field is set to~~

		~~zero and ignored.~~
MAXIMUM PRE-FETCH CEILING	E	Set to a value of 0b. A value of 1b is not supported.~~This field is set to zero and ignored.~~
FSW ~~(Force Sequential Writes)~~	E	Set to a value of 0b. A value of 1b is not supported.~~This field is set to zero and ignored.~~
LBCSS ~~(Logical block cache segment size)~~	E	Set to a value of 0b. A value of 1b is not supported.~~This field is set to zero and ignored. This bit specifies the units to be used for CACHE SEGMENT SIZE field.~~
DRA ~~(Disable Read Ahead)~~	E	1) DRA value returned by the MODE SENSE command: The SATL shall determine if the non-packet device look-ahead is enabled or disabled from the ATA IDENTIFY DEVICE data word 85, bit 6. If the look-ahead is enabled the SATL shall return a value of 0b for the DRA bit. If the look-ahead is disabled the SATL shall return a value of 1b for the DRA bit. **(NOTE to W.G.: I don't believe that a precursory "look-ahead supported" check is necessary here unless T13 individuals request otherwise.)** 2) DRA value controlled by the MODE SELECT command: • If DRA is set to 0b, the SATL shall enable the non-packet device read look-ahead feature by issuing an ATA SET FEATURES – Enable read look-ahead feature command (EFh with Feature register value of Aah). **(Note to editor: Settings preservations must be addressed by the MODE SELECT command translation. This must be done for "software settings preservation" (SATA II Ext) in addition to "ATA SET FEATURES - Disable reverting to power-on defaults.")** • If DRA is set to 1b, the SATL shall disable the non-packet device read look-ahead feature by issuing an ATA SET FEATURES – Disable read look-ahead feature command (EFh with Feature register value of 55h). **(NOTE to editor: Settings preservations must be addressed by the MODE SELECT command translation. This must be done for "software settings preservation" (SATA II Ext) in addition to "ATA SET FEATURES - Disable reverting to power-on defaults.")** ~~By default, this bit shall be set to 0 to indicate that read look-ahead is enabled.~~ ~~If this bit is set to 1 using a MODE SELECT command, it shall be translated into a SET FEATURES command 55h to disable read look-ahead.~~ ~~If this bit is set to 0 using a MODE SELECT command, it shall be translated into a SET FEATURES command AAh to enable read look-ahead. This bit it set to the default values after a logical unit reset or a target reset.~~
NV_DIS	E	Set to a value of 0b. A value of 1b is not supported.
NUMBER OF CACHE SEGMENTS	E	Set to a value of 0b. A value of 1b is not supported.~~This field is set to zero and ignored.~~
CACHE SEGMENT SIZE	E	Set to a value of 0b. A value of 1b is not supported.~~This field is set to zero and ignored.~~
~~NON-CACHE SEGMENT SIZE~~	E	~~This field is set to zero and ignored.~~

Bit or field values that are not supported shall cause the SATL to return a CHECK CONDITION with sense key set to ILLEGAL REQUEST and additional sense code set to INVALID FIELD IN PARAMETER LIST.

~~NOTE 1 - ATA provides no method to disable read cache. The closest reasonable substitute is to precede each READ command with a READ VERIFY SECTORS or READ VERIFY SECTORS EXTENDED command, with will force a media access. But this is considered too extreme for the purposes of SATL.~~