PMC-SIERRA

QuadPHY™ 6G Device

PMC-Sierra Inc.

T10 SAS-2 WG meeting, Houston, 25-26May 2005

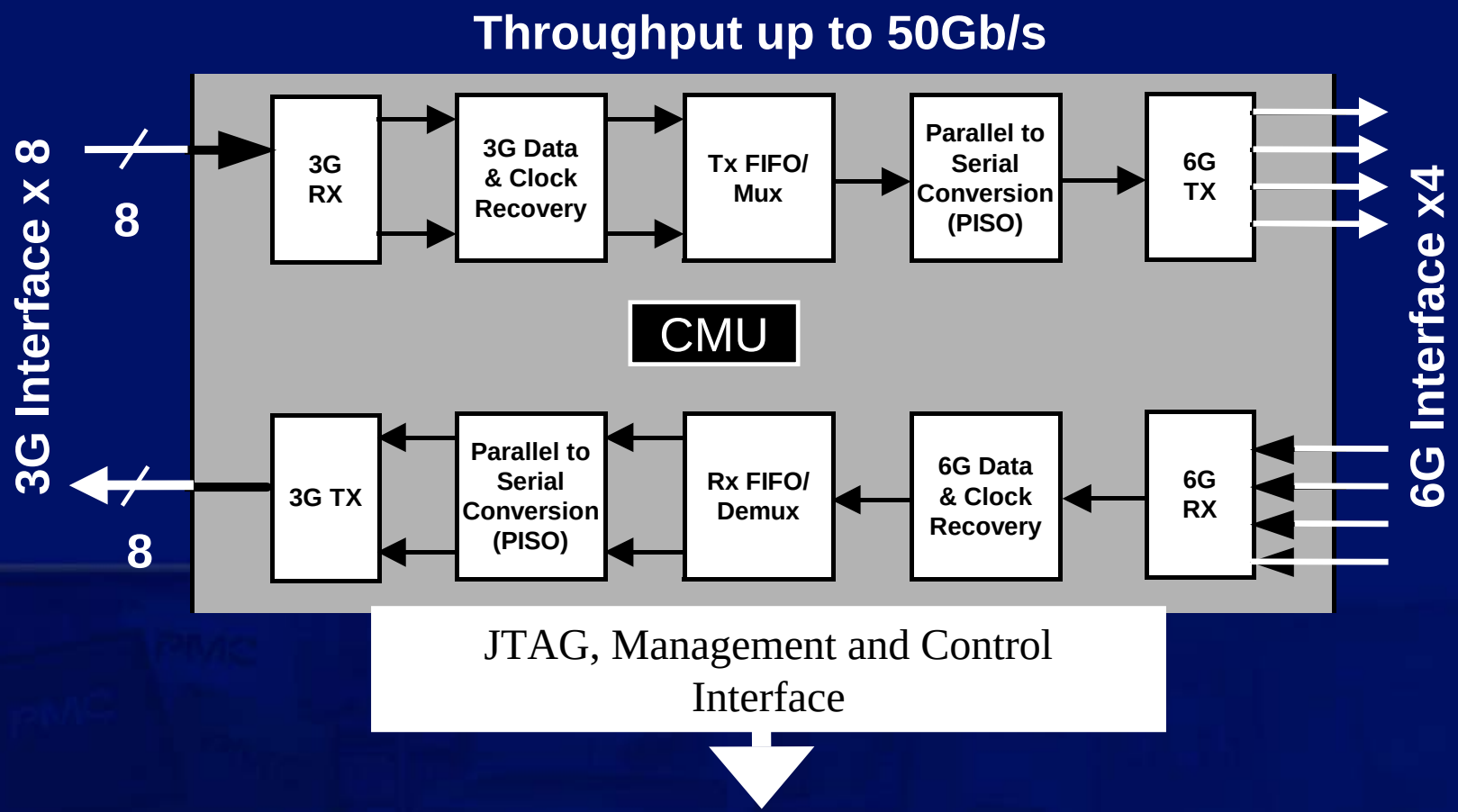
www.pmc-sierra.com

GENERAL FEATURES

- Complies with OIF CEI-6G requirements
- Serial Multiplexer/Demultiplexer with a full-rate two-way aggregate throughput of 50 Gbit/s at 6.25 Gbit/s for backplane applications, 2-level NRZ coding:
  - Multiplexes eight 3.125 Gbit/s serial links into four 6.25 Gbit/s serial links
  - Demultiplexes four 6.25 Gbit/s serial links into eight 3.125 Gbit/s serial links
- Protocol agnostic SERDES device that can support scrambled NRZ data as well as 8B/10B coded data
- Integrated clock synthesis, clock recovery, serializer/deserialzer and built-in self-test

Full feature list could be found on www.pmc-sierra.com

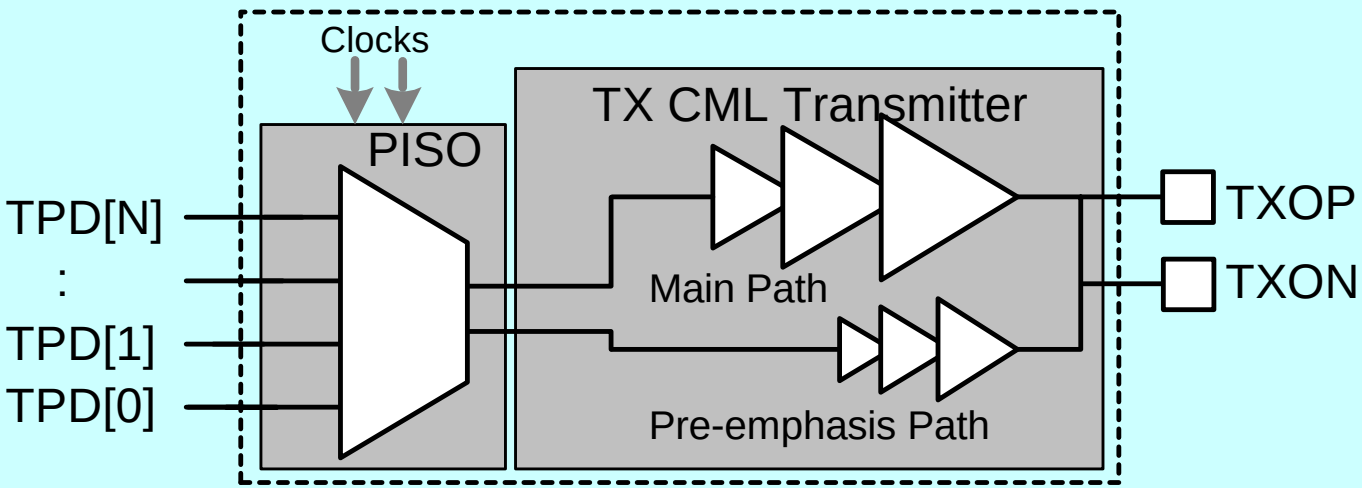
BLOCK DIAGRAM



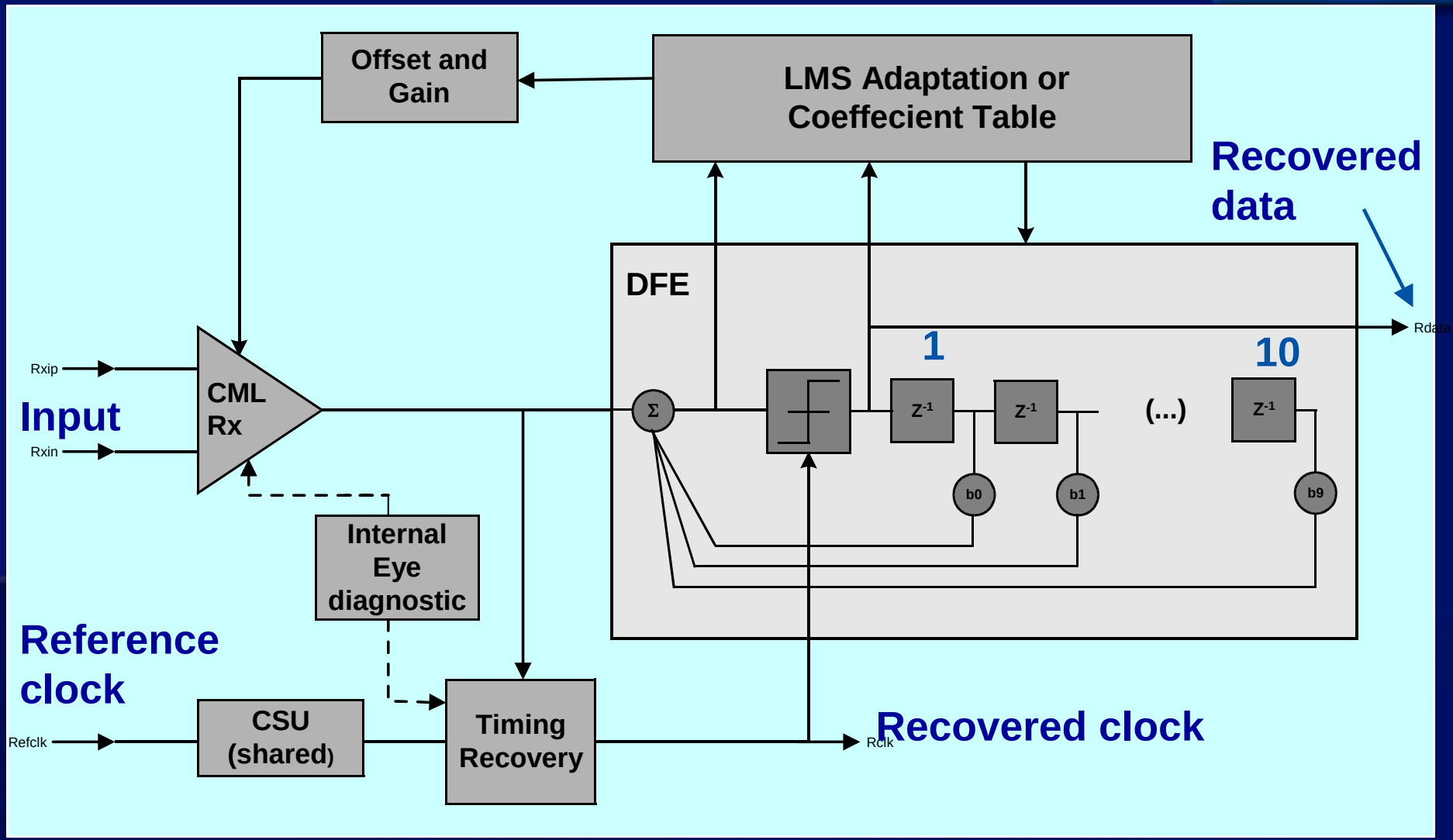
6G INTERFACE

- Four Tx and Rx serial links with a maximum signaling rate of 6.4 Gbit/s
- Programmable Tx 2-tap FIR (pre-emphases)
- Adaptive receiver equalization with 10-tap DFE ensures robust serial link operation and low BER

Tx WITH PRE-EMPHASES



RECIEVER WITH DFE EQUALIZER



- The DFF equalizer with adaptation and internal eye diagnostic

TEST AND MONITORING FEATURES

- Error link monitoring capability
- Built-in self-test (BIST) via internal PRBS generator/ checker
- Pin programmable or software configurable operation using 2-pin IEEE 802.3ae MDC/MDIO serial management interface
- IEEE 1149.1 JTAG Boundary Scan support
- Supports parallel and serial diagnostic loopback
- Comprehensive evaluation platform available to de-risk customer system development
  - Version with 6G on SMA connector (good for testing SAS-2 link signal integrity)
  - Version with 6G on Tyco HM Zd Connector

PHYSICAL CHARACTERISTICS

- Low power operation, 3.0 W typical
- 0.13 μm CMOS technology
- Flip-Chip Package, 320-pin FCBGA
- 19 x 19 mm, 1.0 mm pitch
- 1.2 V core and 1.2 V/2.5 V I/O
- Designed to operate over a wide temperature range and is suited for central office and outside plant equipment.

EXPERIMENTAL RESULTS @ 6.25Gb/s

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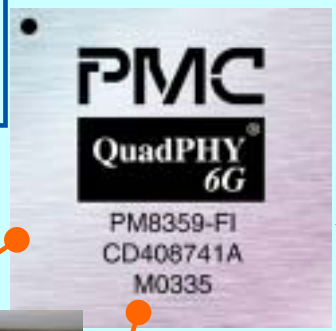
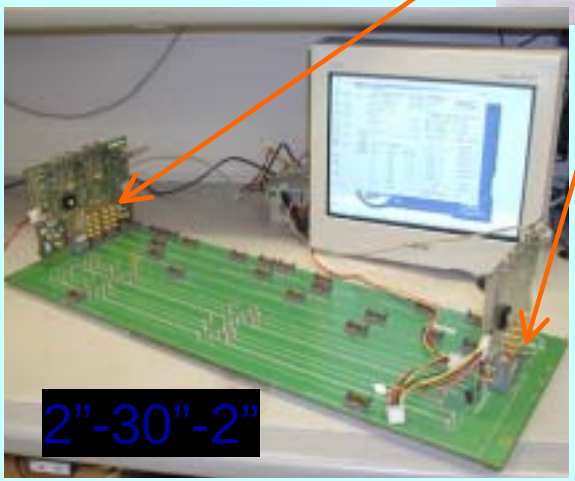
Tx 6.25GB/s

PRBS-31,
No cross talk,
8dB emphasis

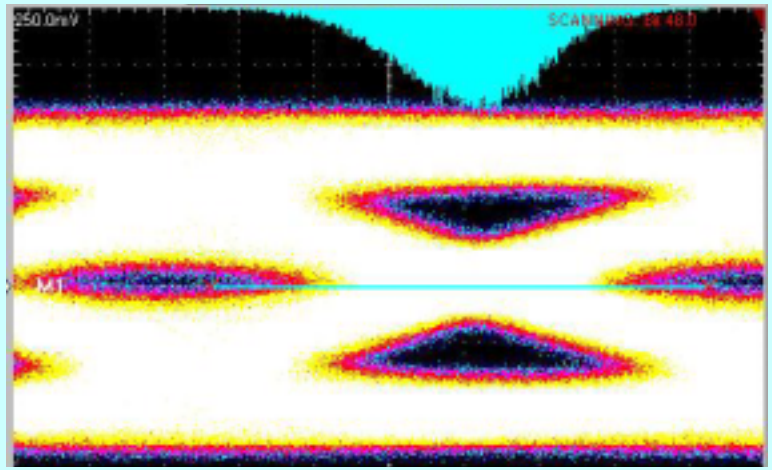




Molex Legacy Backplane

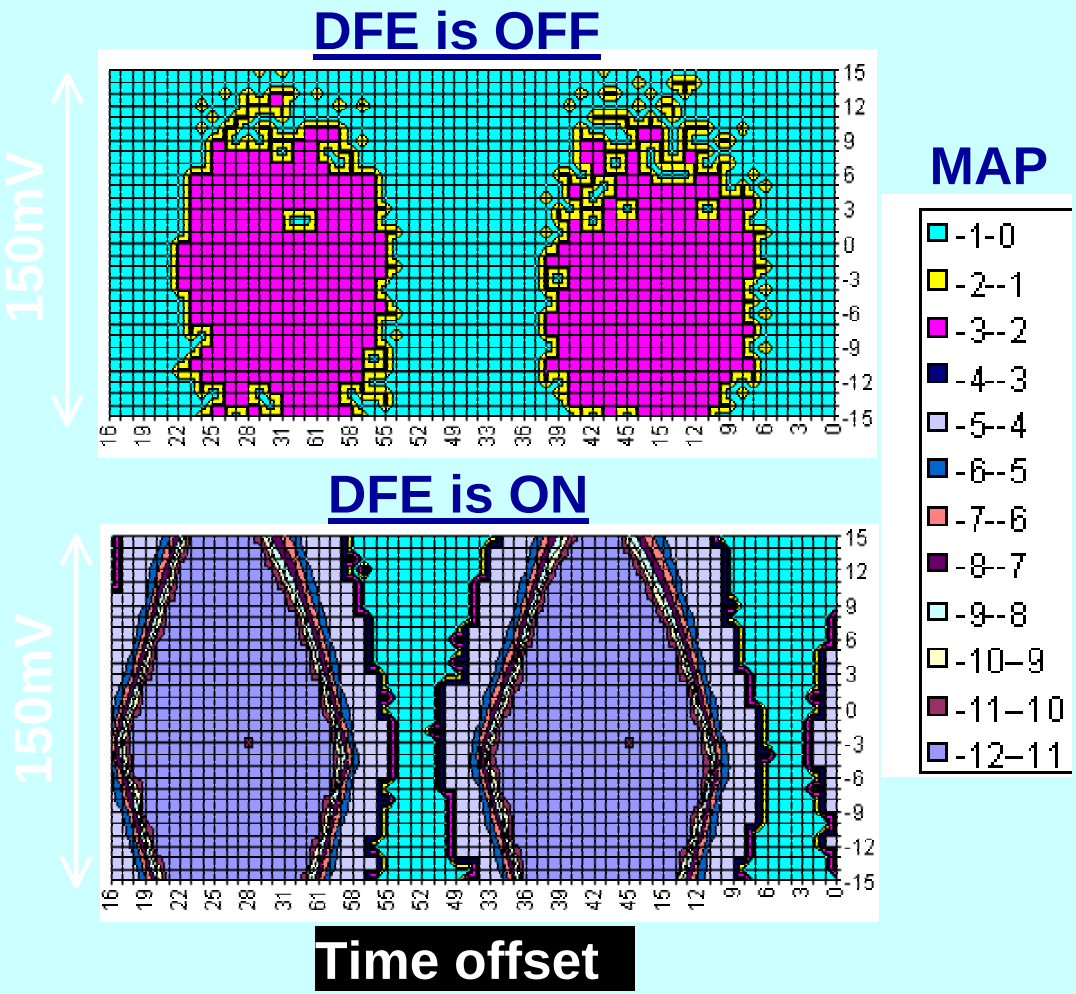
- **Eye is closed (BER=1e-2) at 86cm backplane**
- **Rx with 8 Tap DFE restores the eye**
- **Link operates below BER=1e-15 with 99% confidence level**

Rx Eye



6.25GB/s

INTERNAL EYE CONTOURS AT 6.25GB/s



- Backplane closes the eye, BER=1e-2

- DFE opens the eye. BER=1e-12 is eye setup limit, not the device. Device operated >200 h with no errors resulting BER < 1e-15

- Observation time 100s per dot

PERFORMANCE SUMMARY

- QuadPHY-6G is implemented in a standard 0.13µm CMOS process. It employs 4.9-Gb/s to 6.4-Gb/s NRZ SERDES with adaptive 10-tap DFE technique and 2-tap Tx
- The chip is able to achieve a BER better than 1E-15 over a 34” (86-cm) legacy FR4 backplane with two connectors
- The evaluation boards are available with SMA connectors on 6G I/O side suitable for SAS-2 link performance investigation

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Thinking You Can Build On

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