RapidIO
The Embedded System Interconnect

Next Gen SRIO PHY Preliminary 5.0/6.25 Gbps Electrical Spec Status T10/05-199r0

RapidIO Technical Working Group

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RapidIO Technology

- A point-to-point packet-based switched system interconnect technology
- Developed for large scale embedded systems
  - Control, data and signal plane applications
- Developed jointly by embedded semiconductor vendors and OEMs
- An international standard - ISO/IEC 18372
- Serial and parallel physical layer definitions
- Shipping on chips and in backplane applications now

Leading RapidIO Supporters

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Our Approach to PHYs

- Leverage industry standard PHY technology
  - Currently using EIA-644 and IEEE XAUI
- RapidIO does not standardize mechanicals
  - Will encourage and enable external Standards Organizations as their member companies define use of RapidIO
  - VxS (VME), PICMG 2.18 (cPCI), XMC, AMC, ATCA, CompactTCA

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Current RapidIO PHY

	Parallel	Serial
Electrical std	LVDS	XAUI SERDES
Coding Run length DC balanced Overhead	None Long No Frame signal	8B10B 5 bits Yes 20%
Data Width	8, 16-bit	1x, 4x
Data rates (Mbps)	500, 750,1000, 1500, 2000	1000 2000 2500
Clocking	Source synchronous	Clock and data recovery
Tx Amplitude (mV differential pk-pk)	400-1080	500-1000 short 800-1600 long
Rx Amplitude	200-1200	200-1600

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Future PHY Status

- RapidIO TA has acknowledged the need for higher performance PHY technology and is actively developing a new specification
- Completed next generation PHY requirements document guiding specification development
- Current proposal levarages CEI from the OIF

RapidIO Channels

- Role as system interconnect influences channel scenarios
  - Both control and data plane applications
  - Short reach
    - Chip-to-chip
    - Carrier to mezzanine board
  - Long reach
    - Backplane
    - Backplane plus carrier card with mezzanine
- Support both existing and green field designs
  - Retain existing FR4 backplane materials and connectors

Architectural Considerations

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- Higher data rates primarily driven by data plane applications although some highly pin-constrained settings also see a need
- Applications
  - Encapsulation of OC-192 like streams
    - 10GbE using four lanes or less
    - At least 16 Gb/s PDU data rate after encoding overhead
    - Additional bandwidth desired for additional traffic on the same link e.g. control plane traffic
  - Other interesting data rates
    - FibreChannel: 4.25 and 10.5 Gbaud
- Desire a mechanism to measure receiver performance and adjust transmitter parameters as necessary
  - Interesting in system scenarios where wire lengths widely vary
- Some interest in a high-efficiency encoding (CEI-P or 64B66B) at both 5-6G and 10-11G to allow fall back from 10-11G should a channel be unable to support full-speed

Gen1 SRIO Physical Layer Specification

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- **Electrical Spec Methodology for Gen1 is based on XAUI**
  - Configuration: Supports 1X and 4X lane configurations
  - Speed
    - 1.25, 2.5, and 3.125 Gbps
  - Reach Goals
    - Long: 50cm of FR4 with two connectors
    - Short: unspecified length of FR4 with one connector
  - Compliance Channel: None defined. Transmitter and Receivers must meet near end eye masks
  - Parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002
  - XAUI and SRIO electrical designs should be compatible. SRIO electrical specifications at speeds/range not defined by XAUI are based on suitably modified XAUI specifications
  - 8b/10b encoding
  - AC Coupling is supported (DC optional)
  - Long/Short reach drivers and receivers shall be compatible
  - Supports Hot Plug
  - Clocking requirements for any transmitter or receiver clock is +/-100ppm
  - BER <= 10E-12 are required

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Gen2 SRIO Overview

- Requirements
  - No change to Logical Layer
  - No change to Transport Layer
  - No change to Link Layer portion of Physical Layer
  - Minimize changes to PCS (encoding) portion of Physical Layer
- Non-Requirements
  - Autonegotiation
- Double (~5-6Gbps) and later Quad speed(~10Gbps)
- Two channel optimized variants
  - Short reach (Chip to Chip / Chip to Mezzanine)
    - 20 cm with 1 connector
  - Long reach (Line Card over Backplane to Line Card)
    - 80-100 cm with 2 connectors
- Retain FPGA support over long-term

RapidIO Layering

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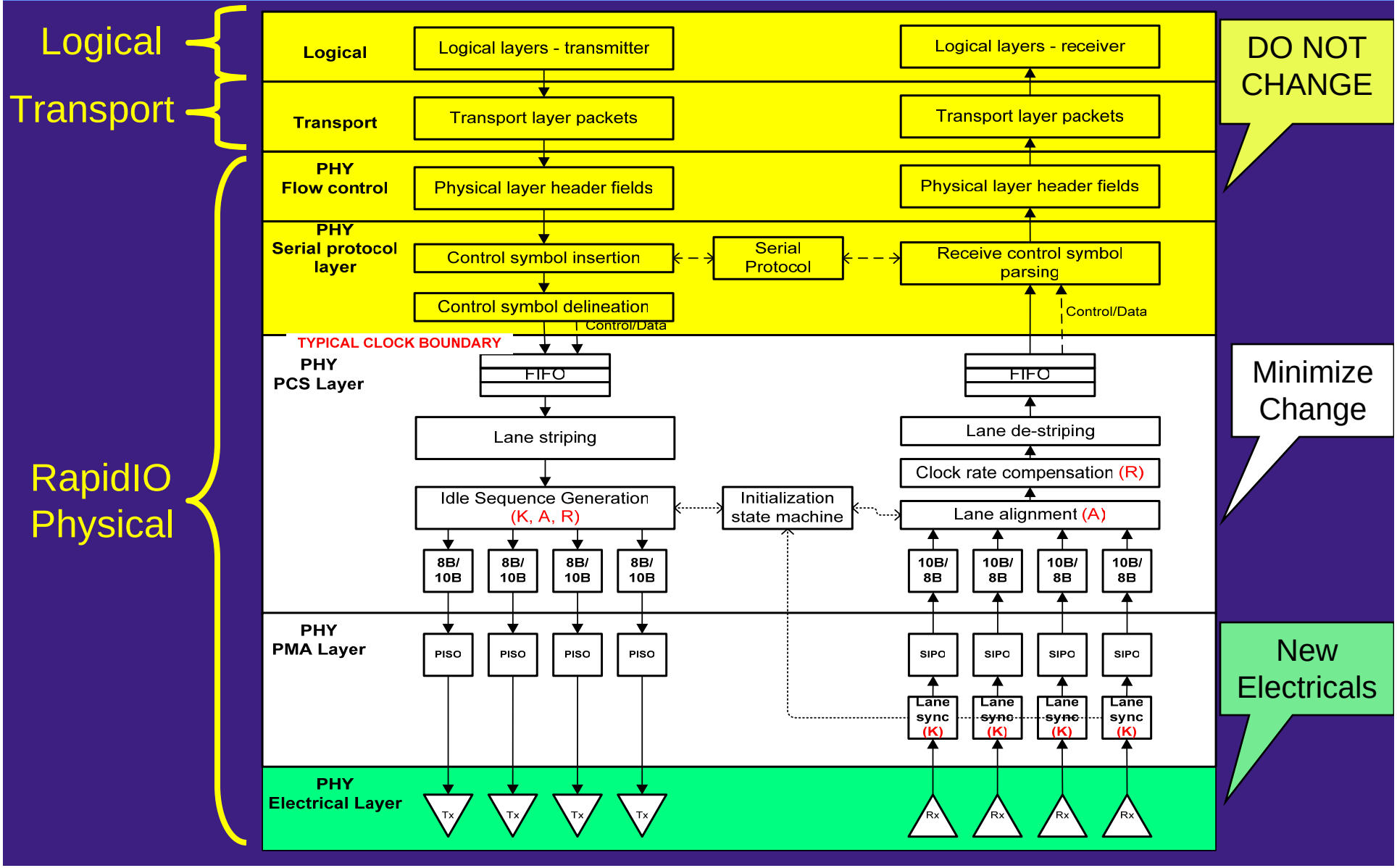

Gen2 SRIO Physical Layer Specification

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- **Electrical Spec Methodology for Gen2 is based the OIF CEI 6G Specification**
  - Configuration: Supports 1X , 2X, 4X, 8X, and 16X lane configurations
  - Speed
    - 5.0 and 6.25 Gbps
  - Reach Goals
    - Long: 80cm of improved FR4 with two connectors (stretch goal of 100cm)
    - Short: 20cm of improved FR4 with one connector
  - Compliance Channel: Follows OIF Stateye methodology for determining channel compliance (A range of materials, connectors, and distances may be compliant)
  - 8b/10b encoding will be maintained
  - AC Coupling shall be supported (DC optional)
  - Long/Short reach drivers and receivers shall be compatible
  - Supports Hot Plug
  - Rev 1.3 clocking requirements will be maintained
  - BER <= 10E-12 are required
  - Rev1.3 lane-lane skew requirement maintained
  - Scrambling will be used for one or more reach configurations
  - Gen2 devices are not required to operate at Gen1 speeds and configuration, but Gen2 device that operate at the same speed and lane configuration must

Why OIF CEI 6G for Gen2 SRIO PHY?

- Historically, SRIO has focused it efforts on defining efficient communications protocols and have chosen to leverage existing PHY electrical standards for compatibility reasons.
- OIF CEI 6G has very similar goals as Gen2 SRIO, so leveraging the OIF work makes sense.

Gen2 SRIO Phy Layer Spec Issues

- **Decision Feedback Equalizer (DFE) Receiver Support**
  - DFE receivers are typically used at data rates greater than 5Gbps.
  - Clock/data recovery is based on sampling several sequential bits using feedback.
  - Use of feedback means a single error in the incoming stream will lead to a burst of errors .
    - Multilane configurations complicate burst error detection (i.e a single error will lead to a burst of errors separated across multiple lanes
    - CRC for data and control symbols may need to be modified
- **Work to date**
  - CRC Polynomials for burst error detection in multilane configurations
  - Maximum burst error length analysis
  - Analysis of DFE tap weights on burst error length

Gen2 SRIO Phy Layer Spec Issues- cont

- **Lane Configurations**
  - Scrambling vs. Striping order
  - Error detection in multilane configurations (DFE error multiplication)
  - Scrambler synchronization across lanes
- **Work to date**
  - Evaluation of scrambling/striping order

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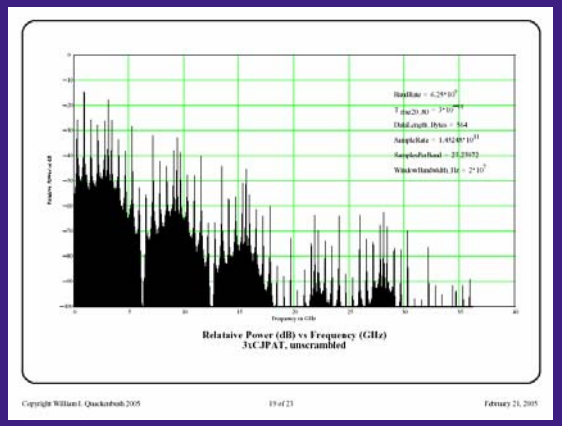
Gen2 SRIO Phy Layer Spec Issues- cont

- **Scrambler**
  - What speed/reach configurations?
  - What polynomial order?
  - Scrambling /lane striping order (i.e. scramble, then stripe, or stripe, then scramble?)
  - Scrambler initialization (offset, disable for debug, how to initialize?)
  - Scrambler data only, or data and control symbols?
- **Work to date**
  - Impact of scrambler polynomial choice on the spectral content of 8B/10B encoded signals
  - Autocorrelation of scrambler sequences

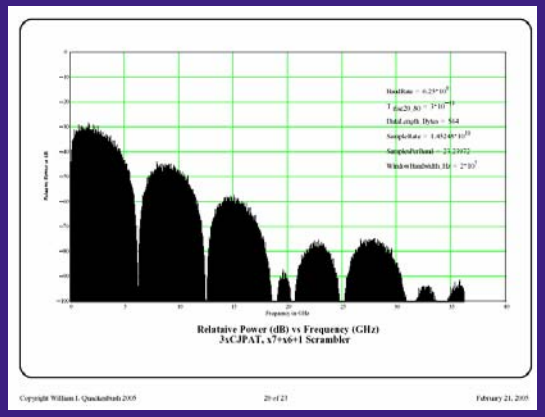
Spectral Content of Scrambler Polynomials- Example

- Shown below is the spectral content of CJTPAT after scrambling and 8B/10B encoding for two different scrambler polynomial choices

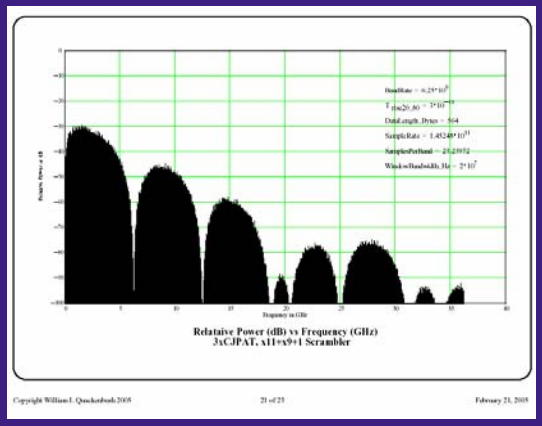
Unscrambled



$X^7 + X^6 + 1$



$X^{11} + X^9 + 1$



CEI with Respect to OIF, RapidIO, and SAS

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- Discovery, Configuration, & Initialization
  - Out of Scope for OIF
  - RapidIO in-band methodology but does not define auto rate negotiation
  - SAS probably requires In-Band autonegotiation and initialization
- Data Format
  - OIF assumes scrambled data
  - RapidIO will scramble data then apply 8B/10B coding
  - SAS coding ?
- Receiver DFE causes Burst Errors
  - Error Detection capability (CRC) must be reviewed
- Channel
  - OIF and RapidIO
    - Support a variety of connectors and backplanes.
  - SAS environment is more limited.
    - Known connectors, and cabling.
- Compliance Methodology & Test Points
  - CEI
    - Transmitter compliance masks at Device Edge
    - Channel compliance via simulated operation with Channel's Measured S Parameters
    - Receiver must operate with any compliant Transmitter & Receiver
  - RapidIO
    - Compliance methodology not yet determined. Likely to follow CEI model.
  - SAS
    - Compliance Points at connectors (?) not device edge.

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Next Steps

- **Establish Liaison between RapidIO and T10**
  - **RapidIO is willing to share our technical work for 6G SRIO**
- **Collaborative Ideas**
  - **Compliance channel requirements (acceptable materials, connectors, channel loss for 5/6.25Gbps operation, StatEye, etc.)**
  - **Scrambler requirements for 5/6.25Gbps operation**
  - **DFE support (burst error analysis, how to spec)**