<u>Timely Safe Recording</u>
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4.7 Timely Safe Recording method
4.7.1 General
In order to overcome the limitations of host defect management and the limitations of Logical Unit defect management, a new recording method, timely and safe, is proposed. The general idea of this method is to postpone the time consuming management of defects after an initial fast writing phase. The initial writing phase is fastened by reducing the amount of write-to-verify-to-write transitions. Defect management through reallocation is still performed by the Logical Unit for non-streamed data. Defect management may be performed by the host for streamed data (through reallocation).

This method is applicable to any media type offering Logical Unit-based defect management and the resulting media is read-write backward compatible with legacy host-logical unit pairs.

The Logical Unit reports support of this feature through TSR Feature (Feature Code 0042h).

The host and the Logical Unit agree on an error reporting threshold through the error reporting threshold length field of the Read/Write Error Detection and Recovery Parameters Mode Page. The Logical Unit signals necessity to read defect information through WRITE ERROR RECOVERY NEEDED. The host gathers this defect information using GET PERFORMANCE command.

4.7.2 Two phase recoding
For this method, the recording is organized in two phases.

4.7.2.1 Phase one – fast recording and error detection
During this phase, the host issues write commands (WRITE10, WRITE12 and/or WRITE AND VERIFY) with TSR bit set to one. If BD-R Pseudo-Overwrite (POW) Feature is present and current, the host shall during this phase write only to unrecorded LBA when TSR bit is set to one. The Logical Unit performs the writes with error detection but no automatically reallocation on error (regardless of AWRE bit in mode page 01h). The Logical Unit reports error discovery using WRITE ERROR RECOVERY NEEDED within the agreed threshold (see 6.50.3 Command Execution). The host reads the defect information using GET PERFORMANCE command with Type=02h (Defect Status data), and resumes writing. The host shall retain both the data and its destination LBA for the next phase for non-streamed data located on the reported defects in Defect Status Descriptor. The host may and is recommended to retain the same information for streamed data located on the reported defects in Defect Status Descriptor. The host concludes this phase with a SYNCHRONIZE CACHE command. The Logical Unit will finish any pending verification and report all found defective writable units (see 6.47.3 Command Execution). The host is expected to have formed a list of defects pairs (data, LBA) at the end of this phase.

The TSR writes are limited to complete ECC blocks to avoid read-write-modify by the logical unit in phase two. (Read-write-modify in phase two could fail in case the ECC block is damaged during phase one.)

4.7.2.2 Phase two – hardware defect management
During this phase, for all non-streamed data, the host issues write commands with TSR bit set to zero (rewritable media such as BD-RE, HD-DVD-Rewritable or DVD-RAM) or one (write-once media such a BD-R) for defective writable units reported by the Logical Unit during the previous phase. Now the Logical Unit can proceed with automatic reallocation / defect management.

For streamed data, the host can decide to take 3 different actions:
a) Nothing. The streamed content can be played back and interruptions in the stream are possible, due to the bad clusters, there are no timing problems; This permits simplification of the host implementation and does not require to retain defect pairs for streamed content at phase one.
b) Software reallocation. For rewritable media, host deduces from the defect list free good locations where it reallocates the data. For write-once media, the unrecorded locations are assumed good. For both rewritable and write-once media, the host updates the file system information to reflect this reallocation. Notice this is performed using allocation descriptors of the

data and not using a remapping table. This is also not a phase two, but a new phase one (to avoid hardware reallocation). There is a potential recursion if new defects are found, however the recursion is ended by exhausting the free space of the media. The reallocated streamed content plays without problems and no timing problems.

c) Hardware remapping. Host uses the defect pairs list from the phase one to rewrite the bad clusters data and generates a linear replacement. This stream will have all the content but will have timing problems during real-time playback. The content can eventually be copied to a good piece of media.

The action b) is recommended.

4.7.3.0 Implementation notes for the Logical Unit

The Logical Unit may simplify its implementation by using the deferred error report possibility brought by the TSR error reporting threshold only for sequential writing. For non-sequential writing, the simplified implementation would perform verification immediately. For sequential writing, the simplified implementation would memorize the starting LBA of the sequential writing. Then it would perform verification when the LBA of a write command minus the memorized LBA equal or higher the error reporting threshold, or when a non-sequential write interrupts the sequential writing, or when the Logical Unit finds an opportune earlier switch to verification.

The Logical Unit may re-use defect tables (DFL) cache from the media to temporarily store defect information discovered during the phase one, so it does not need additional memory to perform TSR. This ensures that the Logical Unit is capable to store at least as much defect information as the media physical specification is able to handle. If more defects than the media physical specification is able to handle is found before the Logical Unit could report them to the host through GET PERFORMANCE command issued by the host, Logical Unit shall behave as if the DFL list has been exhausted (write failure). The Logical Unit shall forget defect information already reported to the host through GET PERFORMANCE response if the DFL is about to be exhausted.

For BD devices, the Logical Unit may mark as PBA with RDE the defective ECC blocks found during phase one. So if an host software fails for some reason to perform phase two, the Logical Unit still maintains correct information status for these ECC blocks.

For Write-Once media, write commands are issued by the host with TSR bit set to one for both phases. The Logical Unit can distinguish write commands from phase one and phase two by the respectively recorded or unrecorded status of the LBA in CDB. If the LBA is unrecorded, this is phase one and the Logical Unit shall behave as described in 4.7.2.1 (recording and error detection). If the LBA is recorded, this is phase two and the Logical Unit shall behave as described in 4.7.2.2 (remapping the data to spare area). However the Logical Unit shall rejects attempt to miss-use the TSR bit if the LBA is recorded but absent from the DFL and defect information discovered during the phase one.

For Rewritable media, write commands with TSR bit set to one are issued by the host only during phase one.

4.8 Real-Time Stream Recording/Playback Model
[…]

5.1.6 TSR Feature

A Logical Unit that reports the TSR (Timely Safe Recording) feature is able to detect and report defectives writable units and to manage the defect or not according to the instruction from the host. The feature descriptor is defined in Table 11.

Table 11. TSR Feature Descriptor

Bit / Byte	7	6	5	4	3	2	1	0
0	(MSB)							
1				Feature Code = 0042h				(LSB)

	Bit 7 6 5 4 3	Bit 2 1 0	

Byte				
2	Reserved	Version = 0h	Persisten t	Current
3	Additional Length = 04			
4	Reserved			
5	Reserved			
6	Reserved			
7	Reserved			

The Feature Code field shall be set to 0042h.

The Version field shall be set to 0h.

The Persistent bit shall be set to zero, indicating that this Feature may change its current status.

The Current bit, when set to zero, indicates that this Feature is not currently active and that the Feature dependent data may not be valid. When set to one, this Feature is currently active and the Feature dependent data is valid.

The Additional Length field shall be set to 040h.

When this feature is present and current, the Logical Unit provides error detection and reporting within selectable threshold, and controllable hardware defect management. See 4.7, Timely Safe Recording method for a description of implementation requirements

[…]

6.8 GET PERFORMANCE Command

[…]

6.8.3.4 Defect Status data (Type=02h)

This command reports Defect Status data to the Initiator that is created by certification on the Restricted Overwrite media or by TSR writing. If the mounted media is not a Restricted Overwrite media or if the Logical Unit does not support certification, and if the Logical Unit does not support TSR on the current media, this command shall be terminated with CHECK CONDITION status and SK/ASC/ASCQ values shall be set to ILLEGAL REQUEST/INVALID FIELD IN CDB.

The Data Type field in CDB shall be set to zero.

All Defect Status data shall be for LBAs that are greater than or equal to the Starting LBA specified in the CDB. In the case of TSR, the host when reading defect information after the logical unit reported CHECK CONDITION and sense bytes SK/ASC/ASCQ WRITE ERROR. RECOVERY NEEDED shall set the Starting LBA in the CDB to the lowest LBA for which the host knows the data (according the agree error reporting threshold length).

The Write and Except bits in the Performance Header for Defect Status data are not used and shall be set to zeros.

Defect Status Descriptors shall be transferred to the Initiator in ascending order. If the certified areas are non-contiguous and scattered, separate descriptors, to exclude the void areas shall return the Defect Status Descriptor(s).

The Defect Status Data Length field shall specify the amount of data that follows the Defect Status Data Length field. If there is no Defect Status data on the media, Defect Status Data Length field shall be set to 4 and no Defect Status Descriptor shall be transferred.

[…]

Table 285 . Defect Status Descriptor

Bit Byte	7	6	5	4	3	2	1	0
0	(MSB)							
1				Start LBA				
2								
3								(LSB)
4	(MSB)							
5				End LBA				

	7	6	5	4	3	2	1	0
6								
7								(LSB)
8	Blocking Factor							
9	Reserved					First Bit Offset		
10	DS #8	DS #7	DS #6	DS #5	DS #4	DS #3	DS #2	DS #1
…	…	…	…	…	…	…	…	…
2047	DS # 16 304	DS # 16 303	DS # 16 302	DS # 16 301	DS # 16 300	DS # 16 299	DS # 16 298	DS # 16 297

The Start LBA field contains the start Logical Block Address of the certified sector where the following Defect Status (DS #n bits) starts. The returned Logical Block Address shall be the first sector of a Block that contains logical blocks specified by the Blocking Factor field.

The End LBA field contains the end Logical Block Address of the certified sector where the following Defect Status (DS #n bits) ends. The returned Logical Block Address shall be the last sector of a Block that contains logical blocks specified by the Blocking Factor field.

The Blocking Factor field shall indicate the number of logical blocks per DS #n bit. In the case of DVD-RW and DVD-RAM, this field shall be set to 16 as an ECC Block. In the case of HD-DVD-Rewritable, BD-R and BD-RE, this field shall be set to 32 as an ECC Block.

[…]

6.47 SYNCHRONIZE CACHE Command

[…]

6.47.3 Command Execution

In streamed write operations, the SYNCHRONIZE CACHE command shall force conditions equivalent to a buffer underrun.

If all data in the cache is synchronized with the media when this command is received, it shall not be considered an error.

The Logical Unit shall perform any pending verification for TSR at this time:

- If IMMED bit is set to zero, and at least one defective writable unit was found during the cache synchronization, the Logical Unit shall terminate the command with CHECK CONDITION and sense bytes SK/ASC/ASCQ WRITE ERROR. RECOVERY NEEDED.
- If the IMMED bit is set to one, the host shall poll the progress of the synchronize cache operation using TEST UNIT READY command until the Logical Unit reports either no CHECK CONDITION or if at least one defective writable unit was found during the cache synchronization CHECK CONDITION and sense bytes SK/ASC/ASCQ WRITE ERROR. RECOVERY NEEDED.

In both cases, the Logical Unit shall however complete the synchronization of all data in the cache and the verifications for TSR prior to terminating the SYNCHRONIZE CACHE operation with CHECK CONDITION with said sense bytes. If this CHECK CONDITION with said sense bytes is returned, the host shall read the defect information using GET PERFORMANCE command with Type=02h (Defect Status data).

[…]

6.50 WRITE (10) Command

[…]

6.50.2 The CDB and Its Parameters

6.50.2.1 The CDB

The WRITE (10) CDB is shown in Table 573.

Table 573. WRITE (10) CDB

Bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code (2Ah)							
1	Reserved			DPO	FUA	Reserved	TSR	RelAdr
2	(MSB)							

3	Logical Block Address	
4		
5		(LSB)
6	Reserved	
7	(MSB)	Transfer Length
8		(LSB)
9	Control	

6.50.2.3 TSR

Timely Safe Recording (TSR) bit, set to one, indicates during phase one that the Logical Unit shall detect and report defective writable units within the Error reporting threshold set in Read/Write Error Detection and Recovery Parameters Mode Page (page code 01h). The Logical Unit may perform certify before write or may perform verification after write or both or another method of error detection but shall ensure error detection is performed. The same bit, set to one, indicates also that replacement due to defect shall **not** be perform at this time – AWRE (Automatic Write Reallocation Enabled) and Write Retry Count settings from Read/Write Error Detection and Recovery mode page shall be ignored – no automatic reallocation and no write retry is allowed. The host may perform writing with TSR bit set to one, and then may repeat the writing of signaled defective writable units with TSR bit set to zero (rewritable media) or one (write-once media). For best performance, the Logical Unit may remember the defective writable units after reporting them to the host in order to avoid the work of detection if the host writes again this particular writable unit (with or without TSR set to one). For Write-Once media during this phase one, the LBA in CDB shall match an unrecorded LBA. Combination of Pseudo-Overwrite and TSR in a single write command is not permitted.

TSR bit set to one indicates during phase two that the Logical Unit shall perform hardware defect management. This is for the sole use on write once media. During this phase, the LBA in CDB shall match a recorded LBA. Additionally, the Logical Unit shall ensure the LBA matches a DFL entry or a defect found during phase one (if not, the write command shall be terminated with CHECK CONDITION status and SK/ASC/ASCQ values shall be set to ILLEGAL REQUEST/INVALID FIELD IN CDB). The data shall be written by the Logical Unit to the spare area and the DFL shall be updated to reflect this remapping, as if the Logical Unit was performing a defect management for this block.

See 4.7.3.0 to distinguish phase one and two on write once media.

If TSR bit is set to one and if the TSR is not present or not current, the Logical Unit shall terminate the command with CHECK CONDITON status and SK/ASC/ASCQ values shall be set to ILLEGAL REQUEST/INVALID FIELD IN CDB.

If the LBA and transfer length is not matching ECC block first byte and ECC block end, and TSR bit is set to one, the Logical Unit shall fail the command with check condition and SK/ASC/ASCQ values shall be set to ILLEGAL REQUEST/INVALID FIELD IN CDB.

When TSR bit is set to zero, no change to the behavior of the command is to be performed. However for rewritable media, if TSR is set to zero, and if the writable unit was detected as defective during the execution of an earlier write command with TSR set to one, the Logical Unit may perform replacement immediately, without first attempting to record the known-as-defective writable unit.

FUA and TSR bits are not mutually exclusive. If both FUA and TSR bits are set to one during the phase one of TSR, the Logical Unit shall perform the error detection prior to returning GOOD status. In case a defect is detected, it shall be reported as CHECK CONDITION and sense bytes SK/ASC/ASCQ WRITE ERROR. RECOVERY NEEDED immediately and shall not be reported as deferred error.

6.50.2.3 DPO

Disable Page Out (DPO) is not used by MM Logical Units and shall be set to zero.

[…]

6.50.3 Command Execution

[…] Added at the end of 6.50.3:

In case of TSR bit set to one during phase one, when TSR recording method Feature (0042h) is current and if a defect is found for the writable unit being written, the Logical Unit shall terminate the command with CHECK CONDITION status and sense bytes SK/ASC/ASCQ shall be set to WRITE ERROR RECOVERY NEEDED within the error reporting threshold set through Read/Write Error Detection and Recovery mode page. Both errors found during writing and errors found during verify shall be reported with this error code. Data in buffer for non defective writable unit(s) shall be written on the medium normally. In other words, data in buffer for other writable unit(s) than the writable unit reported as defective shall be written, or if eventually the other writable unit(s) is found defective, they shall be equally reported as defective. If this CHECK CONDITION with said sense bytes is returned, the host shall read the defect information using GET PERFORMANCE command with Type=02h (Defect Status data).
Reporting of non-manageable defects such as incompatible media for write are unchanged by TSR bit.

[…]

6.51 WRITE (12) Command

[…]

6.51.2 The CDB and Its Parameters

6.51.2.1 The CDB

The WRITE (12) CDB is shown in Table 577.

Table 577. WRITE (12) CDB

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (AAh)							
1	Reserved			Reserved	FUA	Reserved	TSR	Reserved
2	(MSB)							
3	Logical Block Address							
4								
5								(LSB)
6	(MSB)							
7	Transfer Length							
8								
9								(LSB)
10	Streaming	Reserved						
11	Control							

6.51.2.2 TSR

See 6.50.2.3 TSR for a description of TSR bit.

Notice that TSR and Streaming bits are not mutually exclusive. When both bits are set to one, the Logical Unit shall perform stream write with error detection and report but no replacement if a defect is found. If insufficient time is available to perform error detection given the data rate streaming requirement set by the host through an earlier SET STREAMING Command, and given the Error reporting threshold set by the host through an earlier MODE SELECT on Read/Write Error Detection and Recovery Parameters Mode Page, the command is terminated with CHECK CONDITION status due to a timeout, sense bytes SK/ASC/ASCQ shall be set to ILLEGAL REQUEST/INSUFFICIENT TIME FOR OPERATION.
With TSR and Streaming bits combination, the host software will have a guaranteed average streaming speed, but has to expect the write to be done by burst by the logical unit. Hence the host software has buffer data between bursts (while logical unit is detecting potential errors),

6.51.2.3 FUA

[…]

6.52 WRITE AND VERIFY (10) Command

[…]

6.52.2 The CDB and Its Parameters

6.52.2.1 The CDB

The WRITE AND VERIFY (10) CDB is shown in Table 580.

Table 580. WRITE AND VERIFY (10) CDB

Bit Byte	7	6	5	4	3	2	1	0
0	Operation Code (2Eh)							
1	Reserved						TSR	Reserved
2	(MSB)							
3	Starting Logical Block Address							
4								
5									(LSB)
6	Reserved								
7	(MSB) Transfer Length								
8									(LSB)
9	Control								

6.52.2.2 TSR

See 6.50.2.3 TSR for a description of TSR bit.

The verification enforced by this command may be considerate by the Logical Unit as sufficient error detection and no additional error detection work is requested.

6.52.2.3 Starting Logical Block Address

[…]

7.2   Read/Write Error Detection and Recovery Parameters Mode Page (Page Code 01h)

7.2.1   Introduction

The Read/Write Error Detection and Recovery Parameters Mode Page (Table 589) specifies the error detection and recovery parameters the Logical Unit shall use during any command that performs a data read or write operation from the media (e.g. READ, READ CD, WRITE, etc.).

Table 588 shows the Features associated with the Read/Write Error Detection and Recovery Mode Page.

Table 588. Features Associated with the READ/WRITE Error Detection and Recovery Mode Page

Feature Number	Feature Name	Requirement
0010h	Random Readable	Mandatory when PP bit is 1.
0020h	Random Writable	Mandatory when PP bit is 1.
0024h	Hardware Defect Management	Mandatory
0025h	Write Once	Mandatory when PP bit is 1.
0029h	Enhanced Defect Reporting	Mandatory
0042h	TSR	Mandatory

7.2.2 The Mode Page and its Parameters

7.2.2.1 The Mode Page

Table 589. Read/Write Error Detection and Recovery Parameters Mode Page Format

Bit Byte	7	6	5	4	3	2	1	0
0	PS	Reserved	Page Code (01h)					
1	Page Length (0Bh)							
2	Error Recovery Behavior							
	AWRE	ARRE	TB	RC	Reserved	PER	DTE	DCR
3	Read Retry Count							
4	Reserved							
5	Reserved							
6	Reserved							
7	Reserved							EMCDR
8	Write Retry Count							
9	(MSB)							
10	Error reporting threshold length							
11	(count of logical block)							
12								(LSB)

7.2.2.2 PS
The Parameters Savable (PS) bit is defined in 7.1.4.1.

7.2.2.3 Page Code
The Page Code field shall be set to 01h, identifying the Read/Write Error Detection and Recovery Parameters Mode Page.

7.2.2.4 Page Length
The Page Length shall be set to 0Bh.

7.2.2.5 Error Recovery Behavior
7.2.2.5.1 Automatic Write Reallocation Enabled (AWRE)
The Automatic Write Reallocation Enabled bit (AWRE) shall be ignored when the Current bit of the Defect Management Feature descriptor is set to zero.
If AWRE is set to one, the Logical Unit shall enable automatic reallocation of defective blocks during write operations. If AWRE bit is set to zero, the Logical Unit shall not perform automatic reallocation of defective data blocks during write operations. If the media format is MRW, the default value for AWRE is one (1b). Error reporting as required by the error recovery bits (EER, PER, DTE, and DCR) shall be performed only after completion of the reallocation.
The Automatic Read Reallocation Enabled bit (ARRE) shall be ignored when the Current bit of the Defect Management Feature descriptor is set to zero.

7.2.2.5.2 Automatic Read Reallocation Enabled (ARRE)
If the Automatic Read Reallocation Enabled bit (ARRE) is set to one, the Logical Unit shall enable automatic reallocation of defective data blocks during read operations. If ARRE is set to zero, the Logical Unit shall not perform automatic reallocation of defective data blocks during read operations.
All error recovery actions required by the error recovery bits (TB, EER, PER, DTE, and DCR) shall be processed. The automatic reallocation shall then be performed only if the Logical Unit successfully recovers the data. Error reporting as required by the error recovery bits shall be performed only after completion of the reallocation. The reallocation process shall present any failures that occur. When ARRE is set to one, DCR and RC shall be each set to zero. When media formatted as MRW is detected, the value of ARRE shall default to zero. When DVD+RW

media with the Basic Format is detected, ARRE and AWRE shall default to zero and is unable to be set to one by the Initiator.

[…]

7.2.2.8 Write Retry Count
The Write Retry Count field specifies the number of times that the Logical Unit shall attempt its write recovery algorithm.

7.2.2.9 Error Reporting Threshold Length
The Error Reporting Threshold Length field specifies the threshold length for error reporting. It is a count of logical blocks. A defect found during the execution of a write command, or read command, or verification of a writable unit including the LBA of the previously mentioned write command, shall be reported before or when this count of logical block has been transmitted by the host through write commands. The defect may be reported earlier but shall not be reported later. If a write command would cause the count of logical block to be exceeded and a defect has already been found but not reported, the write command shall be terminated with CHECK CONDITION status and sense bytes SK/ASC/ASCQ shall be set to (new) 02 04 09 LOGICAL UNIT NOT READY, THRESHOLD CONDITION MET. The host shall issue again the write command that did cause the count of logical block to be exceeded after reading the defect information from the Logical Unit using GET PERFORMANCE command with Type=02h (Defect Status data). If a write command would cause the count of logical block to be exceeded but writing or verification of buffered write commands has not been performed, the write command shall be terminated with CHECK CONDITION status and sense bytes SK/ASC/ASCQ shall be set to 02 04 08 LOGICAL UNIT NOT READY, LONG WRITE IN PROGRESS. The Logical Unit shall then proceed with cache writing and or verification[D.B.1]. ~~If a write command buffer is larger than the agreed threshold, the command shall be terminated with CHECK CONDITION and sense bytes SK/ASC/ASCQ shall be set to 05 24 00 INVALID FIELD IN CDB.~~

A value of 0h means that TSR method is not supported ~~or that no threshold is supported~~. If TSR ~~/ Nero recording~~ method is supported, ~~it is recommended for performance purposes that~~ the threshold ~~is supported and that its~~'s length ~~is~~ shall be ~~at least as big as~~strictly bigger than the buffer ~~of~~ reported by the Logical Unit to READ BUFFER CAPACITY. A threshold length which allows enough delay between the write pass and the verify pass so that write to verify and verify to write transition time is negligible compared to the write time for the threshold length is recommended. If the Logical Unit does not support interruption of verify pass during phase one to proceed incoming commands, it should not allow a threshold length longer than what it can verify without causing a timeout.

The host may keep the default threshold length or may increase or decrease the threshold length by MODE SELECT. If the value set by the host is not supported, it shall be rounded by the LOGICAL UNIT to the nearest smaller threshold supported. The host shall check the selected value using MODE SENSE.

The host shall not change the error reporting threshold during phase one. The logical unit shall fail, with CHECK CONDITION and sense bytes SK/ASC/ASCQ shall be set to ILLEGAL REQUEST/ COMMAND SEQUENCE ERROR, any change attempt after the first TSR write has been issued and when no synchronize cache command has yet being issued to signal the end of the phase.