To: T10 Technical Committee

From: Bill Bissonette (Bill.Bissonette@intel.com)
Date: February 17, 2005
Subject: 05-077r0 SAS-1.1 SAS-SATA OOB Algorithm Summary

Revision history

Revision 0 (February 16, 2005) First revision

Related documents

SAS-1.1r8

SATA 1.0a

SATA II Electrical spec

Overview

This paper is an expository on the realities of the SAS OOB algorithm described in SAS-1.1r8 section 5.3.7.5. In particular, it describes the scenarios in which a SATA drive will be exposed to SAS-level OOB bursts then describes the electrical realities of such. Finally, it calls for a response from the SATA disk drive suppliers to help the SAS Phy TWG determine whether this is indeed a problem that needs to be addressed with changes to the SAS-1.1 specification.

SAS-SATA OOB 'Toggling' Algorithm

SAS-1.1 working draft currently specifies an OOB algorithm as follows:

> **5.3.7.5 Transmitter device signal output levels for OOB signals**
>
> Transmitter devices supporting being attached to SATA devices shall use SATA 1.0 signal levels (see ATA/ATAPI-7 V3) during the first OOB sequence after a power on or hard reset if the 1,5 Gbps transfer ate is supported. As soon as COMSAS has been exchanged, the transmitter device shall increase its transmit levels to the SAS voltage levels specified in table 32 (see 5.3.7) and table 33 (see 5.3.7.3). If a COMINIT is not received within a hot-plug timeout at SATA 1.0 signal levels, the transmitter device shall increase its transmit levels to the SAS voltage levels and perform the OOB sequence again. If no COMINIT is received within a hot-plug timeout of the second OOB sequence the transmitter device shall initiate another OOB sequence using SATA 1.0 signal levels. The transmitter device shall continue alternating between sending COMINIT at SATA 1.0 signal levels and SAS signal levels until a COMINIT is received. If the OOB sequence is completed at the SAS voltage level and a SATA device is detected rather than a SAS target device, the transmitter device shall switch to SATA 1.0 voltage levels and repeat the OOB sequence.
>
> If the OOB sequence is completed at the SAS voltage level and a SATA device is detected rather than a SAS target device, the transmitter device shall switch to SATA 1.0 voltage levels and repeat the OOB sequence.

Figure 1: SAS-1.1r8 SAS-SATA OOB text

OOB scenarios for SATA drives in a SAS system

If a SATA drive is already installed in a system when the power is applied or when the system experiences a reset sequence, there is little probability that SATA drive will be exposed to a SAS amplitude OOB sequence since it will respond to the first COMINIT (interpreted by the SATA drive as a COMRESET) with a COMINIT which will, in turn, cause the expander or initiator to maintain SATA OOB levels from there on out (until the next hard reset or power cycle). See Figure 2.

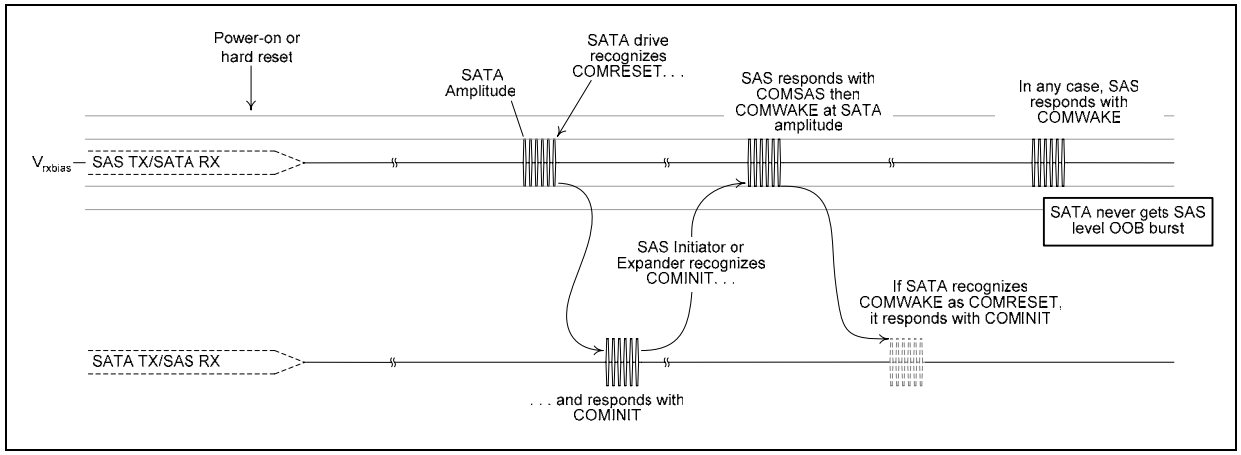

Figure 2: The "normal" scenario

After a power-on or hard reset event, if the SATA drive is not initialized before the SAS Expander or Initiator has issued the first COMINIT at SATA levels, the SATA drive will be exposed to a SAS-level COMINIT as shown in Figures 3 & 4. The SATA drive may or may not recognize the SAS-level COMINIT but the subsequent sequence is the same for either case. It is also possible in these cases that the RX termination is turned off for some time after the reset. A high impedance termination **could** cause an amplification of the received signal level. ***Is this valid?***

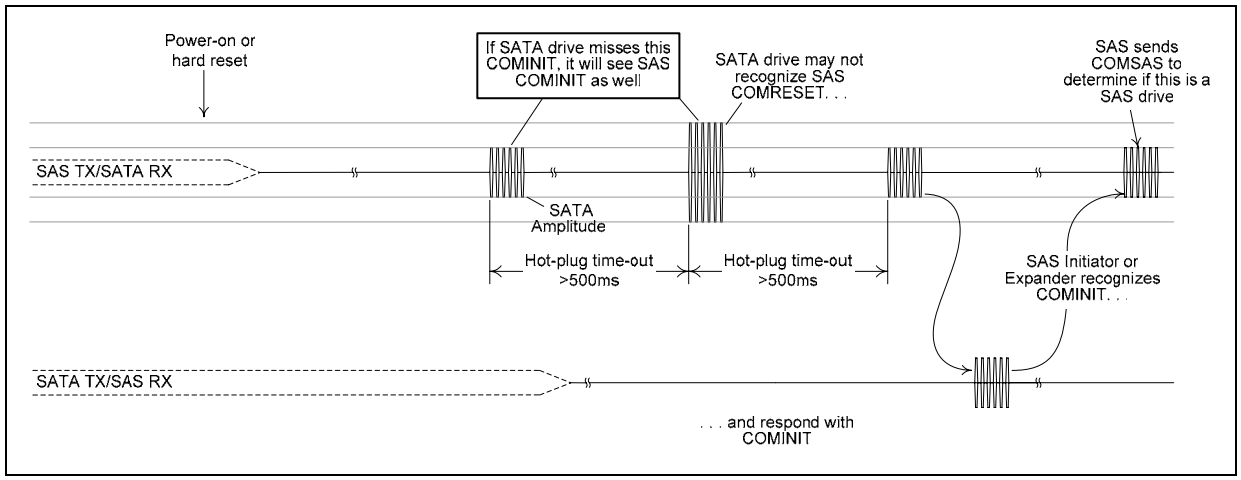

Figure 3: SATA drive wakes up too late, doesn't recognize SAS-level COMINIT

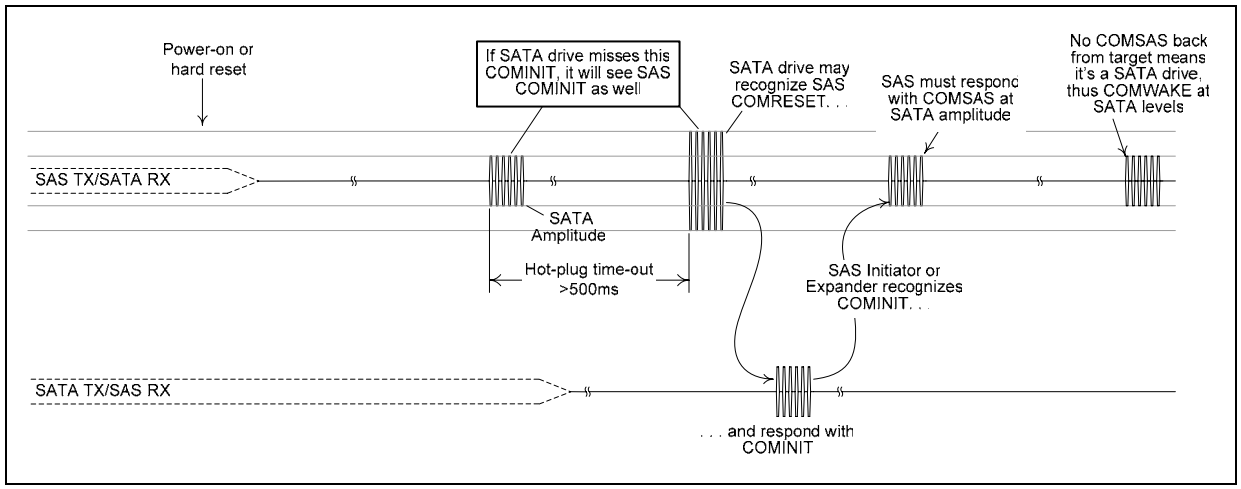

Figure 4: SATA drive recognizes SAS-level COMINIT

As shown in figure 5, a SATA drive that is 'hot-plugged' into a backplane has a significant likelihood (on the order of 50%) of exposure to a SAS-amplitude COMINIT.

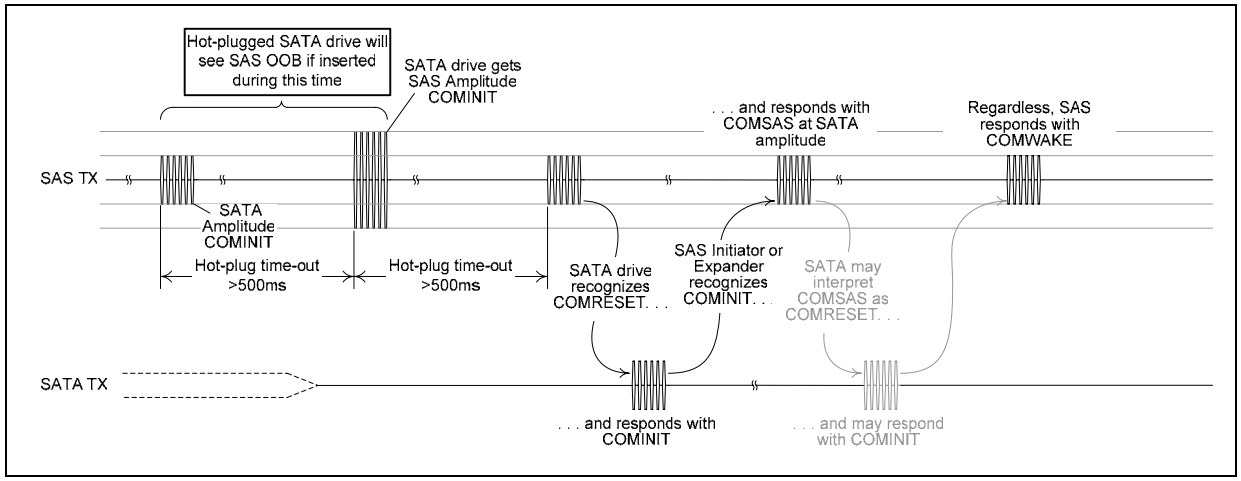

Figure 5: SATA drive hot-plugged

Voltage Considerations at the Receiver

Proposal T10 05-019 proposes that all OOB sequences from initiators and expanders that support SATA be transmitted at SATA amplitudes. There is concern from SAS drive suppliers that SAS devices may fail to detect SATA-level OOBs. And there are existing, shipping SAS-1.0 and SAS-1.1 initiator and expander devices that have implemented the OOB toggling algorithm and implementation of such a change to the OOB algorithm would cause design changes. The outstanding question has become: ***Is there a risk that SAS level OOB bursts will damage a SATA drive or cause the drive to fail an OOB initialization sequence?***

The SATA II electrical specification states that the maximum differential amplitude at the receiver is 600mV maximum for Gen1i and 750mV maximum for Gen2i. These are operational specifications and the 'absolute maximum' amplitudes are not specified (***are they***?).

It has been stated by SAS Phy TWG members that some SAS expanders or initiators DO transmit at nearly 1600mV.

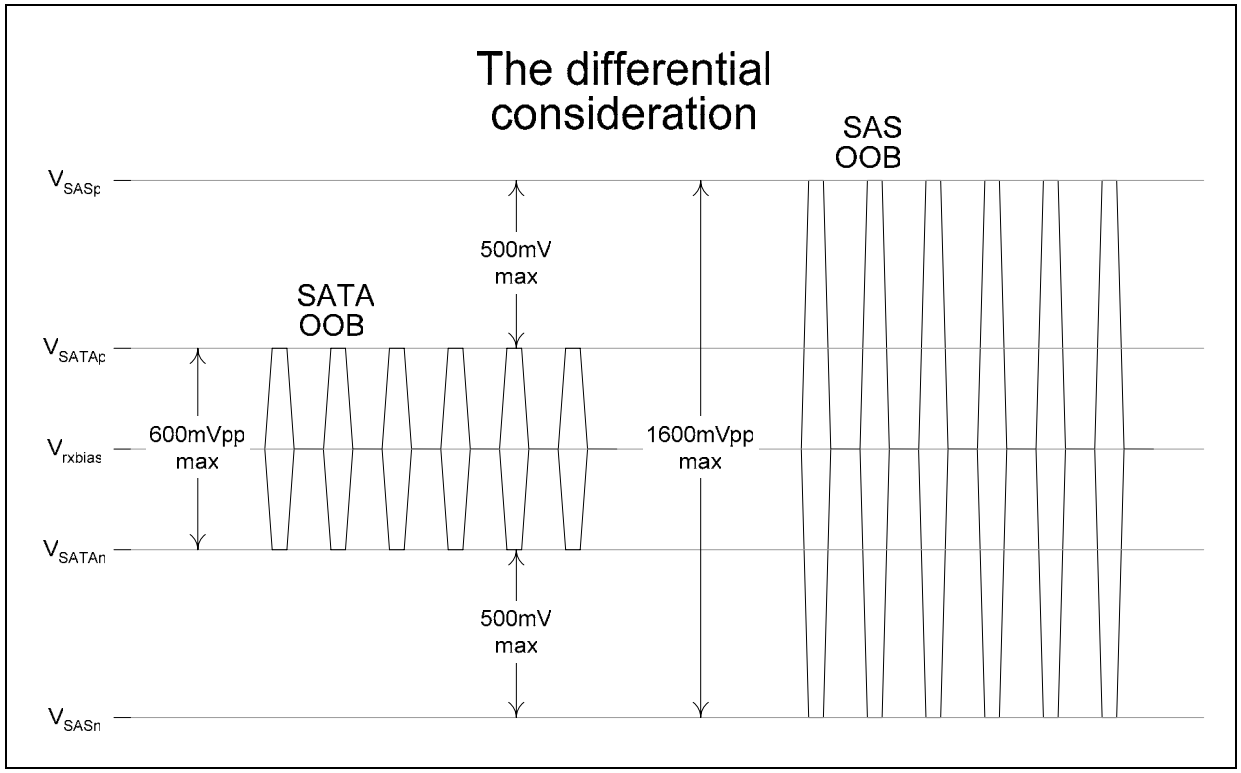

Figure 6: Differential Amplitude Case

Figure 6 illustrates worst-case SATA Gen1i and SAS level OOB bursts as seen by a SATA drive receiver. The individual voltages within the burst are not shown, but rather the burst envelopes for a COMINIT burst sequence. The differential amplitude beyond the maximum Gen1i specification is 1000mV. ***Will***

this cause any damage or cause the SATA OOB detection circuitry to miss a subsequent (500ms later) SATA level OOB burst?

Concern: The receiver FETs will saturate.

Discussion: SATA spec requires 3us max recovery time from "transient" event. SAS spec requires at least 500ms (hot plug time-out) before next COMINIT which is >100,000 times longer that required. Receiver has plenty of time to recover before next COMINIT. ***Does this apply?***

SAS transmitter IS AC coupled and RX bias will settle well before the next OOB burst (when SAS TX launch amplitudes are adjusted within the 500ms hot-plug time-out).

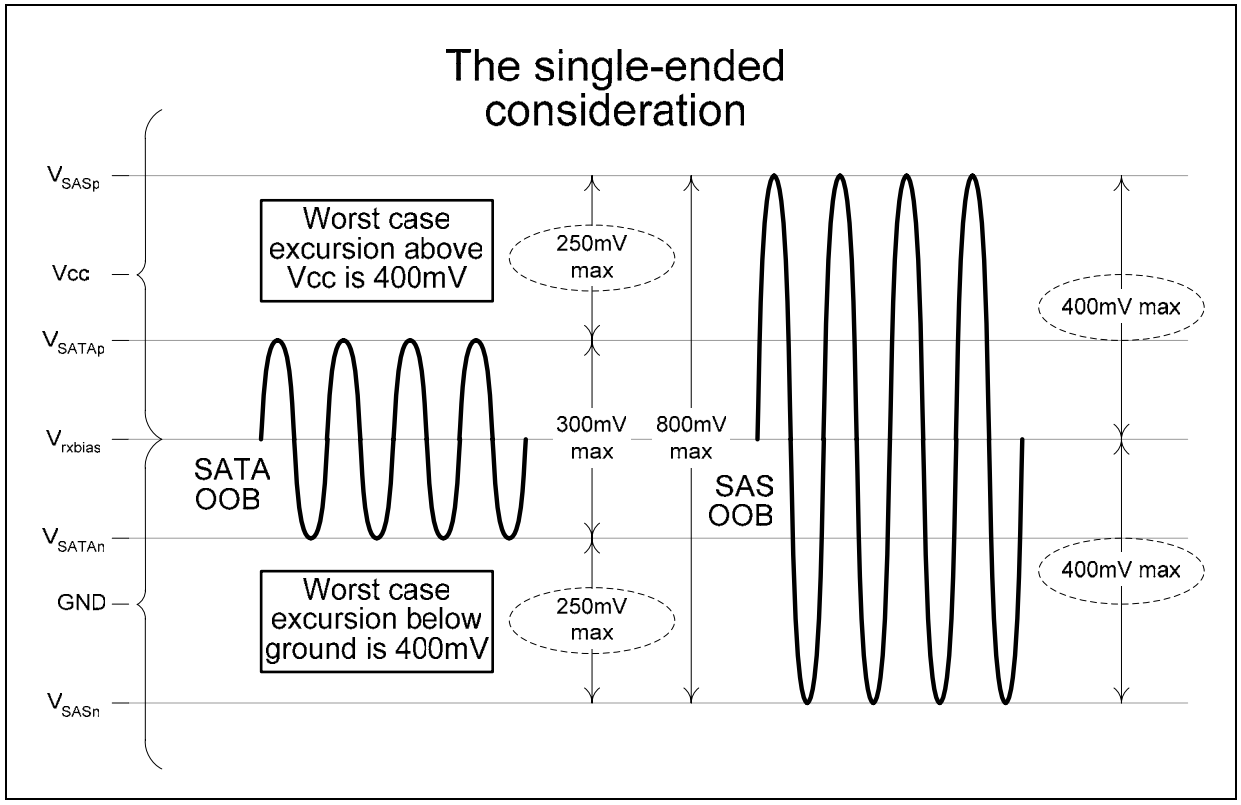

Figure 7: Single-ended Amplitude Case

Figure 7 illustrates the single-ended voltages as seen by either the RXn or RXp inputs on a SATA drive for the SATA and SAS level OOBs. The actual amplitude excursion beyond the maximum SATA Gen1i specification is 250mV maximum, with a 400mV maximum excursion above and below the RX bias voltage. Note that V_{RXbias} can be any voltage between GND and Vcc on the drive, depending on the design of the receiver circuitry and, in particular, the voltage that the receiver termination resistors are tied to.

Concern: Excursions below ground or above the power supply rail may cause ESD diodes to conduct and, over time, this would damage the receiver. ***Is this a realistic scenario?***

Discussion: V_{RXbias} can be anywhere between Vcc and GND. Excursions are no more than 400mV above power rail or 400mV below ground. ESD forward bias voltages are typically greater than 400mV, so this scenario is not a likely.

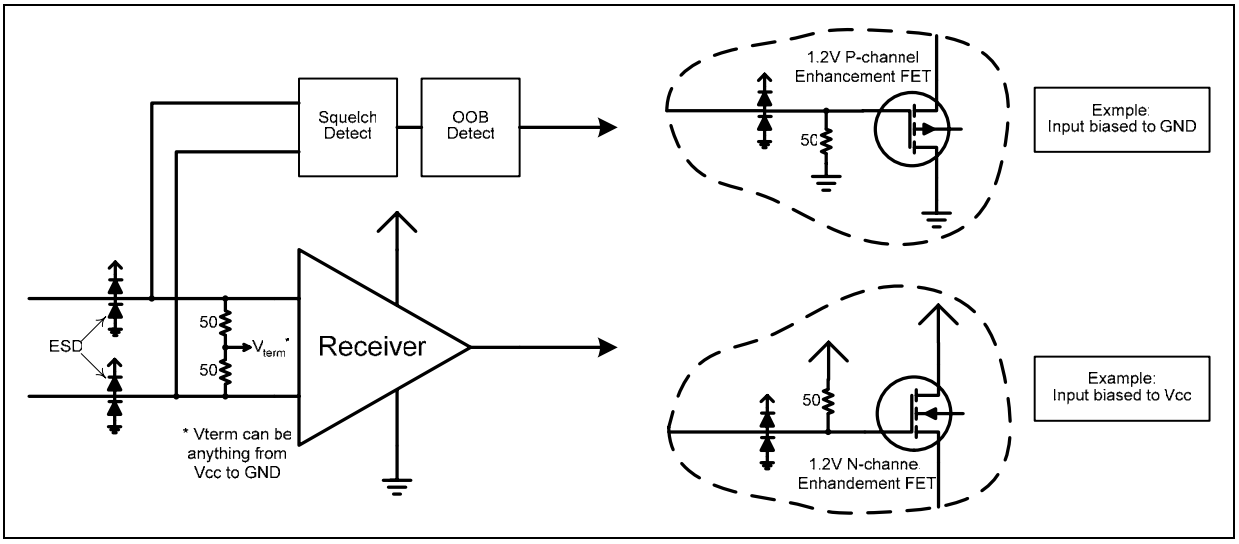

Figure 8: SATA receiver diagram and possible input FET configurations

Figure 8 has been added to this document only as a reference diagram for possible discussion around this subject. It is NOT intended to reflect any supplier's particular receiver implementation and, more than that, is not an indication that the author thinks he knows anything about the subject.

The circuit examples showing FETs is an attempt to visualize a possible worst-case input structure for single-ended input voltage excursions. It is assumed in those diagrams that these MOS gates are good to 1.2V (V_{GS} or V_{GD}) reflecting the low end of current Si processes used for high-speed mixed signal circuits.

Other considerations not treated here

In a hot-plug scenario, there may be the additional factor of transients that can act as additive to the OOB burst amplitudes – particularly in a single-ended sense. The whole transient concern is a hot topic in both the SAS and SATA phy working groups. Can the additive effects of the SAS OOB signaling be dealt with in those transient discussion instead of over-complicating this SAS OOB algorithm issue?

Conclusion and call for assistance from SATA Phy TF members

SATA drives, particularly in hot-plug scenarios, will be exposed to SAS level OOB bursts. SAS system suppliers depend in part on the very attractive SATA support feature. It is a feature that is demonstrating market acceptance and will cause market pull for SATA drives in the enterprise and SMB markets. The T10 technical committee intends to release SAS-1.1 to letter ballot shortly after the March 7-11 plenary week and humbly requests the assistance of the SATA phy WG and SATA drive supplier representatives to help resolve this issue in the interest of a robust SAS and SATA-in-the-enterprise deployment this year.

Thanks!