To: T10 Technical Committee
From: Mark A. Overby (moverby@nvidia.com), nVidia Corporation
Date: 10 November 2004
Subject: T10/04-397 SAT protocol specific port mode page

Revision History

Revision	Date	Author	Revision Notes
0	10 November 2004	Mark Overby	Initial draft

Related Documents

SPC-3 (1416D r21a)
SAT (1711D r1)

Overview

In order to successfully communicate with ATA drives certain timing mode parameters must be set on both the device and the host. For serial ATA environments, speed negotiation happens automatically at the PHY layer. However, for parallel ATA it is the responsibility of the host to correctly initialize both the device and the host for the appropriate DMA and/or PIO timing modes.

In the T10 SCSI architecture model there is no current mechanism that models the necessary communication that the ATA host undergoes in a traditional ATA-only environment. This proposal addresses this need for SATL's that need to deal with ATA hosts to set and maintain timing modes. It also gives the application client an opportunity to control physical data transfer rates for diagnostic, test, error handling, or other environmental-specific reasons.

Proposed Changes

Annex D.6 in SPC-3 (r21a), Table D.12

- Add entries for mode page 19h, new sub page codes 1h and 2h. These mode pages would correspond to a protocol specific port entry for parallel and serial ATA respectively.
- Add a new column to this table that indicates these mode pages are only used in the context of SAT. Recommend a new column with a header of S that references SAT 1.0 (1711D).

SAT 1.0 (1711D r1)

- Move current section 10.3 to 10.4
- Create new section 10.3 entitled SCSI – ATA Translation Specific Mode Pages. The wording style below is purely suggestive and the editor should edit the content as necessary to conform to the style of the SAT document.

10.3 SCSI – ATA Translation Specific Mode Pages

This section describes mode pages that the SATL may implement that are unique to the SCSI – ATA translation environment. These mode pages are for use by the SATL and are shown in Table 1 and described in this section. A SATL may support zero, one, or both of the mode pages described in this section. A SATL should support the appropriate mode page for the attached ATA environment (e.g. Serial ATA).

Table 1 SCSI - ATA Translation Specific Mode Pages

Mode Page		
Page Code	**Sub Page Code**	**Page Name**
19h	01h	Parallel ATA Port Specific Page
19h	02h	Serial ATA Port Specific Page

10.3.1 Parallel ATA Port Specific Page (Page 19h, Sub Page 01h)

The Parallel ATA Port Specific mode page provides parallel ATA specific controls for a SATL to configure the ATA host as well as understand what parameters are communicated to the ATA device to ensure proper communication for specific transfer rates. This mode page uses the sub_page format as described in SPC. The protocol mode page itself is described in SPC-3. This document describes the protocol specific mode parameters that are provided for this page. See Table 2 for the format of this mode page.

SATL implementations that support the attachment of parallel ATA devices shall support this mode page when requested through mode sense. SATL implementations should allow application clients to configure alternate parallel ATA timings through mode select using this mode page.

Table 2 Parallel ATA Port Specific Mode Page

Bit / Byte	7	6	5	4	3	2	1	0
0	PS	SPF(1b)	PAGE CODE (19H)					
1	SUBPAGE CODE (01H)							
2	(MSB)	PAGE LENGTH						
3								(LSB)
4	RESERVED							
5	RESERVED				PROTOCOL IDENTIFIER (08H)			
6	RESERVED		PIO4A	PIO3A	RESERVED		PIO4S	PIO3S
7	RESERVED	MWD2A	MWD1A	MWD0A	RESERVED	MWD2S	MWD1S	MWD0S
8	RESERVED	UDMA6S	UDMA5S	UDMA4S	UDMA3S	UDMA2S	UDMA1S	UDMA0S
9	RESERVED	UDMA6A	UDMA5A	UDMA4A	UDMA3A	UDMA2A	UDMA1A	UDMA0A

For the behavior and meaning of the PS bit, see clause 7.4.5 of SPC-3. SATL implementations may save the state of the timing parameters defined in this mode page. However SATL implementations shall not use any saved parameters to configure the ATA host timing modes into an illegal configuration for the attached device.

PIO3S shall be set to 1 by the SATL when the ATA device IDENTIFY DEVICE data word 64; bit 0 is set to 1. This bit, when set, indicates that the device supports PIO mode 3. PIO4S shall be set to 1 by the SATL when the ATA device IDENTIFY DEVICE data word 64, bit 1 is set to 1 and the ATA host supports transfers as PIO mode 4. This bit, when set, indicates that the attachment environment supports PIO mode 4. These fields shall be treated as reserved for MODE SELECT with this mode page. These fields are collectively referred to as the PIO supported fields.

For a MODE SENSE command, PIO3A shall be set to 1 by the SATL when the ATA host is configured to use mode 3 PIO transfers. If PIO3A is set to 1, PIO4A shall be 0. PIO4A shall be set to 1 by the SATL when the ATA host is configured to use mode 4 PIO transfers. If PIO4A is set to 1, PIO3A shall be zero. For MODE SELECT, the application client sets this bit to indicate to the SATL that PIO mode 3 transfers are requested when a command using the ATA PIO protocol is transmitted. These fields are collectively referred to as the PIO active fields.

When the SATL receives a MODE SELECT command and the PIO active field indicates a change from the current setting, the SATL shall configure the host to use the new PIO transfer rate, if supported. The application client shall not request a PIO mode setting that the ATA device cannot support and the SATL shall generate an appropriate error if the application client attempts such an operation.

MWD0S, MWD1S, and MWD2S are collectively referred to as the multiword DMA (MWDMA) supported fields. MWD0S shall be set to 1 by the SATL when the ATA device IDENTIFY DEVICE data word 63, bit 0 is 1 and the ATA host supports multiword mode 0. MWD1S shall be set to 1 by the SATL when the ATA device IDENTIFY DEVICE data word 63, bit 1 is 1 and the ATA host supports multiword DMA mode 1. MWD2S shall be set to 1 by the SATL when the ATA device IDENTIFY DEVICE data word 63, bit 2 is 1 and the ATA host supports multiword DMA mode 2. Only one of the multiword DMA supported fields shall be 1 during any MODE SENSE request. If any of these fields are set, the remaining fields shall be 0. These fields are reserved for MODE SELECT requests.

MWD0A, MWD1A, and MWD2A are collectively referred to as the MWDMA active fields. MWD0A shall be set to 1 by the SATL when the host and device are configured to use multiword DMA mode 0. MWD1A shall be set to 1 by the SATL when the host and device are configured to use multiword DMA mode1. MWD2A shall be set to 1 by the SATL when the host and device are configured to use multiword DMA mode 2.

When the SATL receives a MODE SELECT command and the MWDMA active field indicates a change from the current settings, the SATL shall issue a SET FEATURES command, sub-command code 03h (Set Transfer Mode), to the ATA device. If the SET FEATURES command completes without error, the SATL shall then configure the ATA host to use the new MWDMA timing mode for DMA operations. If the SET FEATURES command completes with an error, the SATL shall generate a CHECK CONDITION with a sense key of HARDWARE ERROR with an additional sense key of LOGICAL UNIT DOES NOT RESPOND TO SELECTION (05h). Application clients shall not request a timing mode that is not reported as being supported in this environment and the SATL shall generate an appropriate error if the application client attempts such an operation.

UDMA0S, UDMA1S, UDMA2S, UDMA3S, UDMA4S, UDMA5S, AND UDMA6S are collectively referred to as the Ultra DMA (UDMA) supported fields. The SATL shall determine the highest UDMA supported as being the lower of the ATA host maximum transfer mode and the device maximum transfer mode. The device reports the UDMA transfer mode from the IDENTIFY DATA, word 88, bits 6:0. The UDMA supported fields shall be set as defined in Table 3.

Table 3 UDMA Supported Field Requirements

Highest UDMA supported[1]	UDMA0S	UDMA1S	UDMA2S	UMDA3S	UMDA4S	UMDA5S	UDMA6S
UDMA unsupported	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0
2	1	1	1	0	0	0	0
3	1	1	1	1	0	0	0
4	1	1	1	1	1	0	0
5	1	1	1	1	1	1	0
6	1	1	1	1	1	1	1

[1] The highest UDMA supported is the lowest supported speed of the device and host

UDMA0A, UDMA1A, UDMA2A, UDMA3A, UDMA4A, UDMA5A, AND UDMA6A are collectively referred to as the ultra DMA (UDMA) active fields. Only one of the UDMA active fields shall bet set to 1 at any time. See Table 4 for the meaning of each UDMA active field.

Table 4 UDMA Active Fields

UDMA Active Field	Description
UDMA0S	ATA host and device communicate using UDMA Mode 0
UDMA1S	ATA host and device communicate using UDMA Mode 1
UDMA2S	ATA host and device communicate using UDMA Mode 2
UDMA3S	ATA host and device communicate using UDMA Mode 3
UDMA4S	ATA host and device communicate using UDMA Mode 4
UDMA5S	ATA host and device communicate using UDMA Mode 5
UDMA6S	ATA host and device communicate using UDMA Mode 6

When the SATL receives a MODE SELECT command and the UDMA active field indicates a change in the requested UDMA speed in the communications interface. The SATL shall:

1. Issue a SET FEATURES, sub-command 03h, to set the UDMA timing mode on the device to the requested state.
2. Check the status of the SET FEATURES command once completed. If the command completes in error, the SATL shall not change any host timing modes and shall complete the MODE SELECT command with a CHECK CONDITION, sense key of HARDWARE ERROR, and additional sense code

of LOGICAL UNIT DOES NOT RESPOND TO SELECTION. The SATL shall take no further action regarding this timing mode request.

3. Configure the ATA host to communicate with the device at the requested UDMA timing speeds.
4. Complete the MODE SELECT command with the appropriate status code.

Application clients shall not request a timing mode that is not reported as being supported in this environment and the SATL shall generate an appropriate error if the application client attempts such an operation.

The MWDMA and UDMA active fields are mutually exclusive of each other. If a bit it set in a MWDMA active field, no UDMA active fields shall be set to 1. Likewise, if a UDMA active field is set to 1, no MWDMA active field shall be set to 1.

10.3.2 Serial ATA Port Specific Page (Page 19h, Subpage 02h)

The Serial ATA Port Specific mode page provides serial ATA specific controls for a SATL to configure or obtain status of the serial ATA link from the ATA host. This mode page uses the sub_page format as described in SPC-3. The protocol mode page itself is described in SPC-3. This document describes the protocol specific mode parameters that are provided for this page. See Table 5 for the format of this mode page.

Table 5 Serial ATA Port Specific Mode Page

Bit / Byte	7	6	5	4	3	2	1	0
0	PS	SPF(1b)	PAGE CODE (19H)					
1	SUBPAGE CODE (02H)							
2	(MSB)	PAGE LENGTH (H)						
3								(LSB)
4	RESERVED							
5	RESERVED				PROTOCOL IDENTIFIER (08H)			
6	RESERVED				NTFV	CNTRLV	ERRV	STATV
7	RESERVED							
8	(MSB)	SSTATUS						
11								(LSB)
12	(MSB)	SERROR						
15								(LSB)
16	(MSB)	SCONTROL						
19								(LSB)
20	(MSB)	SNOTIFICATION						
23								(LSB)
24		RESERVED						
64								

For the behavior and meaning of the PS bit, see clause 7.4.5 of SPC-3. SATL implementations may save the state of the timing parameters defined in this mode page.

For a MODE SENSE request STATV, ERRV, CNTRLV, and NTFV shall be set to 1 if the SSTATUS, SERROR, SCONTROL, and SNOTIFICATION fields, respectively, contain valid data. For a MODE SELECT command, these fields indicate if the SERROR, SCONTROL, and SNOTIFICATION fields contain values that shall be written, by the SATL, to the appropriate register(s) in the serial ATA host. The STATV and SSTATUS fields shall be set to 0 by the application client when issuing a MODE SELECT command for this mode page.

The SSTATUS field contains the serial ATA link status (SSTATUS) register as defined in ATA/ATAPI-7, volume 3.

The SERROR field contains the serial ATA error (SERROR) register as defined in ATA/ATAPI-7, volume 3.

The SCONTROL field contains the serial ATA link control (SCONTROL) register as defined in ATA/ATAPI-7, volume 3.

The SNOTIFICATION field contains the serial ATA command queuing notification register (SNOTIFICATION) as defined in the serial ATA specifications.