T10/04-378r1 SAS-1.1 Clarification of SATA Signaling Level Specification

To: T10 Technical Committee
From: Barry Olawsky, HP (barry.olawsky@hp.com)
Date: 17 January 2005
Subject: T10/04-378r1 SAS-1.1 Clarification of SATA Signaling Level Specification

Revision History
Revision 0 (8 November 2004) first revision
Revision 1 (17 January 2005) added analytical and simulation data

Related Documents
sas1r05 - Serial Attached SCSI 1.1 revision 5
03-240r1 - SAS-1.1 Merge IT and IR with XT and XR (Rob Elliott, Hewlett Packard)

Overview
Evaluate validity of SATA mode receiver sensitivity spec for XR and IR.

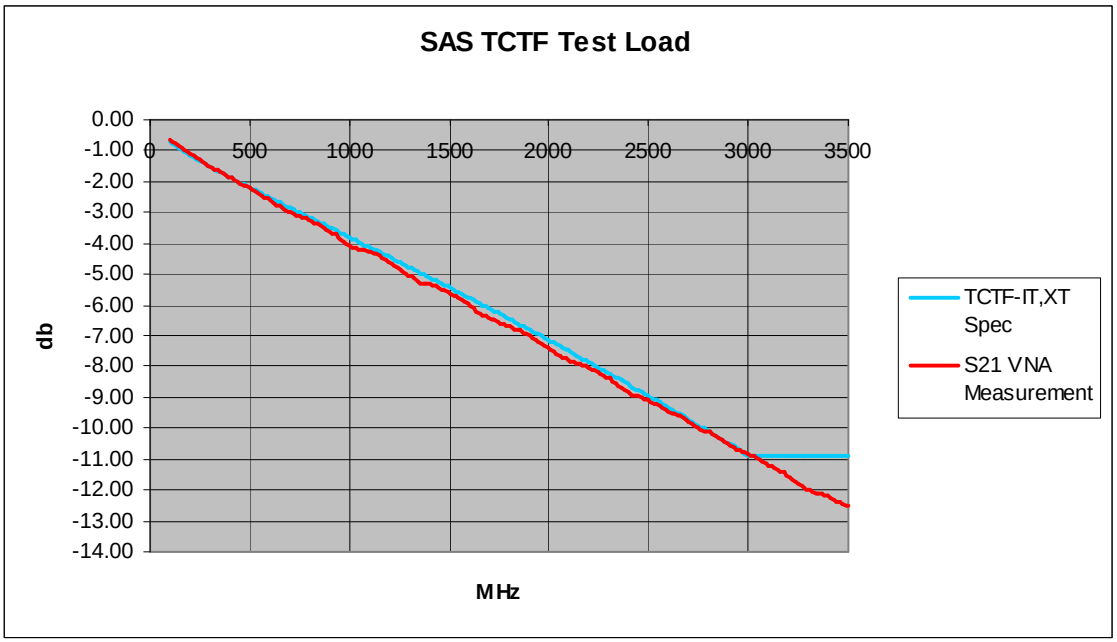
Proposed Changes
Add following note to table 30 referencing the 225mV cell in SATA column.

Amplitude measurement methodologies of Serial ATA and this standard differ. Under conditions of maximum rise/fall time and jitter, eye diagram methodologies may indicate far less amplitude than the technique specified by the Serial ATA standard. To compensate for this difference, it is recommended that Serial ATA devices used in SAS applications undergo additional testing. Eye-diagram tests should be used to confirm the minimum SATA device amplitude specified in the Serial ATA specification.

Supporting Information Only (NOT part of SAS-1.1 proposal):

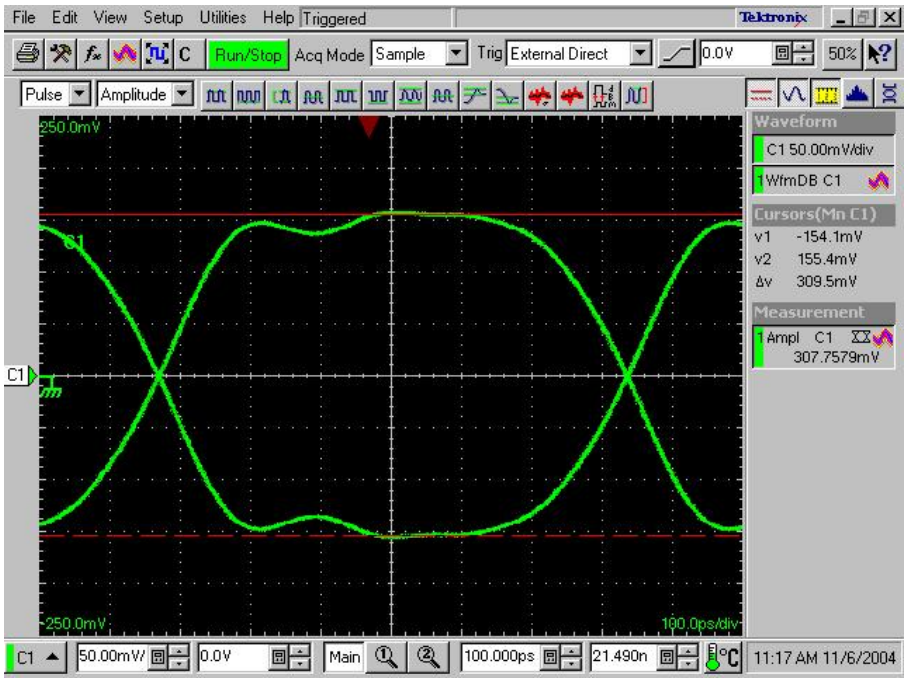
To evaluate the existing SATA mode receive output level specification, a TCTF test load for IT/XT was constructed. The amplitude was measured at the far end of the TCTF test load with a variety of transmitter and data pattern configurations as detailed below with each scope capture.

S21 of TCTF test load:



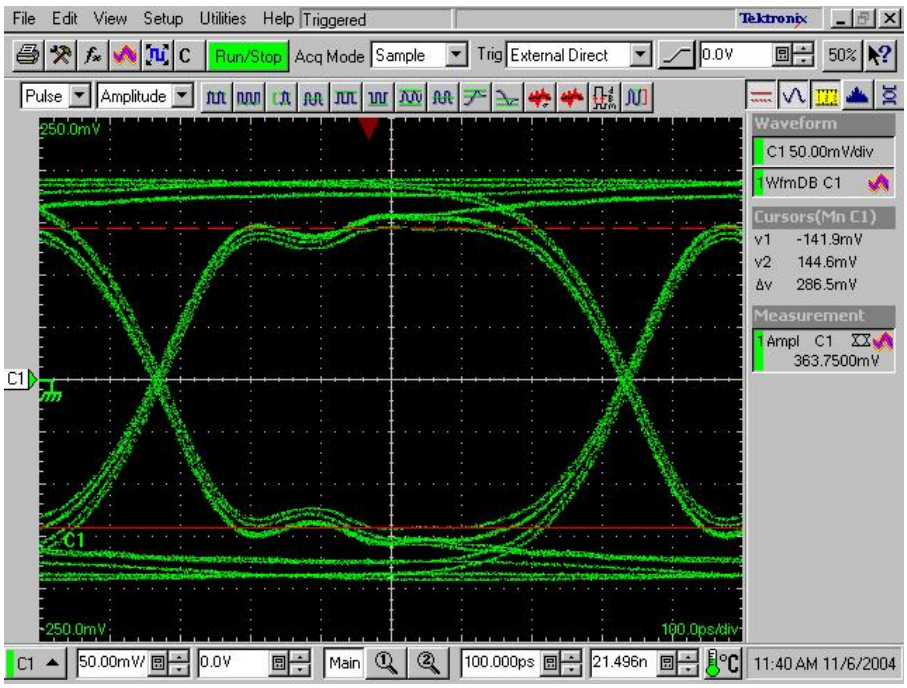
Vpp at receiver end of TCTF test load with

- D3186 pattern generator transmitting D10.2
- Vpp at transmitter of 400mVpp
- Measured amplitude of 310mVpp at scope terminated load



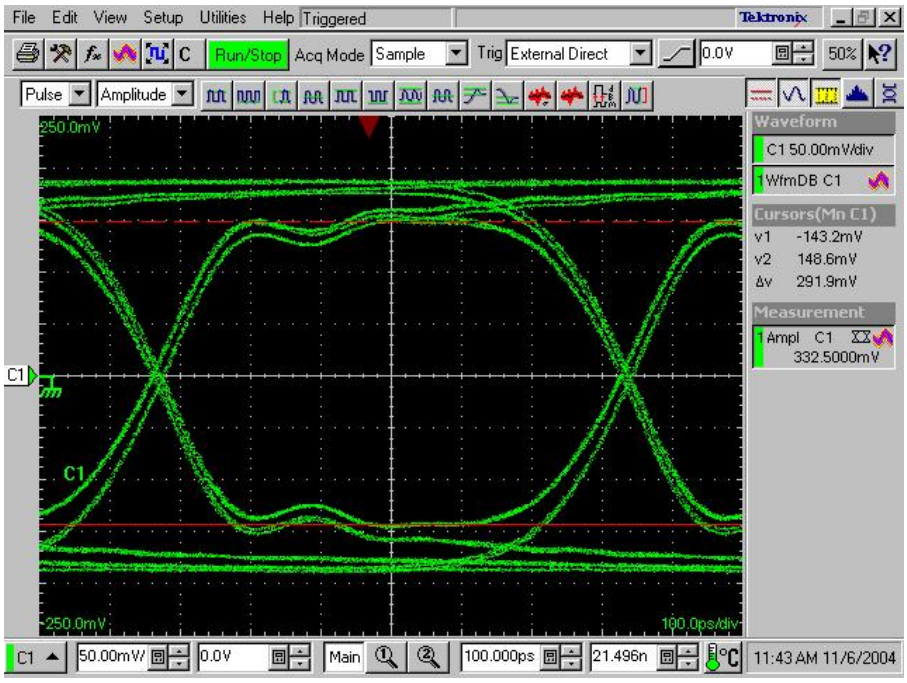
Vpp at receiver end of TCTF test load with

- D3186 pattern generator transmitting K28.5+, K28.5- (Note, this pattern is invalid)
- Vpp at transmitter of 400mVpp
- Measured amplitude of 287mVpp at scope terminated load



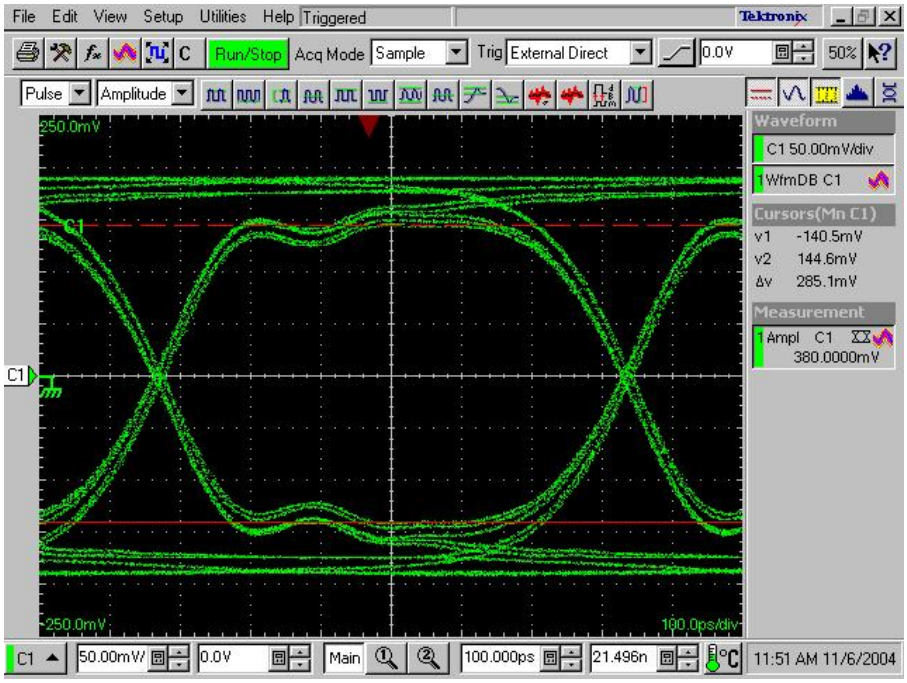
Vpp at receiver end of TCTF test load with

- D3186 pattern generator transmitting D12.0-, D11.4+
- Vpp at transmitter of 400mVpp
- Measured amplitude of 292mVpp at scope terminated load



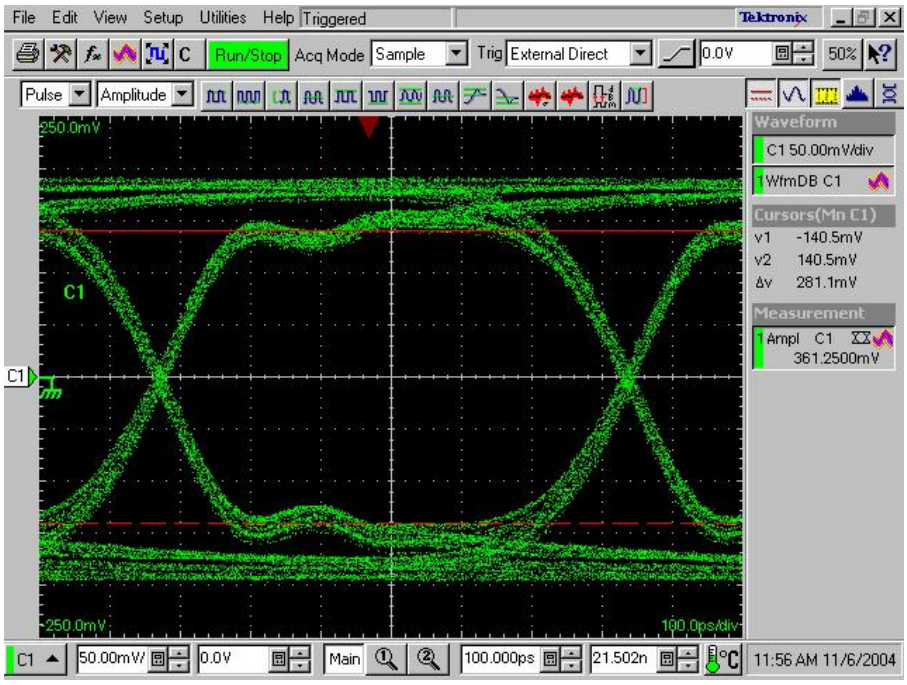
Vpp at receiver end of TCTF test load with

- D3186 pattern generator transmitting D11.7+, D20.7-
- Vpp at transmitter of 400mVpp
- Measured amplitude of 285mVpp at scope terminated load



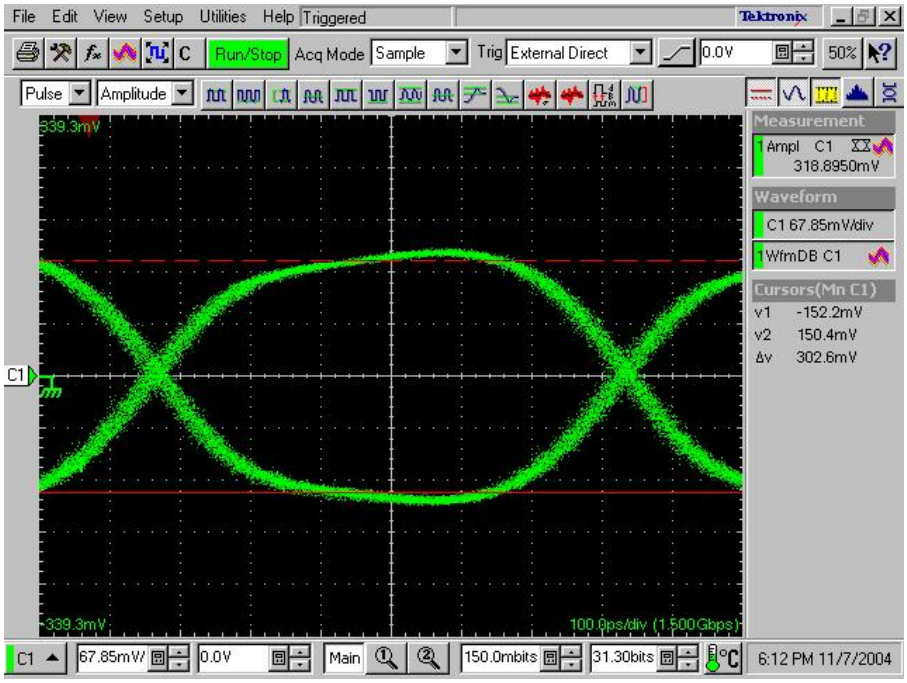
Vpp at receiver end of TCTF test load with

- D3186 pattern generator transmitting PRBS7
- Vpp at transmitter of 400mVpp
- Measured amplitude of 281mVpp at scope terminated load



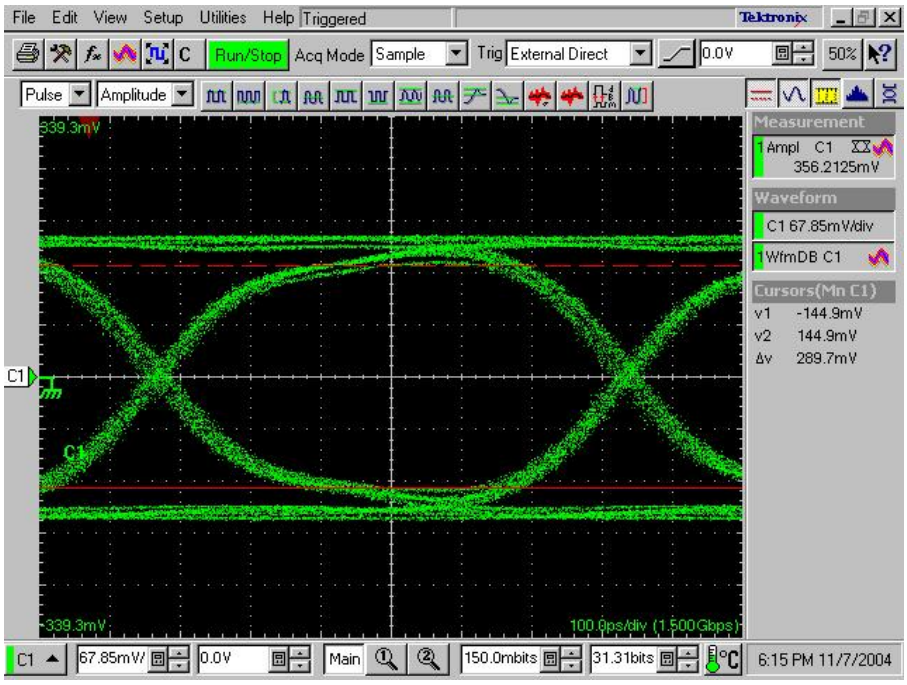
Vpp at receiver end of TCTF test load with

- 100ps edge rate reference phy transmitting D10.2
- Vpp at transmitter of 400mVpp (with scaling factor on scope)
- Measured amplitude of 303mVpp at scope terminated load



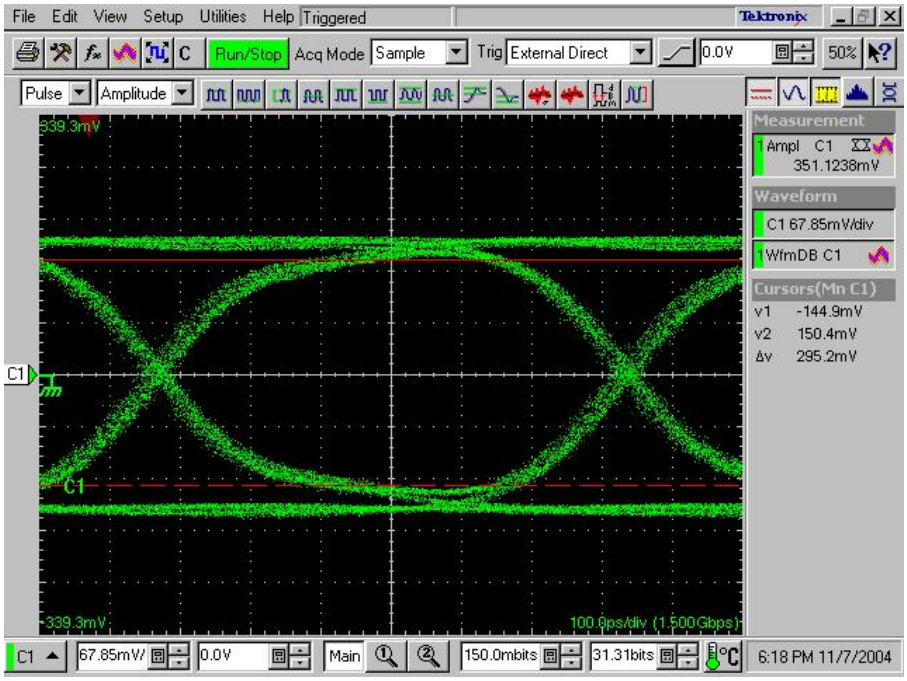
Vpp at receiver end of TCTF test load with

- 100ps edge rate reference phy transmitting K28.5+, K28.5- (Note, this pattern is invalid)
- Vpp at transmitter of 400mVpp
- Measured amplitude of 290mVpp at scope terminated load



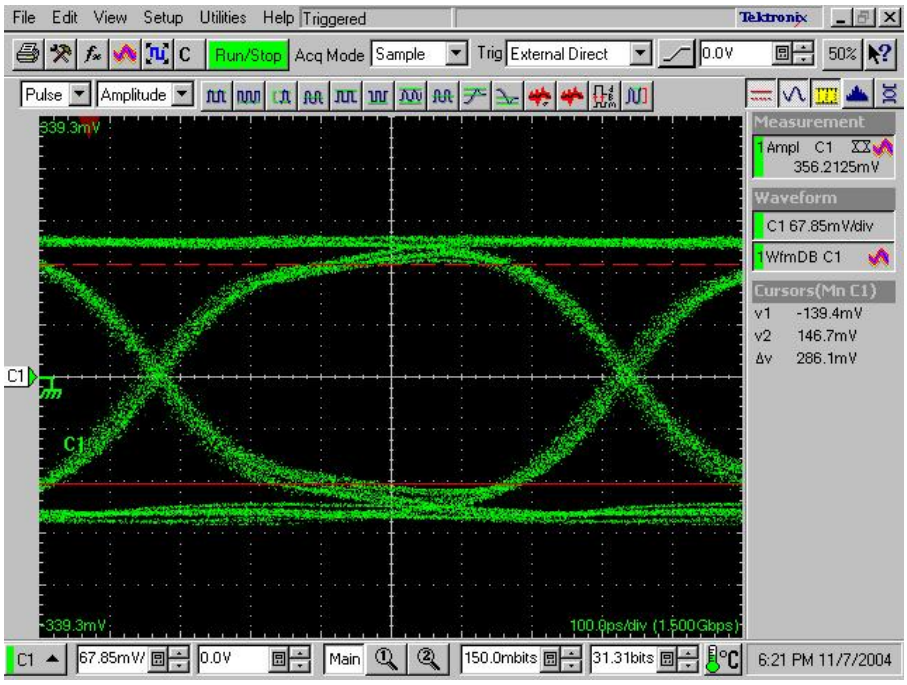
Vpp at receiver end of TCTF test load with

- 100ps edge rate reference phy transmitting D12.0-, D11.4+
- Vpp at transmitter of 400mVpp
- Measured amplitude of 295mVpp at scope terminated load



Vpp at receiver end of TCTF test load with

- 100ps edge rate reference phy transmitting D11.7+, D20.7-
- Vpp at transmitter of 400mVpp
- Measured amplitude of 286mVpp at scope terminated load

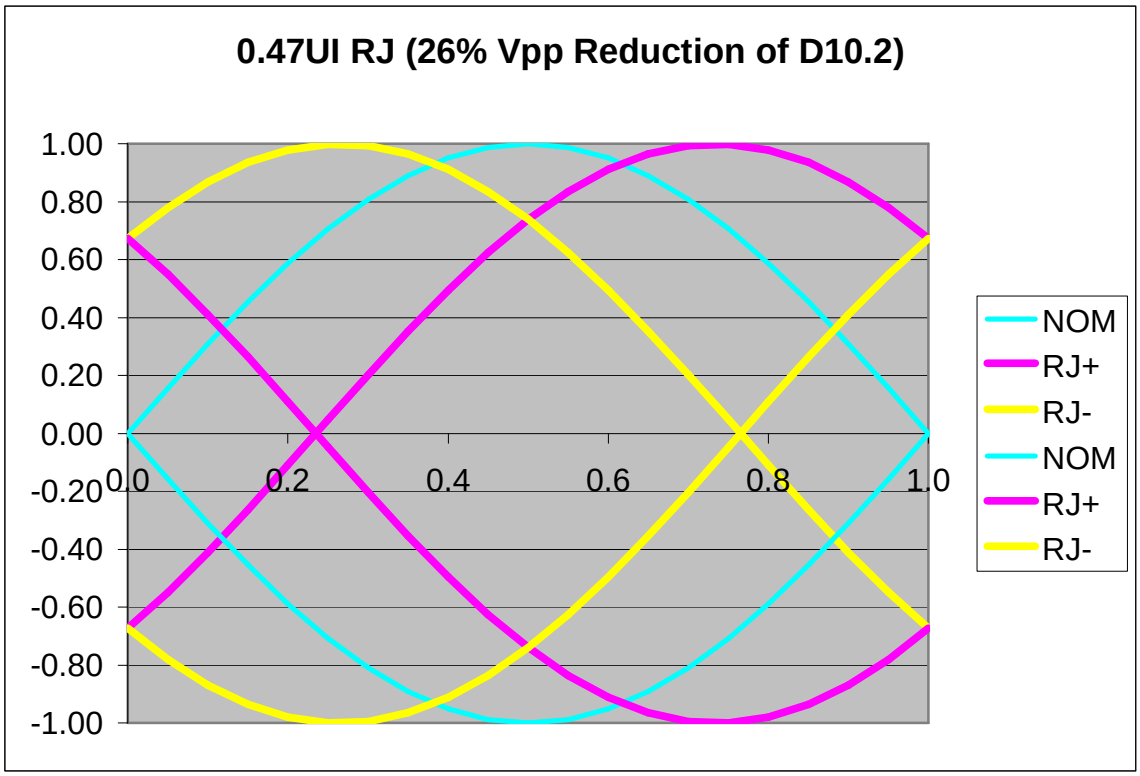


Amplitude Measurement Methodology of Serial ATA

To determine the signal amplitude using SATA disc drives with the TCTF we must understand how the drive is qualified. Serial ATA Amplitude measurements are NOT made using the classical eye-diagram approach. For SATA II, samples are acquired in a 0.1UI section at the center of specific bits using predefined patterns. The center position of the bit is determined by a recovered clock but for SATA I the method is not clearly defined. The samples of high and low states are then averaged. The process provides different results than what would be obtained with the classical eye-diagram approach. I will examine each component further.

RJ:

The following diagram displays a single bit of a D10.2 pattern with maximum rise time. Assuming maximum jitter output and none of it deterministic, we obtain 0.47UI of random jitter as indicated by the shifted edges.

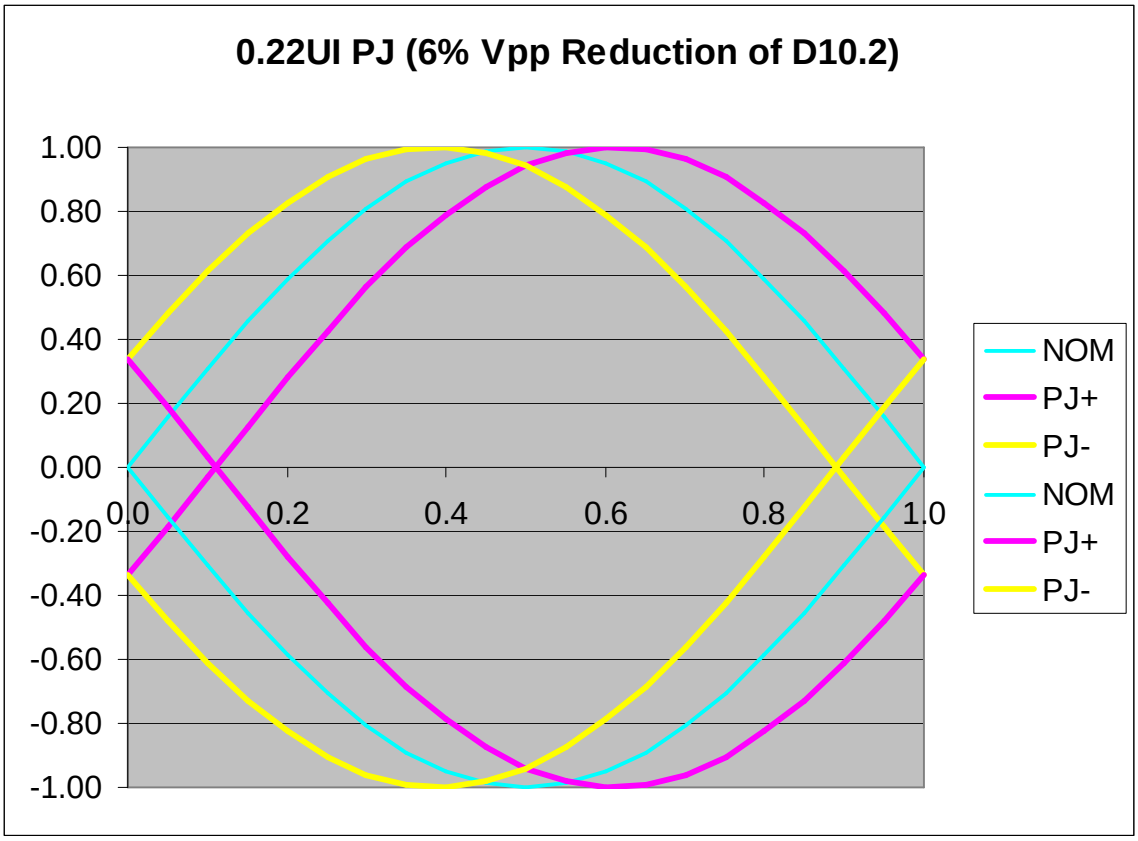


Using an eye-diagram approach to measuring the amplitude we can see that the amplitude has been reduced by at least 26% due the addition of jitter. Results obtained by the methodology defined in Serial ATA II are not so apparent.

Assuming RJ is untrackable by the clock recovery circuitry and a uniform distribution where RJ spans from -0.235UI to +0.235UI, the averaging process yields a 10% reduction. Processing of a Gaussian sample set yielded a slightly smaller value of 5%.

PJ:

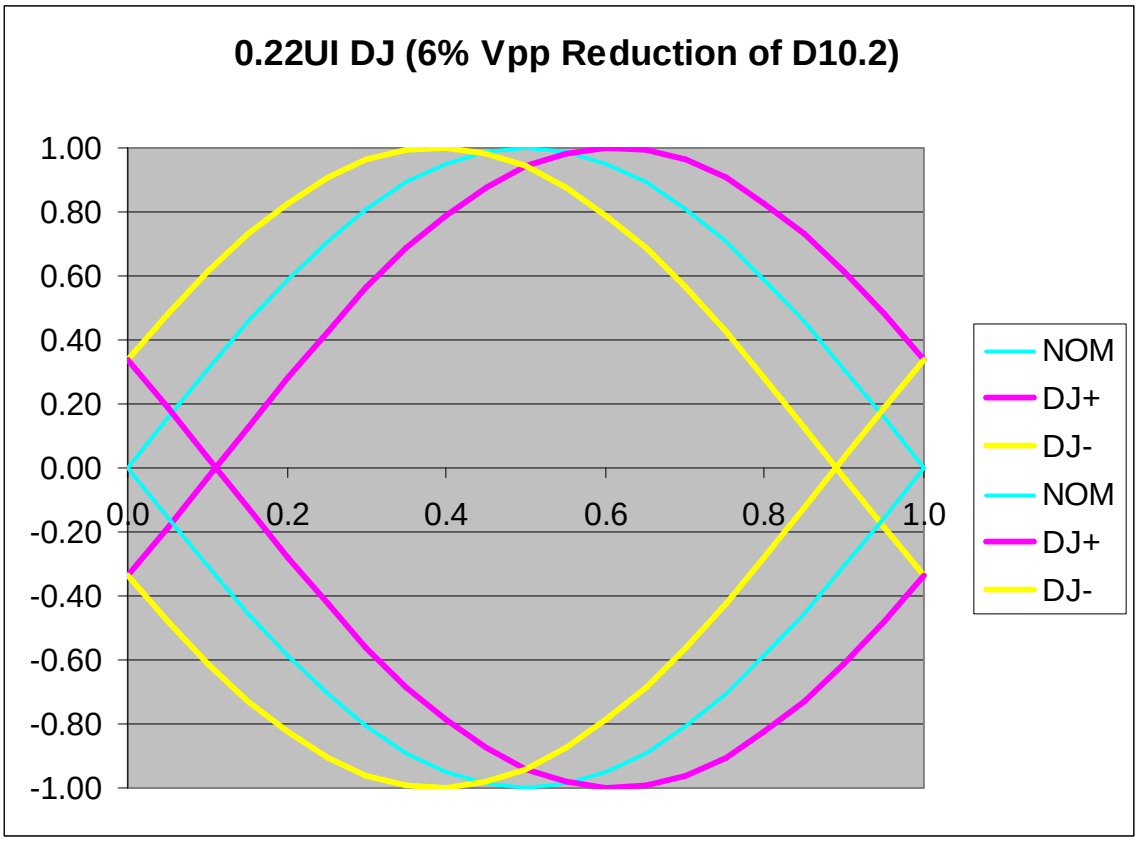
Assuming maximum deterministic jitter output and all of it is periodic, we obtain 0.22UI of deterministic jitter as indicated by the shifted edges.



Using an eye-diagram approach to measuring the amplitude we can see that the amplitude has been reduced by at least 6% due the addition of jitter. Assuming PJ is untrackable by the clock recovery circuitry and worst case distribution where consecutive edges are shifted by the +0.11UI and –0.11UI, a 6% amplitude reduction is obtained with the Serial ATA II methodology. An evenly spread distribution yields only a 2% reduction in the measured amplitude.

DJ (data dependent / ISI only):

Assuming maximum deterministic jitter output and all of it data dependent / ISI in nature, we obtain 0.22UI of deterministic jitter as indicated by the shifted edges. Clearly a D10.2 pattern does not exhibit data dependent jitter. A D10.2 pattern was chosen for this example to represent a the effect of additional jitter on a single bit within a more complicated pattern.



Using an eye-diagram approach to measuring the amplitude we can see that the amplitude has been reduced by at least 6% due the addition of jitter. Since the Serial ATA II methodology examines a specific bit of a repeating pattern, the additional jitter shall result in NO amplitude reduction.

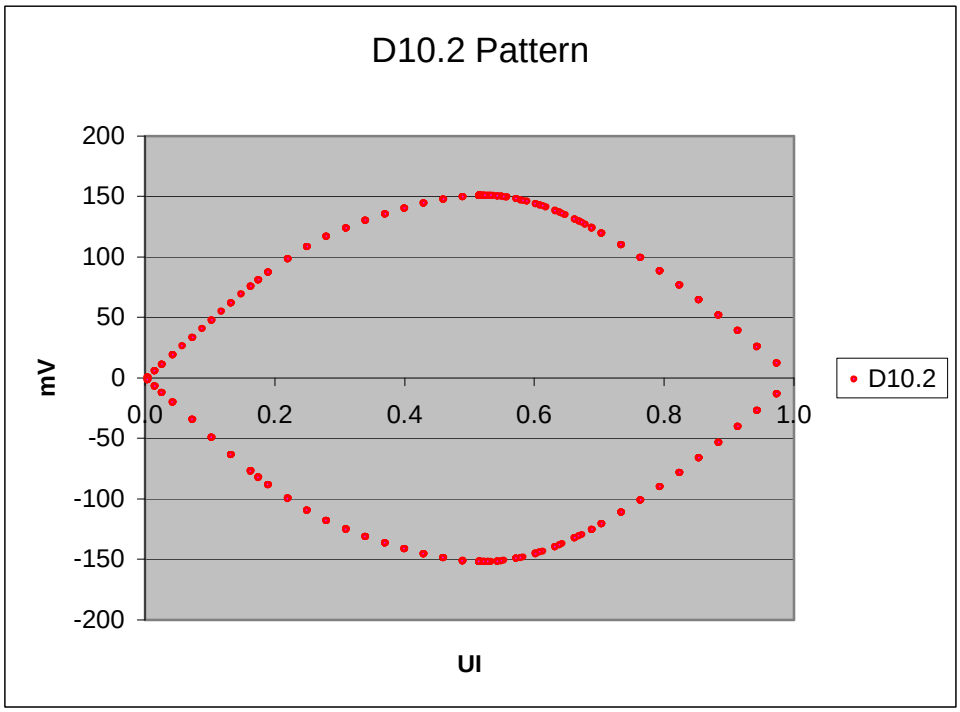
Given this, it would appear that the case where the two measurement methodologies differ the most is,

1) Data Dependent Jitter of 0.22UI
2) Random Jitter of 0.25UI (with a Gaussian distribution)

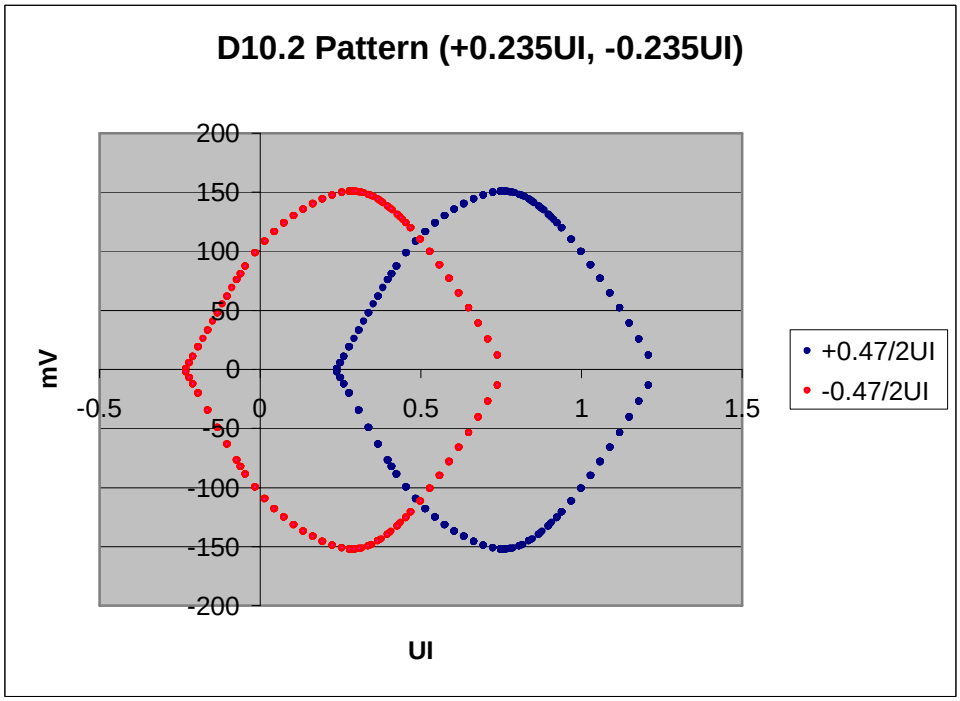
The eye-diagram approach indicates a 26% reduction whereas the Serial ATA II methodology results in a paltry 1% reduction.

Simulation Results

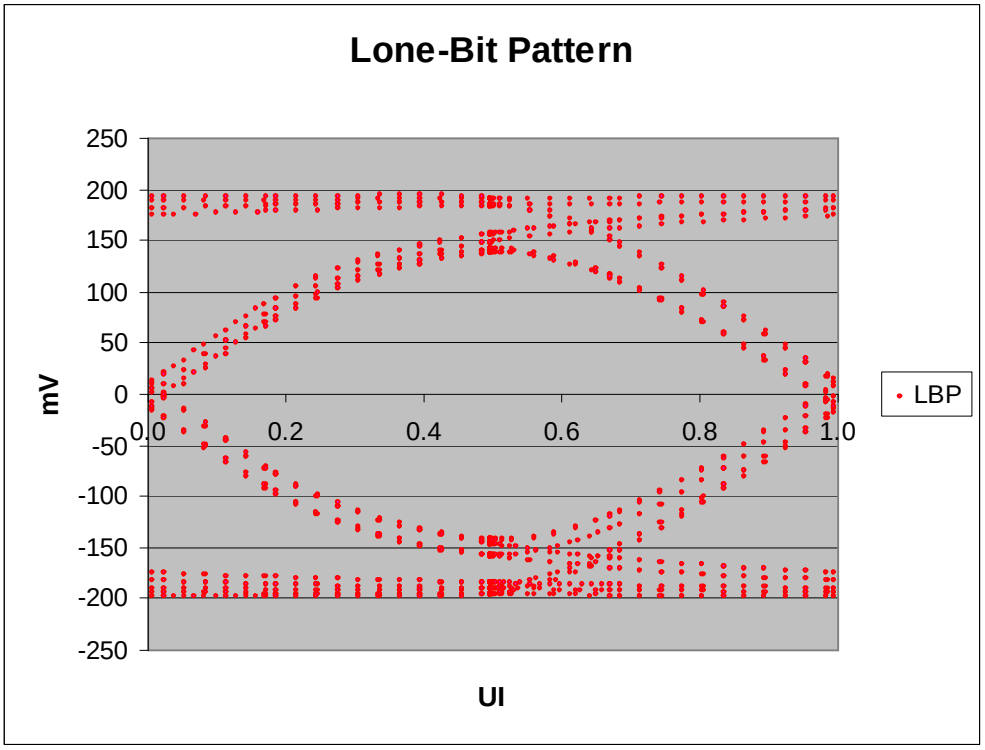
Simulation results of D10.2, K28.5 and the lone-bit patterns are included below. The transmitter amplitude is set to 400mVpp. A TCTF-IT/XT loss model is used. Rise/fall time of the transmitter is 267ps.



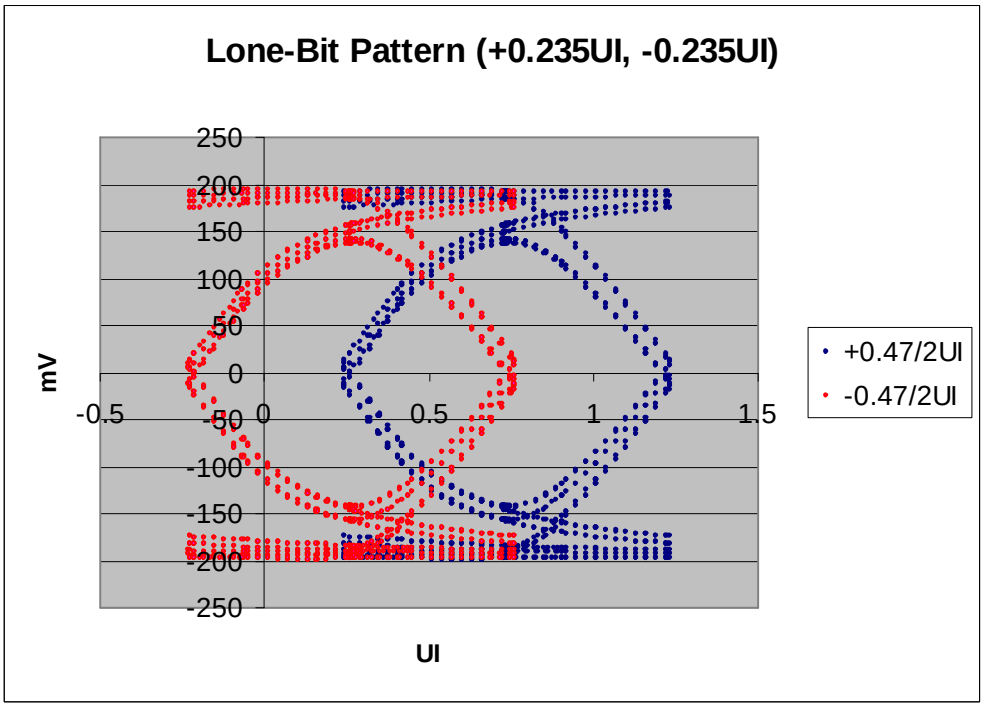
D10.2 amplitude with no transmitter jitter: 300mV



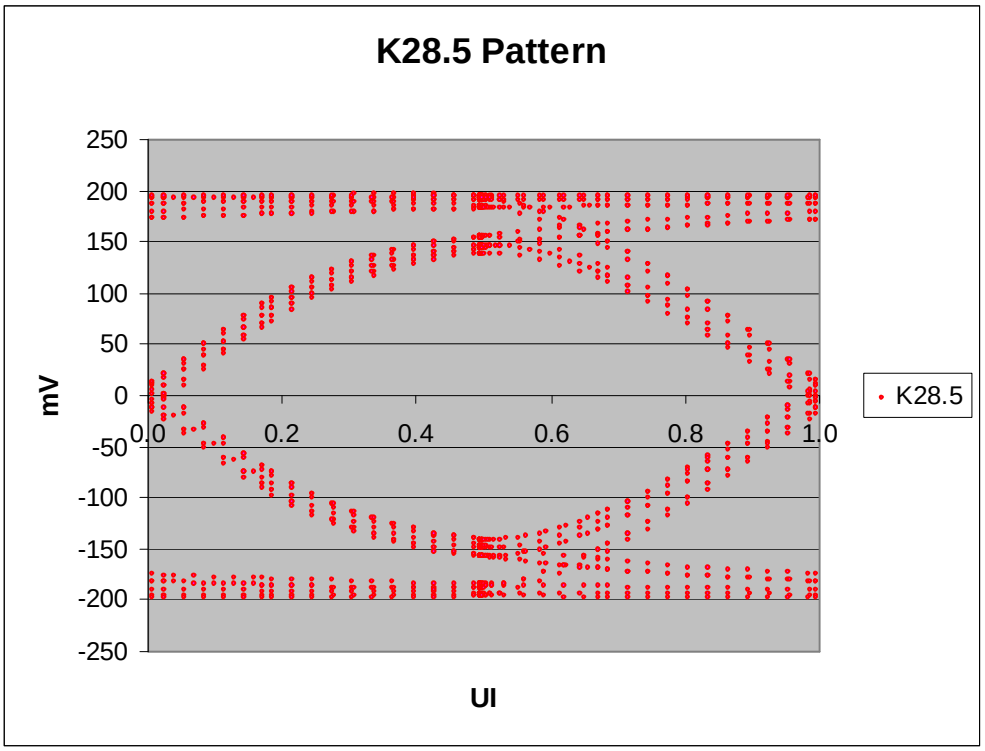
D10.2 amplitude with 0.47UI transmitter jitter: 220Mv



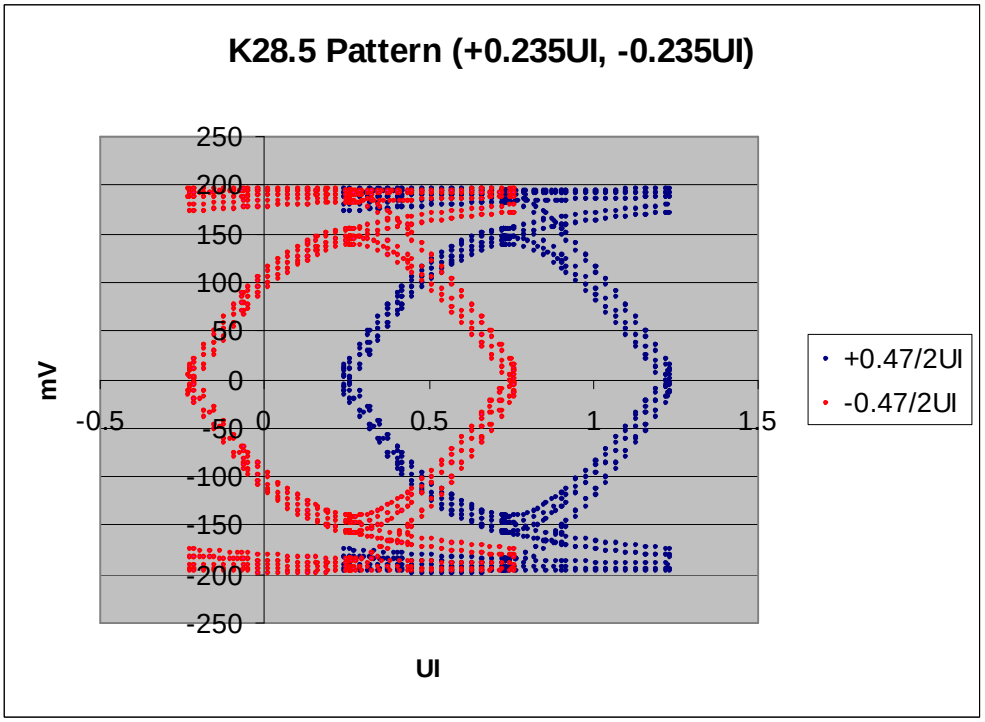
Lone-bit pattern amplitude with no transmitter jitter: 281mV



Lone-bit pattern amplitude with 0.47UI transmitter jitter: 195mV



K28.5 pattern amplitude with no transmitter jitter: 278mV



K28.5 pattern amplitude with 0.47UI transmitter jitter: 191mV

Conclusions

Clearly, using maximum rise/fall times and maximum transmitter jitter the amplitude is reduced. The most alarming conclusion of this study is how the differing test methodologies result in a very different interpretation of the same hardware. The appropriate solution is to use the same test methodology for all measurements. Therefore, SATA drives used in SAS applications should be tested using the same methodology as all other SAS hardware.