SAS 1.1 PHY jitter MJSQ modifications T10/04-332r0

Date: October 4, 2004
To: T10 Technical Committee
From: Bill Ham (bill.ham@hp,com)
Subject: SAS 1.1 PHY jitter MJSQ modifications

The following proposed changes to SAS 1.1 address jitter specifications in an effort to more closely reflect MJSQ methodology and definitions. Comments in other paragraphs of the PHY section are also included to document areas of concern that may need to be addressed separately. The final revision of this proposal shall include only changes to sections concerning jitter. Comments not related to jitter may be addressed by separate proposals.

5.2.4.2 SAS external cables

The SAS external cable connectors are defined in SFF-8470 as the four lane interface with jack screws. The external cable does not include power or the READY LED signal.

Although the connector always supports four physical links, the cable may support one, two, three, or four physical links.

On external cable assemblies, the Tx signal from one connector shall be connected to the corresponding Rx signal of the other connector (e.g., Tx 0+ (S16) of connector shall connect to Rx 0+ (S1) of the other connector) (see 5.2.3.6).

SIGNAL GROUND shall not be connected to CHASSIS GROUND in the cable.

5.2.5 Backplanes

Backplane designs should follow the recommendations in SFF-8460.

5.3 Transmitter and receiver electrical characteristics

5.3.1 Compliance points

Signal behavior at separable connectors and integrated circuit package connections that satisfy the description for a compliance point require compliance with transmitter and receiver characteristics defined by this standard only if the connectors or integrated circuit package connections are identified as compliance points by the supplier of the parts that contain or comprise the candidate compliance point. Table 24 lists the compliance points.

Table 24 — Compliance points

Compliance point	Type	Description
IT	intra-enclosure	Internal connector; transmit serial port
IR	intra-enclosure	Internal connector; receive serial port
CT	inter-enclosure	External connector; transmit serial port
CR	inter-enclosure	External connector; receive serial port
XT	intra-enclosure	Expander or SAS initiator phy; transmit serial port
XR	intra-enclosure	Expander or SAS initiator phy; receive serial port

[B Ham comments:

These definiitons for complinace points are not sufficient. As a minimum, the point in the link where the measurements specified later in this subclause apply needs to be identified. For example the IT point for signal outputs is presumably downstream of the mated connector and the IR point signal output specifications is likewise downstream of the mated connector. For the signal tolerance requirements the point is upstream of the IT connector. The physical compliance point may be on one side of the connector for one requirement and on the other side for the other requirement. One simply cannot make specifications that apply ‘at a connector’ - they must be related to one side or the other of mated connectors.]

5.3.2 General interface specification

A TxRx connection is the complete simplex signal path between the output reference point of one phy or retimer to the input reference point of a second phy or retimer, over which a BER of $< 10^{-12}$ is achieved.

A TxRx connection segment is that portion of a TxRx connection delimited by separable connectors or changes in media.

This subclause defines the interfaces of the serial electrical signal at the compliance points IT, IR, CT, CR, XT, and XR in a TxRx connection. The IT, IR, CT, and CR points are located at the connectors of a TxRx connection.

Each compliant phy shall be compatible with this serial electrical interface to allow interoperability within a SAS environment. All TxRx connections described in this subclause shall exceed the BER objective of 10^{-12}. The parameters specified in this section support meeting this requirement under all conditions including the minimum input and output amplitude levels.

These signal specifications are consistent with using good quality passive cable assemblies constructed with shielded twinaxial cable with 24 gauge solid wire up to eight meters in length.

Figure 46 shows the transmitter transient test circuit.

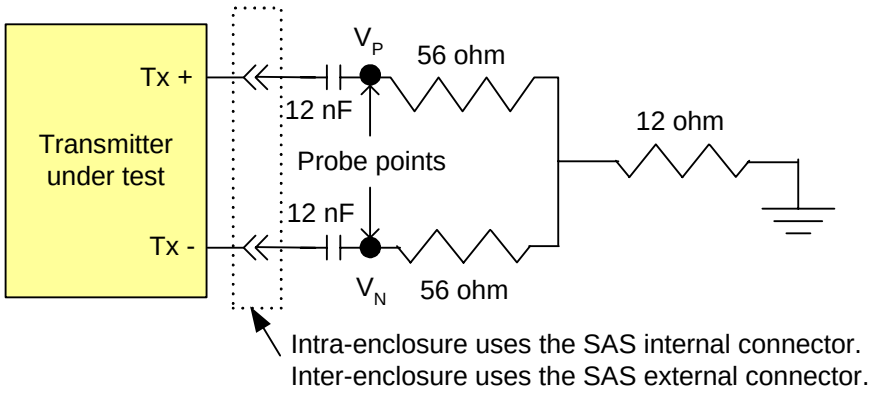

Figure 46 — Transmitter transient test circuit

Figure 47 shows the receiver transient test circuit.

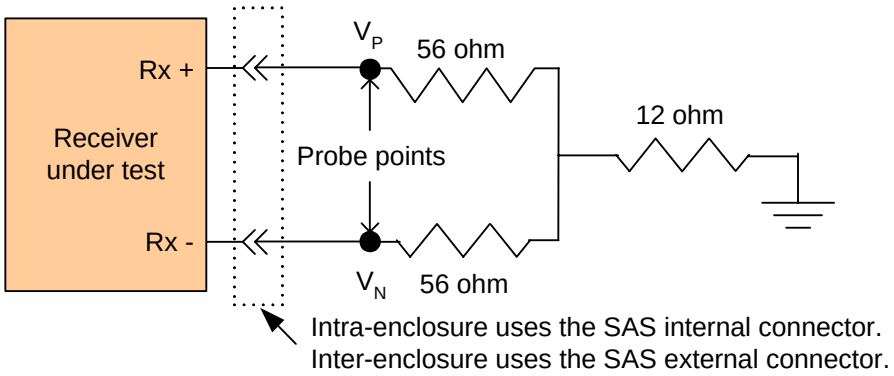

Figure 47 — Receiver transient test circuit

Table 25 defines the general interface characteristics.

Table 25 — General interface characteristics

Characteristic	Units	1,5 Gbps	3,0 Gbps
Physical link rate	MBps	150	300
Bit rate (nominal)	Mbaud	1 500	3 000
Unit interval (UI)(nominal)	ps	666,$\overline{6}$	333,$\overline{3}$
Physical link rate tolerance at XR [b]	ppm	+350 / -5 350	+350 / -5 350
Physical link rate tolerance at IR and CR	ppm	± 100	± 100
Physical link rate tolerance at IT, CT, and XT	ppm	± 100	± 100
Media Impedance (nominal) [a]	ohm	100	100
A.C. coupling capacitor, maximum [c]	nF	12	12
Transmitter transients, maximum [d]	V	± 1,2	± 1,2
Receiver transients, maximum [d]	V	± 1,2	± 1,2
Receiver A.C. common mode voltage tolerance V_{CM}, minimum [e]	mV(P-P)	150	150
Receiver A.C. common mode frequency tolerance range F_{CM} [e]	MHz	2 to 200	2 to 200

[a] The media impedances are the differential impedances.
[b] Allows support for SATA devices with spread spectrum clocking (see ATA/ATAPI-7 V3). SAS initiator phys supporting being attached to SATA devices should also use these tolerances.
[c] The coupling capacitor value for A.C. coupled transmit and receive pairs.
[d] The maximum transmitter and receiver transients are measured at nodes V_P and V_N on the test loads shown in figure 46 (for the transmitter) and figure 47 (for the receiver) during all power state and mode transitions. Test conditions shall include the system power supply ramping at the fastest possible rate for both power on and power off conditions.
[e] Receivers shall tolerate sinusoidal common mode noise components within the peak-to-peak amplitude (V_{CM}) and the frequency range (F_{CM}).

[B Ham comments

Receiver transient specifications are not adequately specified in this table. Is this a BER measurement? What are the other properties of the signal when this specification applies? See also comment below.

Note e: the idea of a receiver device tolerating some common mode level cannot be verified independently of other properties of the input signal. The best one can do here is to state that the receiver device shall tolerate input signals that have the stated common mode properties when all the other requirements of the input signal for a signal tolerance test are also met in the same signal.]

5.3.3 Eye masks

5.3.3.1 Eye masks overview

The eye masks shown in this subclause shall be interpreted as graphical representations of the voltage and time limits on the signal at the compliance point. ~~The time values between X1 and (1 - X1) cover all but 10^{-12} of the jitter population. The random content of the total jitter population has a range of ± 7 standard deviations.~~The mask boundaries define the eye contour of the 1E-12 population at all signal levels. Current equivalent time sampling oscilloscope technology is not practical for measuring compliance to this eye contour. See MJSQ for methods that are suitable for verifying compliance to these masks.

5.3.3.2 Receive eye mask at IR, CR, and XR

Figure 48 describes the receive eye mask. ~~This eye mask applies to jitter after the application of a single pole high-pass frequency weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of ((bit rate) / 1 667)~~

The signal shall be measured using a jitter timing reference, e.g. Golden PLL, that approximates a single pole (20dB / decade) low pass filter with corner frequency of the signaling rate / 1667. This requirement accounts for the low frequency tracking and response time of CDRs in receiver devices.

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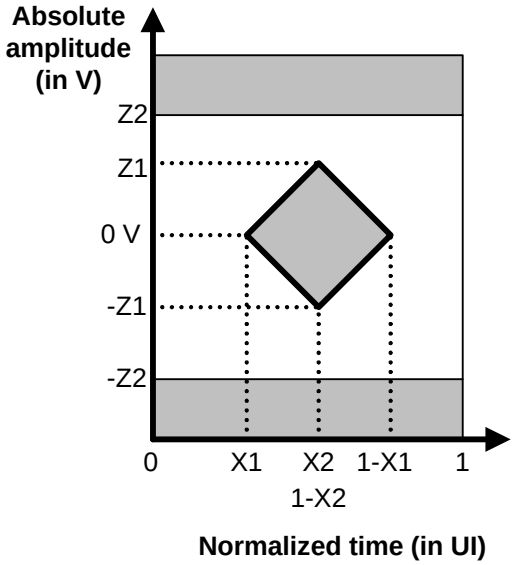

Figure 48 — Eye mask at IR, CR, and XR

Verifying compliance with the limits represented by the receive eye mask should be done with reverse channel traffic present in order that the effects of crosstalk are taken into account.

5.3.3.3 Jitter tolerance masks

Figure 49 describes the receive tolerance eye masks at IR, CR, and XR and shall be constructed using the X2 and Z2 values given in table 27. $X1_{OP}$ shall be half the value for total jitter in table 28 and $X1_{TOL}$ shall be half the value for total jitter in table 29, for applied sinusoidal jitter frequencies above ((bit rate) / 1 667).

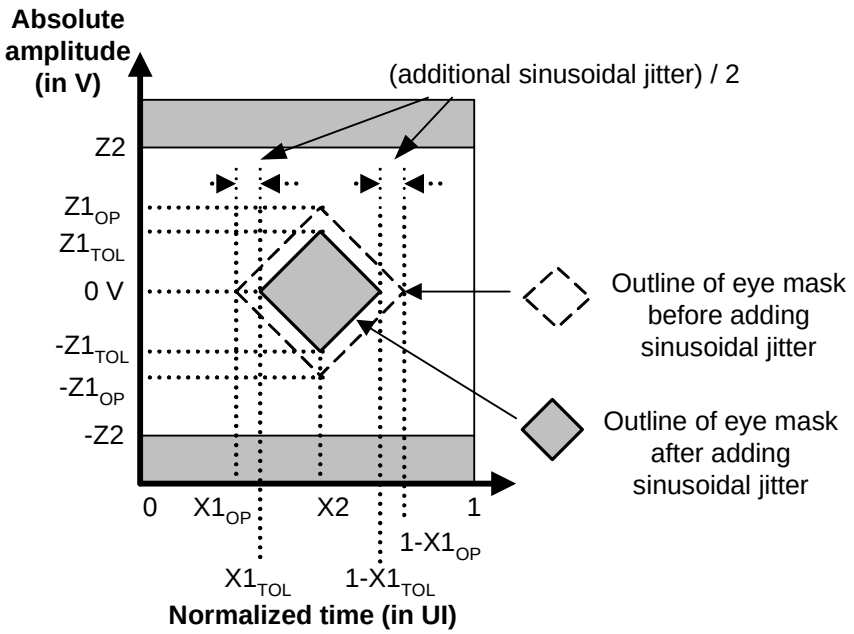

Figure 49 — Deriving a tolerance mask at IR, CR, or XR

The leading and trailing edge slopes of figure 48 shall be preserved. As a result the amplitude value of Z1 is less than that given in table 27 and $Z1_{TOL}$ and $Z1_{OP}$ shall be defined from those slopes by the following equation:

$$Z1_{TOL} = Z1_{OP} \times \frac{X2_{OP} - (0,5 \times \text{additional sinusoidal jitter}) - X1_{OP}}{X2_{OP} - X1_{OP}}$$

where:

a) $Z1_{TOL}$ is the value for Z1 to be used for the tolerance masks; and
b) $Z1_{OP}$, $X1_{OP}$, and $X2_{OP}$ are the values in table 27 for Z1, X1, and X2.

The X1 points in the receive tolerance masks are greater than the X1 points in the receive masks, due to the addition of sinusoidal jitter.

Figure 50 defines the applied sinusoidal jitter mask.

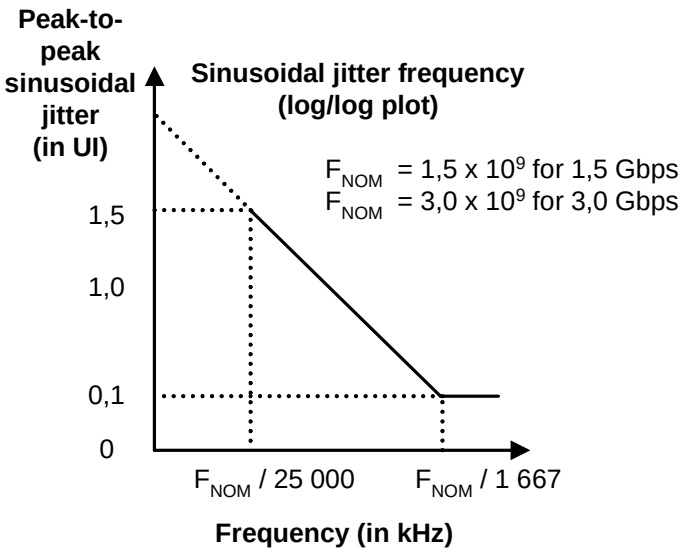

Figure 50 — Applied Sinusoidal jitter mask

5.3.4 Signal characteristics at IT, CT, and XT

This subclause defines the inter-operability requirements of the signal at the transmitter end of a TxRx connection as measured into the zero-length test load specified in figure 52. All specifications are based on differential measurements.

The OOB sequence shall be performed at signal voltage levels corresponding to the lowest supported transfer rate. Expander phys supporting being attached to SATA devices shall use SATA 1.0 signal levels (see ATA/ATAPI-7 V3) during the first OOB sequence after a power on or hard reset if the 1,5 Gbps transfer rate is supported. As soon as COMSAS has been exchanged, the expander phy shall increase its transmit levels to the SAS voltage levels specified in table 27. If a COMINIT is not received within a hot-plug timeout at SATA 1.0 signal levels, the expander phy shall increase its transmit levels to the SAS voltage levels and perform the OOB sequence again. If no COMINIT is received within a hot-plug timeout of the second OOB sequence the expander phy shall initiate another OOB sequence using SATA 1.0 signal levels. The expander phy shall continue alternating between sending COMINIT at SATA 1.0 signal levels and SAS signal levels until a COMINIT is received.

If the OOB sequence is completed at the SAS voltage level and a SATA device is detected rather than a SAS target device, the expander phy shall switch to SATA 1.0 voltage levels and repeat the OOB sequence.

NOTE 9 - SAS initiator phys supporting being attached to SATA devices may use the same algorithm as expander phys.

SAS initiator phys and SAS target phys shall transmit OOB signals at the lowest supported transfer rate using SAS signal levels.

Table 26 specifies the signal characteristics at IT, XT, and XT.

Table 26 — Signal characteristics at IT, CT, XT

Compliance point	Signal characteristic [a]	Units	1,5 Gbps	3,0 Gbps
IT, CT, XT	Skew [b]	ps	20	15
	Tx Off Voltage [c]	mV(P-P)	< 50	< 50
	Maximum rise/fall time [d]	ps	273	137
	Minimum rise/fall time [d]	ps	67	67
	Maximum transmitter output imbalance [e]	%	10	10
	OOB offset delta [f]	mV	± 25	± 25
	OOB common mode delta [g]	mV	± 50	± 50

[a] All tests in this table shall be performed with zero-length test load shown in figure 52.

[b] The skew measurement shall be made at the midpoint of the transition with a repeating 0101b pattern on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Tx+ and Tx- signals. Skew is defined as the time difference between the means of the midpoint crossing times of the Tx+ signal and the Tx- signal.

[c] The transmitter off voltage is the maximum A.C. voltage measured at compliance points IT, CT, and XT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).

[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 0101b pattern on the physical link.

[e] The maximum difference between the V+ and V- A.C. RMS transmitter amplitudes measured on a CJTPAT test pattern (see 5.3.8) into the test load shown in figure 52, as a percentage of the average of the V+ and V- A.C. RMS amplitudes.

[f] The maximum difference in the average differential voltage (D.C. offset) component between the burst times and the idle times of an OOB signal.

[g] The maximum difference in the average of the common mode voltage between the burst times and the idle times of an OOB signal.

5.3.5 Signal characteristics at IR, CR, and XR

Table 27 defines the compliance point requirements of the signal at the receiver end of a TxRx connection as measured into the test loads specified in figure 51 and figure 52.

Table 27 — Signal characteristics at IR, CR, and XR (part 1 of 2)

Compliance point	Signal characteristic	Units	SATA	1,5 Gbps	3,0 Gbps
IR [e]	Jitter (see figure 48) [b]	N/A	N/A	See table 28	See table 28
	2 x Z2	mV(P-P)	N/A	1 600	1 600
	2 x Z1	mV(P-P)	N/A	325	275
	X1 [a]	UI	N/A	0,275	0,275
	X2	UI	N/A	0,50	0,50
	Skew [d]	ps	N/A	80	75
	Max voltage (non-op)	mV(P-P)	N/A	2 000	2 000
	Minimum OOB ALIGN burst amplitude [c]	mV(P-P)	N/A	240	240
	Maximum noise during OOB idle time [c]	mV(P-P)	N/A	120	120
	Max near-end crosstalk [f]	mV(P-P)	N/A	100	100
CR	Jitter (see figure 48) [b]	N/A	N/A	See table 28	See table 28
	2 x Z2	mV(P-P)	N/A	1 600	1 600
	2 x Z1	mV(P-P)	N/A	275	275
	X1 [a]	UI	N/A	0,275	0,275
	X2	UI	N/A	0,50	0,50
	Skew [d]	ps	N/A	80	75
	Max voltage (non-op)	mV(P-P)	N/A	2 000	2 000
	Minimum OOB ALIGN burst amplitude [c]	mV(P-P)	N/A	240	240
	Maximum noise during OOB idle time [c]	mV(P-P)	N/A	120	120
	Max near-end crosstalk [f]	mV(P-P)	N/A	100	100

Table 27 — Signal characteristics at IR, CR, and XR (part 2 of 2)

Compliance point	Signal characteristic	Units	SATA	1,5 Gbps	3,0 Gbps
XR	Jitter (see figure 48) [b]	N/A	See table 28	See table 28	See table 28
	2 x Z2	mV(P-P)	600	1 600	1 600
	2 x Z1	mV(P-P)	225	325	275
	X1 [a]	UI	0,275	0,275	0,275
	X2	UI	0,50	0,50	0,50
	Skew [d]	ps	50	80	75
	Max voltage (non-op)	mV(P-P)	2 000	2 000	2 000
	Minimum OOB ALIGN burst amplitude [c]	mV(P-P)	240	240	240
	Maximum noise during OOB idle time [c]	mV(P-P)	120	120	120
	Max near-end crosstalk [f]	mV(P-P)	< 50	100	100

[a] The value for X1 shall be half the value given for total jitter in table 28. The test or analysis shall ~~include the effects of a single pole high-pass frequency weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of ((bit rate) / 1 667).~~be measured using a jitter timing reference, e.g. Golden PLL, that approximates a single pole (20dB / decade) low pass filter with corner frequency of the signaling rate / 1667. This requirement accounts for the low frequency tracking and response time of CDRs in receiver devices.

[b] The value for X1 applies at a total jitter probability of 10^{-12}. At this level of probability direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter output requirements. See MJSQ

[c] With a measurement bandwidth of 1,5 times the baud rate (i.e. 4,5 GHz for 3,0 Gbps).

[d] The skew measurement shall be made at the midpoint of the transition with a repeating 0101b pattern on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Rx+ and Rx- signals. Skew is defined as the time difference between the means of the midpoint crossing times of the Rx+ signal and the Rx- signal.

[e] If being attached to SATA devices is supported at the IR location, requirements of SATA shall be met at IR.

[f] Near-end crosstalk is the unwanted signal amplitude at receiver terminals DR, CR, and XR coupled from signals and noise sources other than the desired signal. Refer to SFF-8410.

5.3.6 Jitter

Table 28 defines the maximum allowable jitter at IR, CR, and XR.

Table 28 — Maximum allowable jitter at IR, CR, XR

Compliance point	1,5 Gbps [a, b]		3,0 Gbps [a, b]	
	Deterministic jitter [e]	Total jitter [c, d, e, f]	Deterministic jitter [e]	Total jitter [c, d, e, f]
IR	0,35	0,55	0,35	0,55
CR	0,35	0,55	0,35	0,55
XR	0,35	0,55	0,35	0,55

a Units are in UI. All DJ and TJ values are level 1.

b The values for jitter in this section are measured at the average signal amplitude point.

c ~~Total jitter is the sum of deterministic jitter and random jitter. If the actual deterministic jitter is less than the maximum specified, then the random jitter may increase as long as the total jitter does not exceed the specified maximum total jitter.~~{This note adds no value and implies that there is a specification on random jitter values.}

d Total jitter is specified at a CDF level of 10^{-12}.

e The deterministic and total values in this table apply to jitter ~~after application of a single pole high-pass frequency weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of ((bit rate) / 1 667).~~measured using a jitter timing reference, e.g. Golden PLL, that approximates a single pole (20dB / decade) low pass filter with corner frequency of the signaling rate / 1667. This requirement accounts for the low frequency tracking and response time of CDRs in receiver devices. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the method defined in MJSQ clause 8.

f If total jitter received at any point is less than the maximum allowed, then the jitter distribution of the signals is allowed to be asymmetric. The total jitter plus the magnitude of the asymmetry shall not exceed the allowed maximum total jitter. The numerical difference between the average of the peaks with a BER < 10^{-12} and the average of the individual events is the measure of the asymmetry. Jitter peak-to-peak measured < (maximum total jitter - |Asymmetry|).

5.3.7 Receiver jitter tolerance

Table 29 defines the amount of jitter the receiver shall tolerate at IR, CR, and XR.

Table 29 — Receiver jitter tolerance

Compliance point	1,5 Gbps [a]			3,0 Gbps [a]		
	Applied sinusoidal jitter [b, c]	Deterministic jitter [e, f, h]	Total jitter [h]	Applied sinusoidal jitter [b, d]	Deterministic jitter [e, g, h]	Total jitter [h]
IR	0,10	0,35	0,65	0,10	0,35	0,65
CR	0,10	0,35	0,65	0,10	0,35	0,65
XR	0,10	0,35	0,65	0,10	0,35	0,65

a Units are in UI. All DJ and TJ values are level 1.

b The jitter values given are normative for a combination of deterministic jitter, ~~random jitter~~ total jitter, and applied sinusoidal jitter that receivers shall be able to tolerate without exceeding a BER of 10^{-12}. Receivers shall tolerate applied sinusoidal jitter of progressively greater amplitude at lower frequencies, according to the mask in figure 50 with the same deterministic jitter and ~~random~~ total jitter levels as were used in the high frequency sweep.

c Applied sinusoidal swept frequency: 900 kHz to > 5 MHz.

d Applied sinusoidal swept frequency: 1 800 kHz to > 5 MHz.

e No value is given for random jitter. For compliance with this standard, the actual random jitter amplitude shall be the value that brings total jitter to the stated value at a probability of 10^{-12}. The additional 0,1 UI of sinusoidal jitter is added to ensure the receiver has sufficient operating margin in the presence of external interference.

f Deterministic jitter: 900 kHz to 750 MHz.[This is the bandwidth of the instrument - not the DJ itself]

g Deterministic jitter: 1 800 kHz to 1 500 MHz. [This is the bandwidth of the instrument - not the DJ itself]

h The deterministic and total values in this table apply to jitter ~~after application of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of ((bit rate) / 1 667)~~measured using a jitter timing reference, e.g. Golden PLL, that approximates a single pole (20dB / decade) low pass filter with corner frequency of the signaling rate / 1667. This requirement accounts for the low frequency tracking and response time of CDRs in receiver devices. Values for DJ and TJ shall be calculated from the CDF for the jitter population using the method defined in MJSQ clause 8.

5.3.8 Compliant jitter test pattern (CJTPAT)

The CJTPAT within a compliant protocol frame shall be used for all jitter testing unless otherwise specified. Annex A defines the required pattern on the physical link and information regarding special considerations for scrambling and running disparity.

5.3.9 Impedance specifications

Table 30 defines impedance requirements.

Table 30 — Impedance requirements (part 1 of 2)

Requirement	Units	1,5 Gbps	3,0 Gbps
Time domain reflectometer rise time 20 % to 80 % [a, b]	ps	100	50
Media (PCB or cable)			
Differential impedance [b, c, d]	ohm	100 ± 10	100 ± 10
Differential impedance imbalance [b, c, d, g]	ohm	5	5
Common mode impedance [b, c, d]	ohm	32,5 ± 7,5	32,5 ± 7,5

Table 30 — Impedance requirements (part 2 of 2)

Requirement	Units	1,5 Gbps	3,0 Gbps
Mated connectors			
Differential impedance [b, c, d]	ohm	100 ± 15	100 ± 15
Differential impedance imbalance [b, c, d, g]	ohm	5	5
Common mode impedance [b, c, d]	ohm	32,5 ± 7,5	32,5 ± 7,5
Receiver termination			
Differential impedance [b, e, f]	ohm	100 ± 15	100 ± 15
Differential impedance imbalance [b, e, f, g]	ohm	5	5
Receiver termination time constant [b, e, f]	ps	150 max	100 max
Common mode impedance [b, e]	ohm	20 min/40 max	20 min/40 max
Transmitter source termination			
Differential impedance [b]	ohm	60 min/115 max	60 min/115 max
Differential impedance imbalance [b, g]	ohm	5	5
Common mode impedance [b]	ohm	15 min/40 max	15 min/40 max

[a] All times indicated for time domain reflectometer measurements are recorded times. Recorded times are twice the transit time of the time domain reflectometer signal.

[b] All measurements are made through mated connector pairs.

[c] The media impedance measurement identifies the impedance mismatches present in the media when terminated in its characteristic impedance. This measurement excludes mated connectors at both ends of the media, when present, but includes any intermediate connectors or splices. The mated connectors measurement applies only to the mated connector pair at each end, as applicable.

[d] Where the media has an electrical length of > 4 ns the procedure detailed in SFF-8410, or an equivalent procedure, shall be used to determine the impedance.

[e] The receiver termination impedance specification applies to all receivers in a TxRx connection and covers all time points between the connector nearest the receiver, the receiver, and the transmission line terminator. This measurement shall be made from that connector.

[f] At the time point corresponding to the connection of the receiver to the transmission line the input capacitance of the receiver and its connection to the transmission line may cause the measured impedance to fall below the minimum impedances specified in this table. The area of the impedance dip (amplitude as ρ, the reflection coefficient, and duration in time) caused by this capacitance is the receiver termination time constant. The receiver time constant shall not be greater than the values shown in this table. An approximate value for the receiver termination time constant is given by the product of the amplitude of the dip (as ρ) and its width (in ps) measured at the half amplitude point. The amplitude is defined as being the difference in the reflection coefficient between the reflection coefficient at the nominal impedance and the reflection coefficient at the minimum impedance point. The value of the receiver excess input capacitance is given by the following equation:

$$\frac{\text{receiver termination time const}}{(R0 \parallel RR)}$$

where (R0 || RR) is the parallel combination of the transmission line characteristic impedance and termination resistance at the receiver.

[g] The difference in measured impedance to ground on the plus and minus terminals on the interconnect, transmitter or receiver, with a differential test signal applied to those terminals.

5.3.10 Electrical TxRx connections

TxRx connections may be divided into TxRx connection segments. In a single TxRx connection individual TxRx connection segments may be formed from differing media and materials, including traces on printed wiring boards and optical fibers. This subclause applies only to TxRx connection segments that are formed from electrically conductive media.

Each electrical TxRx connection segment shall comply with the impedance requirements of table 30 for the media from which they are formed. An equalizer network, if present, shall be part of the TxRx connection.

TxRx connections that are composed entirely of electrically conducting media shall be applied only to homogenous ground applications (e.g., between devices within an enclosure or rack, or between enclosures interconnected by a common ground return or ground plane).

5.3.11 Transmitter characteristics

For all inter-enclosure TxRx connections, the transmitter shall be A.C. coupled to the interconnect through a transmission network.

For intra-enclosure TxRx connections the expander transmitter shall be A.C. coupled to the interconnect. Other transmitters may be A.C. or D.C. coupled.

A combination of a zero-length test load and the transmitter compliance transfer function (TCTF) test load methodology is used for the specification of the inter-enclosure and intra-enclosure transmitter characteristics. This methodology specifies the transmitter signal at the test points on the required test loads. The transmitter shall use the same settings (e.g., pre-emphasis, voltage swing) with both the zero-length test load and the TCTF test load. The signal specifications at IR, CR, and XR shall be met under each of these loading conditions.

The TCTF is the mathematical statement of the transfer function through which the transmitter shall be capable of producing acceptable signals as defined by a receive mask. The transmission magnitude response of the TCTF in dB is given by the following equation for 1,5 Gbps:

$$|S_{21}| = -20 \times \log_{10}(e) \times ((6,5 \times 10^{-6} \times f^{0,5}) + (2,0 \times 10^{-10} \times f) + (3,3 \times 10^{-20} \times f^{2})) \text{ dB}$$

for 50 MHz < f < 1,5 GHz, and:

$$|S_{21}| = -5,437 \text{ dB}$$

for 1,5 GHz < f < 5,0 GHz,

where:

f is the signal frequency in hertz.

The transmission magnitude response of the TCTF in dB is given by the following equation for 3,0 Gbps:

$$|S_{21}| = -20 \times \log_{10}(e) \times ((6,5 \times 10^{-6} \times f^{0,5}) + (2,0 \times 10^{-10} \times f) + (3,3 \times 10^{-20} \times f^{2})) \text{ dB}$$

for 50 MHz < f < 3,0 GHz, and:

$$|S_{21}| = -10,884 \text{ dB}$$

for 3,0 GHz < f < 5,0 GHz,

where:

f is the signal frequency in hertz.

The TCTF is used to specify the requirements on transmitters that may or may not incorporate pre-emphasis or other forms of compensation. A compliance interconnect is any physical interconnect with loss equal to or greater than that of the TCTF at the above frequencies that also meets the ISI loss requirements shown in figure 53 and figure 54.

Compliance with the TCTF test load requirement shall be determined either:

a) by measuring the signal produced by the transmitter through a physical compliance interconnect attached to the transmitter; or
b) by mathematically processing through the TCTF the signal captured using a zero-length test load.

Compliance with the zero-length test load requirement shall be determined by measurement made across a load equivalent to the zero-length load shown in figure 52.

For both test load cases, the transmitter shall deliver the output voltages and timing listed in table 27 at the designated compliance points. The default mask shall be CR for inter-cabinet TxRx connections and IR for intra-cabinet TxRx connections. The eye masks are shown in 5.3.3.

Figure 51 shows the compliance interconnect test load.

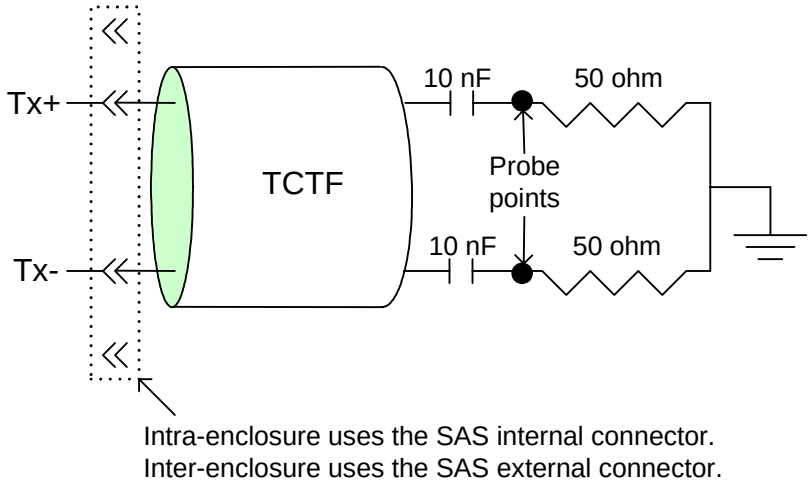

Figure 51 — Compliance interconnect test load

Figure 52 shows the zero-length test load.

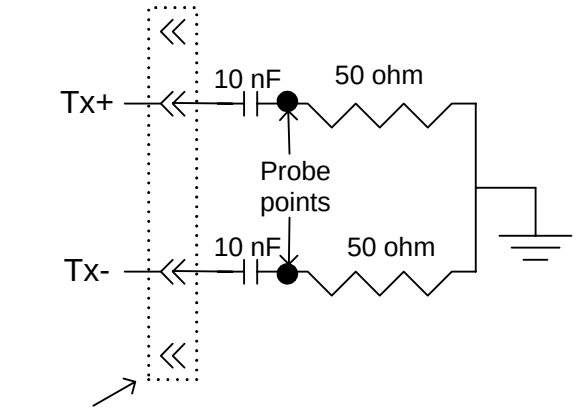

Figure 52 — Zero-length test load

Figure 53 shows an ISI loss example at 3,0 Gbps.

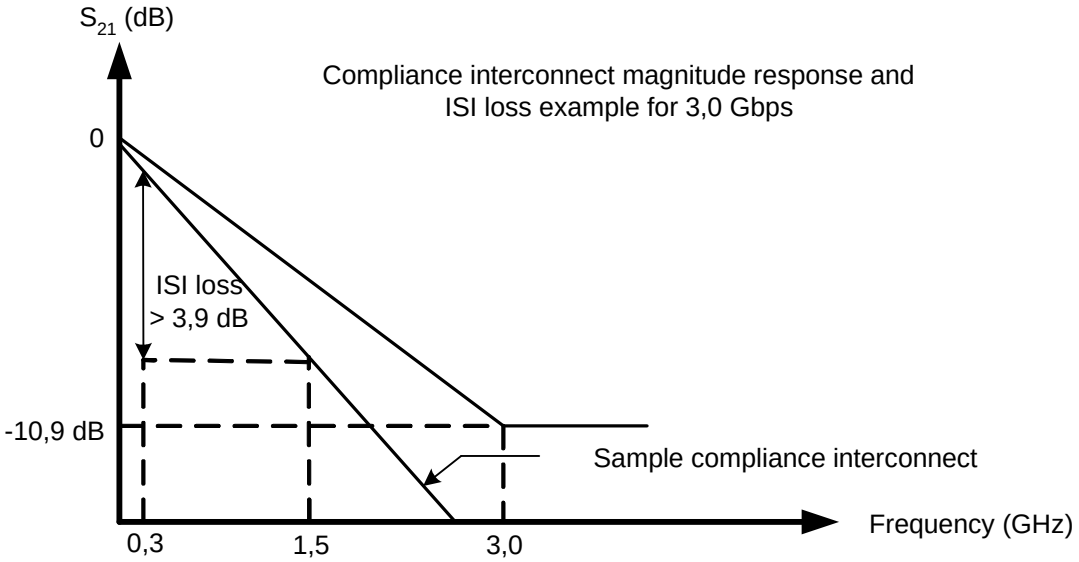

Figure 53 — ISI loss example at 3,0 Gbps

Figure 54 shows an ISI loss example at 1,5 Gbps.

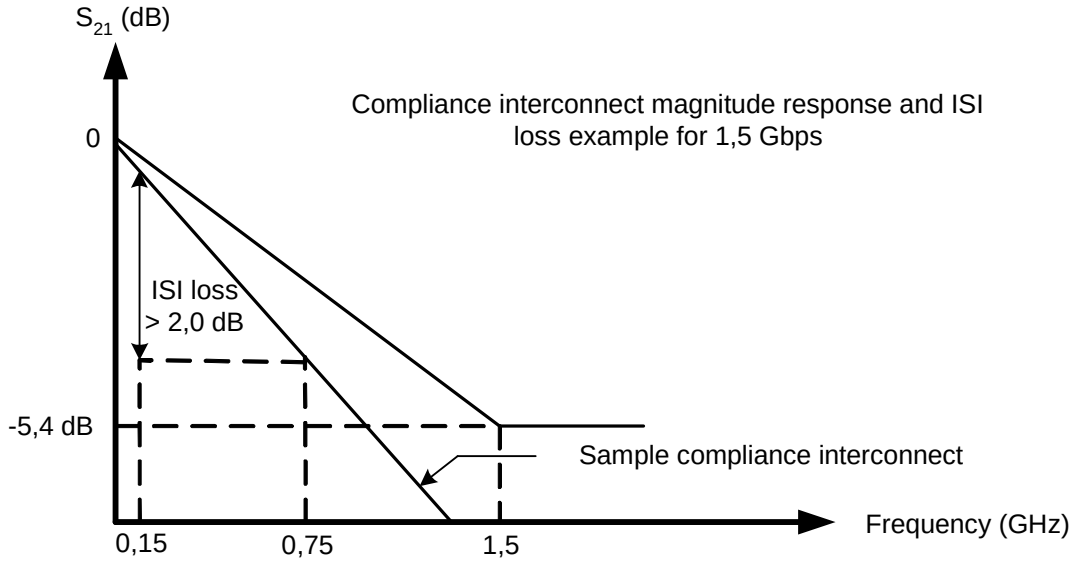

Figure 54 — ISI loss example at 1,5 Gbps

5.3.12 Receiver characteristics

The receiver shall be A.C. coupled to the interconnect through a receive network. The receive network shall terminate the TxRx connection by a 100 ohm equivalent impedance as specified in table 30.

The receiver shall operate within a BER of 10^{-12} when a SAS signal with valid voltage and timing characteristics is delivered to the compliance point from a 100 ohm source. The received SAS signal shall be considered valid if it meets the voltage and timing limits specified in table 27.

[B Ham comment: This method as stated does not allow credit for transmitter devices with equalization. See T11/04-024v6.]

Additionally the receiver shall also operate within the BER objective when the signal at a receiving phy has the additional sinusoidal jitter present that is specified in table 29 and the common mode signal V_{CM} over

frequency range F_{CM} as specified in table 25. The jitter tolerance figure is given in figure 49 for all Rx compliance points in a TxRx connection. The figure given assumes that any external interference occurs prior to the point at which the test is applied. When testing the jitter tolerance capability of a receiver, the additional 0,1 UI of sinusoidal jitter may be reduced by an amount proportional to the actual externally induced interference between the application point of the test and the input to the receiving phy. The additional jitter reduces the eye opening in both voltage and time.

[B Ham comment: the jitter that should be reduced is not the 0.1UI of applied sinusoidal but rather the DJ and TJ that is produced upstream of the interoperability point closest to the PHY receiver. This is an over simplification of specifying signal tolerance at all the interoperability points. See MJSQ.

5.3.13 Spread spectrum clocking

Phys shall not transmit with spread spectrum clocking. Expander phys that support being attached to SATA devices shall support receiving with spread spectrum clocking (see ATA/ATAPI-7 V3). The expander device shall retime data from a SATA device with an internal clock before forwarding to the rest of the SAS domain.

NOTE 10 - If SAS initiator devices support being attached to SATA devices, they should follow the same rules as expander phys.

5.3.14 Non-tracking clock architecture

Phys shall be designed with a non-tracking clock architecture; the receive clock derived from the received bit stream shall not be used as the transmit clock. Expander phys that support being attached to SATA devices shall tolerate clock tracking by the SATA device.

NOTE 11 - If SAS initiator devices support being attached to SATA devices, they should follow the same rules as expander phys.

5.4 READY LED signal electrical characteristics

A SAS target device uses the READY LED signal to activate an externally visible LED that indicates the state of readiness and activity of the SAS target device.

All SAS target devices using the SAS plug connector (see 5.2.3.2) shall support the READY LED signal.

The READY LED signal is designed to pull down the cathode of an LED using an open collector or open drain transmitter circuit. The LED and the current limiting circuitry shall be external to the SAS target device.

Table 31 describes the output characteristics of the READY LED signal.

Table 31 — Output characteristics of the READY LED signal

State	Test condition	Requirement
Negated (LED off)	$0\ V \le V_{OH} \le 3{,}6\ V$	$-100\ \mu A < I_{OH} < 100\ \mu A$
Asserted (LED on)	$I_{OL} = 15\ mA$	$0 \le V_{OL} \le 0{,}225\ V$

The READY LED signal behavior is defined in 10.4.1.