Date: October 4, 2004
To: T10 Technical Committee
From: Bill Ham (bill.ham@hp,com)
Subject: SAS 1.1 PHY Definitions and Acronyms update

The following proposed changes to SAS 1.1 adds a reference to MJSQ, refines and/or adds definitions based on SAS 1.1 application and latest MJSQ wording, and adds missing acronyms.

INCITS.xxx, *AT Attachment with Packet Interface-7 Volume 1 (ATA/ATAPI-7 V1) standard* (T13/1532-D)

INCITS.xxx, *AT Attachment with Packet Interface-7 Volume 3 (ATA/ATAPI-7 V3)(Serial ATA) standard* (T13/1532-D)

ISO/IEC 14776-413, *SCSI Architecture Model-3 (SAM-3) standard* (T10/1561-D)

ISO/IEC 14776-453, *SCSI Primary Commands-3 (SPC-3) standard* (T10/1416-D)

ISO/IEC 14776-322, *SCSI Block Commands-2 (SBC-2) standard* (T10/1417-D)

> NOTE 1 - For more information on the current status of these documents, contact the INCITS Secretariat at 202-737-8888 (phone), 202-638-4922 (fax) or via Email at incits@itic.org. To obtain copies of these documents, contact Global Engineering at 15 Inverness Way, East Englewood, CO 80112-5704 at 303-792-2181 (phone), 800-854-7179 (phone), or 303-792-2192 (fax) or see http://www.incits.org.

2.4 Other references

For information on the current status of the listed documents, or regarding availability, contact the indicated organization.

Serial ATA 1.0 Design Guides. 5 April 2002

Serial ATA II: Extensions to Serial ATA 1.0. Revision 1.0. 16 October 2002

Serial ATA II: Port Selector. Revision 1.0. 28 July 2003

> NOTE 2 - For information on the current status of the Serial ATA documents, contact the Serial ATA Working Group at info@serialata.org. To obtain copies of these documents, see http://www.serialata.org.

INCITS xxx - DT: Methodologies for Jitter and Signal Quality Specification (MJSQ) INCITS technical report. Revision 14 (T11/1316-DT)

SFF-8223, *2.5" Drive Form Factor with Serial Connector*

SFF-8323, *3.5" Drive Form Factor with Serial Connector*

SFF-8523, *5.25" Drive Form Factor with Serial Connector*

SFF-8410, *HSS Copper Testing and Performance Requirements*

SFF-8460, *HSS Backplane Design Guidelines*

SFF-8470, *Shielded High Speed Multilane Copper Connector*

SFF-8482, *Internal Serial Attachment Connector*

> NOTE 3 - For more information on the current status of the SFF documents, contact the SFF Committee at 408-867-6630 (phone), or 408-867-2115 (fax). To obtain copies of these documents, contact the SFF Committee at 14426 Black Walnut Court, Saratoga, CA 95070 at 408-867-6630 (phone) or 408-741-1600 (fax) or see http://www.sffcommittee.org.

OMG Unified Modeling Language (UML) Specification. Version 1.4, September 2001.

> NOTE 4 - For more information on the UML specification, contact the Object Modeling Group at http://www.omg.org.

Common Information Model (CIM) Specification. Version 2.2, 14 June 1999.

> NOTE 5 - For more information on the CIM specification, contact the Desktop Management Task Force, Inc. at http://www.dmtf.org.

3 Definitions, symbols, abbreviations, keywords, and conventions

3.1 Definitions

3.1.1 8b10b coding: A coding scheme that represents an 8-bit data byte as a 10-bit character. See 6.2.

3.1.2 affiliation: STP target port state of limiting acceptance of connection requests to those from a single STP initiator port. See 7.17.4.

3.1.3 application client: An object that is the source of SCSI commands (see SAM-3), ATA commands (see ATA/ATAPI-7 V1), or management function requests.

3.1.4 AT Attachment (ATA): A standard for the internal attachment of storage devices to hosts. See ATA/ATAPI-7 V1.

3.1.5 ATA device: A storage peripheral (analogous to a SCSI target device). See ATA/ATAPI-7 V1.

3.1.6 ATA domain: An I/O system consisting of a set of ATA hosts and ATA devices that communicate with one another by means of a service delivery subsystem. See 4.1.1.

3.1.7 ATA host: A host device that originates requests to be processed by an ATA device (analogous to a SCSI initiator device). See ATA/ATAPI-7 V1.

0.0.1 bandwidth: in jitter context, the corner frequency of a low-pass transmission characteristic, such as that of a receiver.

0.0.2 Baud: a unit of signaling speed, expressed as the maximum number of times per second the signal may change the state of the transmission line or other medium. (Units of Baud are symbols/sec) Note: With the SAS transmission scheme, a symbol represents a single transmission bit. [(Adapted from IEEE Std. 610.7-1995 [A16].12)].

3.1.8 big-endian: A format for storage or transmission of binary data in which the most significant byte appears first. In a multi-byte value, the byte containing the most significant bit is stored in the lowest memory address and transmitted first and the byte containing the least significant bit is stored in the highest memory address and transmitted last (e.g., for the value 0080h, the byte containing 00h is stored in the lowest memory address and the byte containing 80h is stored in the highest memory address).

0.0.3 bit error ratio (BER): the probability of a correct transmitted bit being erroneously received in a communication system. For purposes of this report BER is the number of bits output from a receiver that differ from the correct transmitted bits, divided by the number of transmitted bits.

0.0.4 bit clock: clock used in a jitter measurement that generates a single positive and a single negative transition per unit interval for the purpose of triggering the measuring device. Note that the bit clock frequency is twice the fundamental frequency of an alternating 1010... data stream and is equal numerically to the Baud.

3.1.9 broadcast primitive processor (BPP): An object within an expander function that manages broadcast primitives. See 4.6.5.

3.1.10 burst time: The part of an OOB signal (see 3.1.82) where ALIGN primitives (see 3.1.93) are being transmitted. See 6.5.

3.1.11 byte: A sequence of eight contiguous bits considered as a unit.

0.0.5 clock data recovery (CDR): the function is provided by the SERDES circuitry responsible for producing a regular clock signal from the serial data and for aligning this clock to the serial data bits. The CDR uses the recovered clock to recover the data.

3.1.12 character: A sequence of ten contiguous bits considered as a unit. A byte is encoded as a character using 8b10b coding (see 6.2).

3.1.13 command descriptor block (CDB): A structure used to communicate a command from a SCSI application client to a SCSI device server. See SAM-3.

0.0.6   compliance point: an interoperability point where the interoperability specifications are met.

3.1.14 compliant jitter test pattern (CJTPAT): A test pattern for jitter testing. See 5.3.8.

3.1.15 configurable expander device: An expander device that contains an expander route table that is configured with expander route entries. See 4.1.5.

3.1.16 confirmation: A message passed from a lower layer state machine to a higher layer state machine, usually responding to a request (see 3.1.102) from that higher layer state machine, and sometimes relaying a response (see 3.1.104) from a peer higher layer state machine.

3.1.17 connection: A temporary association between a SAS initiator port and a SAS target port. See 7.12.

3.1.18 connection rate: The effective rate of dwords through the pathway between a SAS initiator phy and a SAS target phy, established through the connection request.

0.0.7   connector: electro-mechanical components consisting of a receptacle and a plug that provides a separable interface between two transmission media segments. Connectors may introduce physical disturbances to the transmission path due to impedance mismatch, crosstalk, etc. These disturbances may introduce jitter and other forms of signal degradation under certain conditions.

3.1.19 control character (Kxx.y): A character that does not represent a byte of data. See 6.2.

0.0.8   cumulative distribution function (CDF): the integral of the PDF from - infinity to a specific time or from a specific time to + infinity.

3.1.20 cyclic redundancy check (CRC): An error checking mechanism that checks data integrity by computing a polynomial algorithm based checksum. See 7.5.

3.1.21 D.C. idle: A differential signal level that is nominally 0 V(P-P). See 5.3.4.

3.1.22 data character (Dxx.y): A character representing a byte of data. See 6.2.

3.1.23 data dword: A dword that starts with a Dxx.y (data character).

3.1.24 deadlock: A condition in which two or more processes (e.g., connection requests) are waiting on each other to complete, resulting in none of the processes completing.

3.1.25 deterministic jitter: ~~Jitter with a non-Gaussian probability density function. Deterministic jitter is always bounded in amplitude and has specific causes. Four kinds of deterministic jitter are identified: duty cycle distortion, data dependent, sinusoidal, and uncorrelated (to the data) bounded. Deterministic jitter is characterized by its bounded, peak-to-peak value.~~

3.1.26 device server: An object within a SAS target device that processes SCSI tasks (see SAM-3), ATA commands (see ATA/ATAPI-7 V1), or management functions.

3.1.27 direct current (D.C.): The non-A.C. component of a signal. In this standard, all frequency components below 100 kHz.

3.1.28 direct routing attribute: The attribute of an expander phy that indicates it may be used by the expander connection manager to route a connection request to an end device. See 4.6.7.1.

3.1.29 direct routing method: The method the expander connection manager uses to establish a connection with an end device. See 4.6.7.1.

3.1.30 discover process: The algorithm used by a management application client to configure the SAS domain. See 4.6.7.4.

3.1.31 disparity: The difference between the number of ones and zeros in a character (see 6.2).

0.0.9   dispersion: (1) A term in used to denote pulse broadening and distortion from all causes. (2) Frequency dispersion caused by a dependence of propagation velocity on frequency, that leads to a pulse widening in a system with infinitely wide bandwidth. The term 'dispersion' when used without qualifiers is definition (1) in this document.

3.1.32 domain: A SAS domain, a SCSI domain, or an ATA domain.

3.1.33 dword: A sequence of four contiguous bytes or four contiguous characters considered as a unit.

0.0.10   duty cycle distortion (DCD): (1) The absolute value of one half the difference in the average pulse width of a '1' pulse or a '0' pulse and the ideal bit time in a clock-like (repeating 0,1,0,1,...) bit sequence.   (2) One-half of the difference of the average width of a one and the average width of a zero in a waveform eye pattern measurement. Definition (2) contains the sign of the difference and is useful in the presence of actual data. DCD from definition (2) may be used with arbitrary data and is approximately the same quantitatively as that observed with clock like patterns in definition (1). DCD is not a level 1 quantity.   DCD is considered to be correlated to the data pattern because it is synchronous with the bit edges. Mechanisms that produce DCD are not expected to change significantly with different data patterns. The observation of DCD may change with changes in the data pattern. DCD is part of the DJ distribution and is measured at the average value of the waveform.

3.1.34 dword synchronization: Detection of an incoming stream of dwords from a physical link by a phy. See 6.8.

3.1.35 edge expander device: An expander device that is part of a single edge expander device set.

3.1.36 edge expander device set: A group of one or more edge expander devices that may be attached to no more than one other edge expander device set or one fanout expander device. See 4.1.8.2.

0.0.11   effective DJ: DJ used for level 1 compliance testing, and determined by curve fitting a measured CDF to a cumulative or integrated dual-Dirac function, where each Dirac impulse, located at +DJ/2 and -DJ/2, is convolved with separate half-magnitude Gaussian functions with standard deviations sigma1 and sigma2. Equivalent to level 1 DJ. See clause 8 of MJSQ.

0.0.12   electrical fall time: the time interval for the falling edge of an electrical pulse to transit between specified percentages of the signal amplitude. In the context of SAS the measurement points are the 80% and 20% voltage levels.

0.0.13   electrical rise time: the time interval for the rising edge of an electrical pulse to transit between specified percentages of the signal amplitude. In the context of SAS, the measurement points are the 20% and 80% voltage levels.

0.0.14   enclosure: the outermost electromagnetic boundary (that acts as an EMI barrier) containing one or more SAS devices.

3.1.37 end device: A SAS device that is not contained within an expander device.

3.1.38 event notification: A message passed from the transport layer to the application layer notifying the application layer that a SCSI event has occurred. See SAM-3.

3.1.39 expander connection manager (ECM): An object within an expander function that manages routing. See 4.6.4.

3.1.40 expander connection router (ECR): The portion of an expander function that routes messages between expander phys. See 4.6.4.

3.1.41 expander device: A device that is part of the service delivery subsystem and facilitates communication between SAS devices. See 4.1.5.

3.1.42 expander function: An object within an expander device that contains an expander connection manager, expander connection router, and broadcast primitive processor. See 4.6.1.

3.1.43 expander phy: A phy in an expander device that interfaces to a service delivery subsystem.

3.1.44 expander port: An expander device object that interfaces to the service delivery subsystem and to SAS ports in other devices.

3.1.45 expander route entry: A routed SAS address and an enable/disable bit in an expander route table (see 4.6.7.3).

3.1.46 expander route index: A value used in combination with a phy identifier to select an expander route entry in an expander route table (see 4.6.7.3).

3.1.47 expander route table: A table of expander route entries within an expander device. The table is used by the expander function to resolve connection requests. See 4.6.7.3.

0.0.15 external connector: a bulkhead connector, whose purpose is to carry the SAS signals into and out of an enclosure, that exits the enclosure with only minor compromise to the shield effectiveness of the enclosure.

0.0.16 eye contour: the locus of points in signal level - time space where the CDF = 1E-12 in the actual signal population determines whether a jitter eye mask violation has occurred.

3.1.48 fanout expander device: An expander device that is capable of being attached to two or more edge expander device sets.

3.1.49 field: A group of one or more contiguous bits.

3.1.50 frame: A sequence of data dwords between a start of frame primitive (e.g., SOF, SOAF, or SATA_SOF) and an end of frame primitive (e.g., EOF, EOAF, or SATA_EOF).

3.1.51 frame information structure (FIS): The SATA frame format. See ATA/ATAPI-7 V3.

0.0.17 Golden PLL: a function that conforms to the requirements in sub clause 6.10.2 of MJSQ that extracts the jitter timing reference from the data stream under test to be used as the timing reference for the instrument used for measuring the jitter in the signal under test.

3.1.52 hard reset: A SAS device or expander device action in response to a reset event in which the device performs the operations described in 4.4.

3.1.53 hard reset sequence: A sequence that causes a hard reset (see 4.4).

3.1.54 hardware maximum physical link rate: The maximum physical link rate capability of a phy.

3.1.55 hardware minimum physical link rate: The minimum physical link rate capability of a phy.

3.1.56 hash function: A mathematical function that maps values from a larger set of values into a smaller set of values, reducing a long value into a shorter hashed value.

3.1.57 I_T nexus: A nexus that exists between a SCSI initiator port and a SCSI target port.

3.1.58 I_T nexus loss: A condition where a SAS port determines that another SAS port is no longer available. See 4.5.

3.1.59 I_T_L nexus: A nexus that exists between a SCSI initiator port, a SCSI target port, and a logical unit. This relationship extends the prior I_T nexus.

3.1.60 I_T_L_Q nexus: A nexus between a SCSI initiator port, a SCSI target port, a logical unit, and a task. This relationship extends the prior I_T nexus or I_T_L nexus.

3.1.61 identification sequence: A sequence where phys exchange IDENTIFY address frames. See 4.4.

3.1.62 idle dword: A vendor-specific data dword that is scrambled and is transmitted outside a frame. See 7.4.

3.1.63 idle time: The part of an OOB signal (see 3.1.82) where D.C. idle (see 5.3.4) is being transmitted. See 6.5.

3.1.64 indication: A message passed from a lower layer state machine to a higher layer state machine, usually relaying a request (see 3.1.102) from a peer higher layer state machine.

3.1.65 information unit (IU): The portion of an SSP frame that carries command, task management function, data, response, or transfer ready information. See 9.2.2.

> Editor's Note 1: need a definition of intersymbol interference (ISI), since it is used a few times in clause 5.

0.0.18   Intersymbol Interference (ISI): reduction in the distinction of a pulse caused by overlapping energy from neighboring pulses. (Neighboring means close enough to have significant energy overlapping and does not imply or exclude adjacent pulses - many bit times may separate the pulses especially in the case of reflections). ISI may result in DDJ and vertical eye closure. Important mechanisms that produce ISI are dispersion, reflections, and circuits that lead to baseline wander.

3.1.66 invalid dword: A dword with an illegal character, with a control character in other than the first character position, with a control character other than K28.5 or K28.3 in the first character position, or with a running disparity error.

3.1.67 jitter: ~~Abrupt and unwanted variations in the interval between successive pulses.~~

0.0.19   jitter: the collection of instantaneous deviations of a signal edge times at a defined signal level of the signal from the reference times for those events. The reference time is the jitter-timing-reference specified in 6.2.3 of MJSQ that occurs under a specific set of conditions.

0.0.20   jitter, data dependent (DDJ): jitter that is added when the transmission pattern is changed from a clock like to a non-clock like pattern. For example, data dependent deterministic jitter may be caused by the time differences required for the signal to arrive at the receiver threshold when starting from different places in bit sequences (symbols). DDJ is expected whenever any bit sequence has frequency components that are propagated at different rates. For example when using media that attenuates the peak amplitude of the bit sequence consisting of alternating 0,1,0,1... more than peak amplitude of the bit sequence consisting of 0,0,0,0,1,1,1,1... the time required to reach the receiver threshold with the 0,1,0,1... is less than required from the 0,0,0,0,1,1,1,1.... The run length of 4 produces a higher amplitude that takes more time to overcome when changing bit values and therefore produces a time difference compared to the run length of 1 bit sequence. When different run lengths are mixed in the same transmission the different bit sequences (symbols) therefore interfere with each other. Data dependent jitter may also be caused by reflections, ground bounce, transfer functions of coupling circuits and other mechanisms.

0.0.21   jitter, deterministic (DJ): jitter with non-Gaussian probability density function. Deterministic jitter is always bounded in amplitude and has specific causes. Deterministic jitter comprises (1) correlated DJ (data dependent (DDJ) and duty cycle distortion (DCD)), and (2) DJ that is uncorrelated to the data and bounded in amplitude (BUJ). DJ is characterized by its bounded, peak-to-peak value. Level 1 DJ, per clause 8 of MJSQ, is defined by an assumed CDF form and may be used for compliance testing.

0.0.22   jitter, sinusiodal (SJ): single tone jitter applied during signal tolerance testing.

0.0.23   jitter eye opening (horizontal): the time interval, measured at the signal level for the measurement (commonly at the time-averaged signal level), between the 10^{-12} CDF level for the leading and trailing transitions associated with a unit interval.

0.0.24   jitter frequency: the frequency associated with the jitter waveform produced by plotting the jitter for each signal edge against bit time in a continuously running bit stream.

0.0.25   jitter output: the quantity of jitter at a specific physical position in the link.

0.0.26   jitter, random, RJ: jitter that is characterized by a Gaussian distribution and is unbounded.

0.0.27   jitter, total, TJ: total jitter in UI is calculated from (1 - jitter eye opening) where jitter eye opening is measured in UI.

0.0.28   jitter timing reference: the signal used as the basis for calculating the jitter in the signal under test. The jitter timing reference has specific requirements on its ability to track and respond to changes in the signal under test. The jitter timing reference may be different from other timing references available in the system.

0.0.29   jitter tolerance for links: the ability of the link downstream from the receive interoperability point to recover transmitted bits in an incoming data stream in the presence of specified jitter in the signal. Jitter tolerance is measured by the amount of jitter required to produce a specified bit error ratio. The required jitter tolerance performance depends on the frequency content of the jitter. Since detection of bit errors is required to determine the jitter tolerance, receivers embedded in an SAS Ports require that the Port be capable of reporting bit errors. For receivers that are not embedded in SAS Ports the bit error detection and reporting may be accomplished by instrumentation attached to the output of the receiver. Jitter tolerance is always measured using the minimum allowed signal amplitude unless otherwise specified. See also signal tolerance.

0.0.30   jitter tolerance for receivers: the ability of a receiver to recover transmitted bits in an incoming data stream in the presence of specified jitter in the signal. Jitter tolerance is measured by the amount of jitter required to produce a specified bit error ratio. The reference point for the jitter tolerance of the receiver is the chip pin. The required jitter tolerance performance depends on the frequency content of the jitter. Since detection of bit errors is required to determine the jitter tolerance, receivers embedded in a SAS Port require that the Port be capable of reporting bit errors. For receivers that are not embedded in a SAS Port the bit error detection and reporting may be accomplished by instrumentation attached to the output of the receiver. Jitter tolerance is always measured using the minimum allowed signal amplitude unless otherwise specified. See also signal tolerance.

3.1.68 least significant bit (LSB): In a binary code, the bit or bit position with the smallest numerical weighting in a group of bits that, when taken as a whole, represent a numerical value (e.g., in the number 0001b, the bit that is set to one).

0.0.31   level 1 DJ: DJ used for compliance and budgeting is level 1 DJ. Level 1 DJ is the value returned by the calculation for DJ defined in clause 8 of MJSQ. Any valid CDF may be used as input to this calculation. See also jitter, deterministic.

0.0.32   level 1 TJ: TJ used for compliance and budgeting is level 1 TJ. Level 1 TJ is the value returned by the calculation for TJ defined in clause 8 of MJSQ. Any valid CDF may be used as input to this calculation. See also jitter, deterministic.

3.1.69 link reset: Performing the link reset sequence (see 3.1.70).

3.1.70 link reset sequence: For SATA, a phy reset sequence (see 3.1.87). For SAS, a phy reset sequence followed by an identification sequence (see 3.1.61), or a phy reset sequence followed by a hard reset sequence (see 3.1.53), another phy reset sequence, and an identification sequence. See 4.4.

3.1.71 little-endian: A format for storage or transmission of binary data in which the least significant byte appears first. In a multi-byte value, the byte containing the least significant bit is stored in the lowest memory address and transmitted first and the byte containing the most significant bit is stored in the highest memory address and transmitted last (e.g., for the value 0080h, the byte containing 80h is stored in the lowest memory address and the byte containing 00h is stored in the highest memory address).

3.1.72 livelock: A condition where two or more processes (e.g., connection requests) continually change their state in response to changes in other processes, resulting in none of the processes completing.

3.1.73 media: ~~Particular elements comprising the interconnect including copper cables, printed circuit boards, and other transmission line materials.~~

0.0.33 media: (1) General term referring to all the elements comprising the interconnect. This includes electrical cables, pc boards, connectors, hubs, and repeaters. (2) May be used in a narrow sense to refer to the bulk cable material in cable assemblies or PC board traces that are not part of the connectors.

3.1.74 message: Information sent between state machines.

3.1.75 most significant bit (MSB): In a binary code, the bit or bit position with the largest numerical weighting in a group of bits that, when taken as a whole, represent a numerical value (e.g., in the number 1000b, the bit that is set to one).

3.1.76 narrow link: A physical link that attaches a narrow port to another narrow port. See 4.1.3.

3.1.77 narrow port: A port that contains exactly one phy. See 4.1.3.

3.1.78 negotiated physical link rate: The current operational physical link rate established after speed negotiation between two phys.

3.1.79 nexus: A relationship between a SCSI initiator port and a SCSI target port that may extend to a logical unit and a task. See SAM-3.

3.1.80 object: An architectural abstraction or container that encapsulates data types, services, or other objects that are related in some way.

3.1.81 OOB sequence: A sequence where two phys exchange OOB signals. See 4.4.

3.1.82 OOB signal: Pattern of ALIGNs and idle time used during the link reset sequence. See 6.5.

3.1.83 partial pathway: The set of physical links participating in a connection request which has not reached a SAS endpoint (i.e., the connection request has been transmitted by the source device and confirmed as received by at least one expander device with AIP). See 4.1.9.

3.1.84 pathway: A set of physical links between a SAS initiator phy and a SAS target phy being used by a connection. See 4.1.9.

3.1.85 pathway blocked count: The number of times the port has retried this connection request due to receiving OPEN_REJECT (PATHWAY BLOCKED).

3.1.86 phy: A device object that is used to interface to other devices. See 4.1.2.

3.1.87 phy reset sequence: An OOB sequence (see 3.1.81) followed by a speed negotiation sequence (see 3.1.149). See 4.4.

3.1.88 physical link: Two differential signal pairs, one pair in each direction, that connect two physical phys. See 4.1.2.

3.1.89 physical phy: A phy (see 3.1.86) that contains a transceiver and electrically interfaces to a physical link to communicate with another physical phy. See 4.1.2.

3.1.90 port: A SAS port or an expander port. Each port contains one or more phys. See 4.1.3.

3.1.91 potential pathway: A set of physical links between a SAS initiator phy and a SAS target phy. See 4.1.9.

3.1.92 power on: Power being applied.

3.1.93 primitive: A dword starting with K28.5 or K28.3 followed by three data characters. See 7.2.

3.1.94 primitive sequence: A set of primitives treated as a single entity. See 7.2.4.

0.0.34   probability density function (PDF): a histogram of the jitter event population.

3.1.95 programmed maximum physical link rate: The maximum operational physical link rate of a phy (e.g., as programmed via the SMP PHY CONTROL function (see 10.4.3.10) or the Phy Control and Discover subpage (see 10.2.6.2.3)).

3.1.96 programmed minimum physical link rate: The minimum operational physical link rate of a phy (e.g., as programmed via the SMP PHY CONTROL function (see 10.4.3.10) or the Phy Control and Discover subpage (see 10.2.6.2.3)).

3.1.97 random jitter: Jitter that is assumed to have a Gaussian distribution.

3.1.98 rate: Data transfer rate of a physical link (e.g., 1,5 Gbps or 3,0 Gbps).

3.1.99 rate change delay time (RCDT): The time between rates during the speed negotiation sequence (see 6.6.4.2).

3.1.100 receiver: ~~The recipient of a signal.~~

0.0.35   receiver: an electronic component that converts an analog serial input signal to an electrical (retimed or non-retimed) logic output signal.

0.0.36   receiver device: the portion of the link downstream from the IR, XR or CR compliance point

3.1.101 reflection coefficient (ρ): The reflection coefficient of the transmission media (i.e., the ratio of the reflected voltage divided by the voltage applied to the transmission media).

0.0.37   reclocker: a type of repeater specifically designed to modify data edge timing such that the data edges have a defined timing relation with respect to a bit clock recovered from the (SAS) data at its input. Also referred to as clock tracking. SAS devices are not allowed to be reclockers. (SATA devices may be implemented as reclockers).

0.0.38   repeater: an active circuit designed to modify the (SAS) signals that pass through it by changing any or all of the following parameters of that signal: amplitude, slew rate, and edge to edge timing. Repeaters have jitter transfer characteristics. Types of repeaters include retimers, reclockers and amplifiers.

0.0.39   retimer (RT): a type of repeater specifically designed to modify data edge timing such that the output data edges have a defined timing relation with respect to a bit clock derived from a timing reference other than the (SAS) data at its input. A retimer shall be capable of inserting and removing words

from the (SAS) data passing through it. In the context of jitter methodology, a retimer resets the accumulation of jitter such that the output of a retimer has the jitter budget of a compliant transmitter. All SAS devices are required to be retimers.

3.1.102 request: A message passed from a higher layer state machine to a lower layer state machine, usually to initiate some action.

3.1.103 reset event: An event that triggers a hard reset (see 4.4.2) from a SAS device.

3.1.104 response: A message passed from a higher layer state machine to a lower layer state machine, usually in response to an indication (see 3.1.64).

0.0.40   return loss: the ratio (expressed in dB) of incident power to reflected power, when a component or assembly is introduced into a link or system. May refer to optical power or to electrical power in a specified frequency range.

0.0.41   run length: number of consecutive identical bits in the transmitted signal e.g., the pattern 0011111010 has a run lengths of five (5), one (1), and indeterminate run lengths at either end.

3.1.105 running disparity: A binary value indicating the cumulative encoded signal imbalance between the one and zero signal state of all characters since dword synchronization has been achieved (see 6.2).

3.1.106 SAS address: A worldwide unique name assigned to a SAS initiator port, SAS target port, expander device, SAS initiator device, or SAS target device. See 4.2.2.

3.1.107 SAS device: A SAS initiator device, SAS target device, or SAS target/initiator device.

3.1.108 SAS domain: The I/O system defined by this standard that may serve as an ATA domain and/or a SCSI domain. See 4.1.7.

3.1.109 SAS initiator device: A device containing SSP, STP, and/or SMP initiator ports in a SAS domain. See 4.1.4.

3.1.110 SAS initiator phy: A phy in a SAS initiator device.

3.1.111 SAS initiator port: An SSP initiator port, STP initiator port, and/or SMP initiator port in a SAS domain.

3.1.112 SAS phy: A phy in a SAS device that interfaces to a service delivery subsystem.

3.1.113 SAS port: A SAS initiator port, SAS target port, or SAS target/initiator port.

3.1.114 SAS target device: A device containing SSP, STP, and/or SMP target ports in a SAS domain. See 4.1.4.

3.1.115 SAS target phy: A phy in a SAS target device.

3.1.116 SAS target port: An SSP target port, STP target port, and/or SMP target port in a SAS domain.

3.1.117 SAS target/initiator device: A device that has all the characteristics of a SAS target device and a SAS initiator device.

3.1.118 SAS target/initiator port: A port that has all the characteristics of a SAS target port and a SAS initiator port in a SAS domain.

3.1.119 SATA device: A storage device that contains a SATA device port in an ATA domain (analogous to a SCSI target device).

3.1.120 SATA device port: A storage device object in an ATA domain that interfaces to the service delivery subsystem with SATA (analogous to a SCSI target port).

3.1.121 SATA host: A host device containing a SATA host port in an ATA domain (analogous to a SCSI initiator device).

3.1.122 SATA host port: A host device object in an ATA domain that interfaces to the service delivery subsystem with SATA (analogous to a SCSI initiator port).

3.1.123 SATA phy: A phy in a SATA device that interfaces to a service delivery subsystem (analogous to a SAS phy).

3.1.124 SATA port selector: A device that attaches to two SATA hosts and one SATA device, and provides the means for one SATA host to access the device at any given time (see SATA II: Port Selector).

3.1.125 scrambling: Modifying data by XORing each bit with a pattern generated by a linear feedback shift register to minimize repetitive character patterns. See 7.6.

3.1.126 SCSI device: A device that contains one or more SCSI ports that are connected to a service delivery subsystem and supports a SCSI application protocol. See SAM-3.

3.1.127 SCSI domain: An I/O system consisting of a set of SCSI devices that communicate with one another by means of a service delivery subsystem. See SAM-3.

3.1.128 SCSI initiator device: A SCSI device containing application clients and SCSI initiator ports that originates device service and task management requests to be processed by a SCSI target device and receives device service and task management responses from SCSI target devices. See SAM-3.

3.1.129 SCSI initiator port: A SCSI initiator device object that acts as the connection between application clients and the service delivery subsystem through which indications and responses are routed. See SAM-3.

3.1.130 SCSI port: A SCSI initiator port or a SCSI target port. See SAM-3.

3.1.131 SCSI target device: A SCSI device containing logical units and SCSI target ports that receives device service and task management requests for processing and sends device service and task management responses to SCSI initiator devices. See SAM-3.

3.1.132 SCSI target port: A SCSI target device object that contains a task router and acts as the connection between device servers and task managers and the service delivery subsystem through which requests and confirmations are routed. See SAM-3.

3.1.133 SCSI target/initiator device: A device that has all the characteristics of a SCSI target device and a SCSI initiator device. See SAM-3.

3.1.134 SCSI target/initiator port: A SCSI target/initiator device object that has all the characteristics of a SCSI target port and a SCSI initiator port. See SAM-3.

3.1.135 Serial ATA (SATA): The protocol defined by ATA/ATAPI-7 V3 (see 2.4).

3.1.136 Serial ATA Tunneled Protocol (STP): The protocol defined in this standard used by STP initiator ports to communicate with STP target ports in a SAS domain.

3.1.137 Serial Attached SCSI (SAS): The set of protocols and the interconnect defined by this standard.

3.1.138 Serial Management Protocol (SMP): The protocol defined in this standard used by SAS devices to communicate management information with other SAS devices in a SAS domain.

3.1.139 Serial SCSI Protocol (SSP): The protocol defined in this standard used by SCSI initiator ports to communicate with SCSI target ports in a SAS domain.

3.1.140 service delivery subsystem: The part of a SCSI I/O system that transmits information between a SCSI initiator port and a SCSI target port, or the part of an ATA I/O system that transmits information between an ATA host and an ATA device, or the part of a SAS I/O system that transmits information between a SAS initiator port and a SAS target port.

0.0.42   signal: the entire voltage waveform within a data pattern during transmission

0.0.43   signal level: the instantaneous intensity of the signal measured in the units appropriate for the type of transmission used at the point of the measurement. The most common signal level unit for electrical transmissions is voltage.

0.0.44   signal amplitude: a property of the overall signal that describes the peak or peak to peak values of the signal level . When signal transitions interfere with or overlap each other in a signal the effective signal amplitude may be expressed as a vertical waveform eye opening.

0.0.45   signal tolerance: the ability of the link downstream from the receive interoperability point to recover transmitted bits in an incoming data stream in the presence of a specified signal. Signal tolerance is measured by the amount of jitter required to produce a specified bit error ratio at a specified signal amplitude. The required signal tolerance performance depends on the frequency content of the jitter and on the amplitude of the signal. Since detection of bit errors is required to determine the signal tolerance, receivers embedded in an SAS Port require that the Port be capable of reporting bit errors. For receivers that are not embedded in an SAS Port the bit error detection and reporting may be accomplished by instrumentation attached to the output of the receiver. Signal tolerance is always measured using the minimum allowed signal amplitude and maximum allowed jitter unless otherwise specified. See also jitter tolerance.

3.1.141 SMP initiator phy: A SAS initiator phy in an SMP initiator port.

3.1.142 SMP initiator port: A SAS initiator device object in a SAS domain that interfaces to the service delivery subsystem with SMP.

3.1.143 SMP phy: A SAS phy in an SMP port.

3.1.144 SMP port: An SMP initiator port, SMP target port, or SMP target/initiator port.

3.1.145 SMP target phy: A SAS target phy in an SMP target port.

3.1.146 SMP target port: A SAS target device object in a SAS domain that interfaces to the service delivery subsystem with SMP.

3.1.147 SMP target/initiator port: A port that has all the characteristics of an SMP initiator port and an SMP target port.

3.1.148 speed negotiation lock time (SNLT): The maximum time during a speed negotiation window for a transmitter to reply with ALIGN (1) (see 6.6.4.2).

3.1.149 speed negotiation sequence: A sequence in which two phys negotiate the operational physical link rate. See 4.4.

3.1.150 speed negotiation transmit time (SNTT): The time during which ALIGN (0) or ALIGN (1) is transmitted during the speed negotiation sequence (see 6.6.4.2).

3.1.151 spread spectrum clocking: The technique of modulating the operating frequency of a transmitted signal to reduce the measured peak amplitude of radiated emissions.

3.1.152 SSP initiator phy: A SAS initiator phy in an SSP initiator port.

3.1.153 SSP initiator port: A SCSI initiator port in a SAS domain that implements SSP.

3.1.154 SSP phy: A SAS phy in an SSP port.

3.1.155 SSP port: An SSP initiator port, SSP target port, or SSP target/initiator port.

3.1.156 SSP target phy: A SAS target phy in an SSP target port.

3.1.157 SSP target port: A SCSI target port in a SAS domain that implements SSP.

3.1.158 SSP target/initiator port: A port that has all the characteristics of an SSP initiator port and an SSP target port.

3.1.159 STP initiator phy: A SAS initiator phy in an STP initiator port.

3.1.160 STP initiator port: A SAS initiator device object in a SAS domain that interfaces to the service delivery subsystem with STP.

3.1.161 STP phy: A SAS phy in an STP port.

3.1.162 STP port: An STP initiator port, STP target port, or STP target/initiator port.

3.1.163 STP target phy: A SAS target phy in an STP target port.

3.1.164 STP target port: A SAS target device object in a SAS domain that interfaces to the service delivery subsystem with STP.

3.1.165 STP target/initiator port: A port that has all the characteristics of an STP initiator port and an STP target port.

3.1.166 STP/SATA bridge: An expander device object containing an STP target port, a SATA host port, and the functions required to forward information between the STP target port and SATA host port to enable STP initiator ports in a SAS domain to communicate with SATA devices in an ATA domain.

3.1.167 subtractive routing attribute: The attribute of an edge expander phy that indicates it may be used by the expander connection manager to route connection requests not resolved using the direct routing method or table routing method. See 4.6.7.1.

3.1.168 subtractive routing method: The method the expander connection manager uses to route connection requests not resolved using the direct routing method or table routing method to an expander device. See 4.6.7.1.

3.1.169 table routing attribute: The attribute of an expander phy that indicates it may be used by the expander connection manager to route connection requests using an expander route table. See 4.6.7.1.

3.1.170 table routing method: The method the expander connection manager uses to route connection requests to an expander device using an expander route table. See 4.6.7.1.

3.1.171 task: An object within the logical unit representing the work associated with a command or group of linked commands.

3.1.172 task management function: A task manager service capable of being requested by an application client to affect the processing of one or more tasks. See SAM-3.

3.1.173 task manager: An agent within the device server that processes task management functions. See SAM-3.

3.1.174 throttling: Reducing the rate at which an STP initiator phy is sourcing dwords. See 7.17.2.

3.1.175 total jitter: ~~Measured jitter including deterministic jitter and random jitter.~~

3.1.176 transceiver: An object that contains both transmitter and receiver objects.

0.0.46   transmission bit: a symbol of duration one unit interval that represents one of two logical values, 0 or 1. For example, for 8b10b encoding, one tenth of a transmission character.

3.1.177 transmitter: ~~The source or generator of a signal.~~

0.0.47   transmitter : a circuit that converts a logic signal to a signal suitable for the communications media .

0.0.48   transmitter device: the portion of the link upstream from the IT, XT or CT compliance points

3.1.178 transmitter compliance transfer function (TCTF): The mathematical statement of the transfer function through which the transmitter shall be capable of producing acceptable signals as defined by a receive mask. See 5.3.11.

3.1.179 transport protocol service confirmation: A message passed from the transport layer to the application layer (i.e., from the SSP initiator port to the SCSI application client) that notifies the application layer that a SCSI transport protocol service has completed.

3.1.180 transport protocol service indication: A message passed from the transport layer to the application layer notifying the application layer (i.e., from the SSP target port to the SCSI device server) to begin a SCSI transport protocol service.

3.1.181 transport protocol service request: A message passed from the SCSI application layer to the SSP transport layer (i.e., from the SCSI application client to the SCSI initiator port) to begin a SCSI transport protocol service.

3.1.182 transport protocol service response: A message passed from the application layer to the transport layer (i.e., from the SCSI device server to the SSP target port) that completes the SCSI transport protocol service.

3.1.183 unit interval (UI): ~~The time required to transmit one bit on a physical link (e.g., 666,6 ps at 1,5 Gbps and 333,3 ps at 3,0 Gbps).~~

0.0.49   unit interval (UI): the normalized (dimensionless) nominal duration of a single transmission bit (e.g., 666,6 ps at 1,5 Gbps and 333,3 ps at 3,0 Gbps). Unit interval is a measure of time that has been normalized such that 1/Baud seconds is 1 UI.

3.1.184 valid dword: A dword that is not an invalid dword.

3.1.185 virtual phy: A phy (see 3.1.86) that interfaces to another virtual phy inside the same device. See 4.1.2.

3.1.186 wide link: A group of physical links that attaches a wide port to another wide port. See 4.1.3.

3.1.187 wide port: A port that contains more than one phy. See 4.1.3.

3.2 Symbols and abbreviations

See 2.1 for abbreviations of standards bodies (e.g., ISO). Additional symbols and abbreviations used in this standard include:

Abbreviation	Meaning
AA	ATA application layer (see 10.3)
A.C.	alternating current

Abbreviation	Meaning
ACK	acknowledge primitive (see 7.2.6.1)
AIP	arbitration in progress primitive (see 7.2.5.1)
ATA	AT attachment (see 3.1.4)
ATAPI	AT attachment packet interface
ATA/ATAPI-7	AT Attachment with Packet Interface - 7 standard (see 2.3)
AWG	American wire gauge
AWT	arbitration wait time
BCH	Bose, Chaudhuri and Hocquenghem code (see 4.2.3)
BER	~~bit error rate~~ bit error ratio
BIST	built in self test
BPP	broadcast primitive processor (see 3.1.9)
CDB	command descriptor block (see 3.1.13)
CJTPAT	~~compliant jitter test pattern~~ compliant jitter tolerance pattern (see 3.1.14)
CRC	cyclic redundancy check (see 3.1.20)
dB	decibel
D.C.	direct current (see 3.1.27)
Dxx.y	data character (see 3.1.22)
DDJ	data dependent jitter
DJ	deterministic jitter
ECM	expander connection manager (see 3.1.39)
ECR	expander connection router (see 3.1.40)
EMI	electromagnetic interference
EOAF	end of address frame primitive (see 7.2.5.6)
EOF	end of frame primitive (see 7.2.6.4)
FIS	frame information structure (see 3.1.51)
G1	generation 1 physical link rate (1,5 Gbps)
G2	generation 2 physical link rate (3,0 Gbps)
G3	generation 3 physical link rate (defined in a future version of this standard)
Gbps	gigabits per second (10^9 bits per second)
GHz	gigaherz (10^9 transitions per second)
ISI	intersymbol interference
IU	information unit (see 3.1.65)
kHz	kilohertz (10^3 bits per second)
Kxx.y	control character (see 3.1.19)
LED	light-emitting diode
LSB	least significant bit (see 0.0.21)
LUN	logical unit number
µA	microampere (10^{-6} amperes)
µs	microsecond (10^{-6} seconds)
MA	management application layer (see 10.4)
Mbaud	megabaud (10^6 transitions per second)

Abbreviation	Meaning
MBps	megabytes per second (10^6 bytes per second)
MHz	megahertz (10^6 bits per second)
MSB	most significant bit (see 3.1.75)
ms	millisecond (10^{-3} seconds)
MT	SMP transport layer state machines (see 9.4)
mV	millivolt (10^{-3} volts)
N/A	not applicable
NAA	name address authority
NAK	negative acknowledge primitive (see 7.2.6.5)
nF	nanofarad (10^{-9} Farads)
ns	nanosecond (10^{-9} seconds)
OOB	out-of-band
PL	port layer state machines (see 8.2)
PLL	phase lock loop
P-P	peak-to-peak
ppm	parts per million (10^{-6})
ps	picosecond (10^{-12} seconds)
ρ	reflection coefficient (rho)
RCDT	rate change delay time (see 3.1.99)
RRDY	receiver ready primitive (see 7.2.6.6)
RJ	random jitter
Rx	receive device
SA	SCSI application layer (see 10.2)
SAM-3	SCSI Architecture Model - 3 standard (see 2.3)
SAS	Serial Attached SCSI (see 3.1.137)
SATA	Serial ATA (see 3.1.135)
SBC-2	SCSI Block Commands - 2 standard (see 2.3)
SCSI	Small Computer System Interface family of standards
SL	link layer for SAS phys state machines (see 7.14)
SL_IR	link layer identification and hard reset state machines (see 7.9.5)
SMP	Serial Management Protocol (see 3.1.138), or link layer for SMP phys state machines (see 7.18.4)
SNLT	speed negotiation lock time (see 3.1.148)
SNTT	speed negotiation transmit time (see 3.1.150)
SOAF	start of address frame primitive (see 7.2.5.12)
SOF	start of frame primitive (see 7.2.6.7)
SP	phy layer state machine (see 6.7)
SP_DWS	phy layer dword synchronization state machine (see 6.8)
SPC-3	SCSI Primary Commands - 3 standard (see 2.3)
SSP	Serial SCSI Protocol (see 3.1.139), or link layer for SSP phys state machines (see 7.16.7)
ST	SSP transport layer state machines (see 9.2)

Abbreviation	Meaning
STP	Serial ATA Tunneled Protocol (see 3.1.136), or link layer for STP phys state machines (see 7.17.8)
s	second (unit of time)
TCTF	transmitter compliance transfer function (see 3.1.178)
TJ	total jitter
TT	STP transport layer state machines (see 9.3)
Tx	transmit device
UI	unit interval (see 3.1.183)
V	volt
VPD	vital product data (see 10.2.9)
XL	link layer for expander phys state machine (see 7.15)
XOR	exclusive logical OR
^	exclusive logical OR
x	multiplication
/	division

3.3 Keywords

3.3.1 ignored: A keyword used to describe an unused bit, byte, word, field or code value. The contents or value of an ignored bit, byte, word, field or code value shall not be examined by the receiving SCSI device and may be set to any value by the transmitting SCSI device.

3.3.2 invalid: A keyword used to describe an illegal or unsupported bit, byte, word, field or code value. Receipt of an invalid bit, byte, word, field or code value shall be reported as an error.

3.3.3 mandatory: A keyword indicating an item that is required to be implemented as defined in this standard.

3.3.4 may: A keyword that indicates flexibility of choice with no implied preference (equivalent to "may or may not").

3.3.5 may not: Keywords that indicate flexibility of choice with no implied preference (equivalent to "may or may not").

3.3.6 need not: Keywords indicating a feature that is not required to be implemented (equivalent to "is not required to").

3.3.7 obsolete: A keyword indicating that an item was defined in prior standards but has been removed from this standard.

3.3.8 optional: A keyword that describes features that are not required to be implemented by this standard. However, if any optional feature defined by this standard is implemented, then it shall be implemented as defined in this standard.

3.3.9 reserved: A keyword referring to bits, bytes, words, fields and code values that are set aside for future standardization. A reserved bit, byte, word or field shall be set to zero, or in accordance with a future extension to this standard. Recipients are not required to check reserved bits, bytes, words or fields for zero values. Receipt of reserved code values in defined fields shall be reported as error.