This document includes State Diagrams derived from the Serial ATA II Specification: Extensions to Serial ATA 1.0, T10 document number T10/03-264r1.

The diagrams are based on the T13 ATA-7 style of drawing state diagrams. Since the SATA II document (03-264r1) does not provide state machine diagrams in the traditional T10 or T13 formats, it is difficult to see the changes from SATA 1.0 to SATA II. These diagrams provide a simple means to compare the SATA II extensions to the SATA 1.0 document. The differences in SATA 1.0 state machines (Host PHY Initialization, Device Phy Initialization, and Device Idle) are shown in BLUE typeface. The new state machines are also included for FPDMA Command Queuing.

John Masiewicz
Western Digital
Host Phy Initialization State Machine

HP1: HR_reset
Transmit COMRESET
Clear Resume Pend=0

<table>
<thead>
<tr>
<th>Power-on reset or reset request</th>
</tr>
</thead>
<tbody>
<tr>
<td>xx:HP1</td>
</tr>
</tbody>
</table>

No Power-on reset & no reset request
HP1:HP2

No COMINIT from device & (ASR & >=10mS)
HP2:HP1

No COMINIT from device & (ASR & <=10mS)
HP3:HP1

HP2: HR_AwaitCOMINIT
Interface Quiescent

COMINIT from device
HP2:HP3

No COMINIT from device & (No ASR or <10mS)
HP2:HP2

No ASR & Async COMINIT
xx:HP3

HP3: HR_AwaitNoCOMINIT
Interface Quiescent

COMWAKE from device
HP5:HP7

No COMWAKE from device
HP5:HP6

No COMWAKE from device & (ASR & >=10mS) & (Resume Pending=0)
HP6:HP1

HP3:HP3

Calibration not complete
HP4:HP4

Calibration complete or bypass not implemented
HP4:HP5

HP4: HR_Calibrate
Perform Calibration

HP5: HR_COMWAKE
Transmit COMWAKE

COMWAKE from device
HP5:HP7

No COMWAKE from device
HP5:HP6

HP6: HR_AwaitCOMWAKE
Interface Quiescent

COMWAKE from device
HP6:HP7

No COMWAKE from device & (No ASR, or <10mS, or Resume Pending=1)
HP6:HP6

No ASR & Async COMINIT
xx:HP3

HP2:HP1

HP8: HR_AwaitALIGN
Xmit D10.2 at lowest speed

Wait elapsed & no ALIGN from device
HP8:HP1

ALIGN from device
HP8:HP9

Wait not elapsed & no ALIGN from device
HP8:HP8

< 3 back-to-back non-ALIGNs detected
HP10:HP10

3 back-to-back non-ALIGN detected
HP10:HP8

HP8:HP8

HP9: HR_AdjustSpeed
Interface Undefined, not Quiescent

Appropriate speed set
HP9:HP10

Appropriate speed not set
HP9:HP9

< 3 back-to-back non-ALIGNs
HP10:HP10

HP10: HR_SendALIGN
Transmit ALIGN at speed detected

HP10:HP10

HP11: HR_Ready
Xmit words from Link
If ASR, Clear Resume Pend=0

Partial from link
HP11:HP12

No Partial from link & COMWAKE from device
HP12:HP7

Slumber from link
HP11:HP13

No Partial from link & COMWAKE from device
HP12:HP12

No Partial from link & no COMWAKE from device
HP12:HP5

Partial from link
HP12:HP12

No Partial from link & no COMWAKE from device
HP12:HP5

No Slumber from link & COMWAKE from device
HP13:HP7

No Slumber from link & no COMWAKE from device
HP13:HP5

No Slumber from link
HP13:HP13

All States: See text for complete requirements
Device Phy Initialization State Machine

DP1: DR\textunderscore reset
- Interface Quiescent
- COMRESET or power-on reset
- xx:DP1
- Async Signal Recovery (ASR)
- DP9:DP1

DP2: DR\textunderscore COMINIT
- Transmit COMINIT
- Xmit COMINIT
- DP2:DP3

DP3: DR\textunderscore AwaitCOMWAKE
- Interface Quiescent
- No COMWAKE from host & (No ASR) or <10mS)
- DP3:DP1

DP4: DR\textunderscore AwaitNoCOMWAKE
- Interface Quiescent
- COMWAKE from host
- DP3:DP4

DP5: DR\textunderscore Calibrate
- Perform Calibration
- Calibration complete, not implemented, or bypass
- DP5:DP6
- Calibration not complete
- DP5:DP5

DP6: DR\textunderscore COMWAKE
- Send COMWAKE
- No COMWAKE and part of partial/slumber awake sequence
- DP4:DP6

DP7: DR\textunderscore Send\textunderscore ALIGN
- Transmit ALIGN
- COMWAKE sent
- DP6:DP7

DP8: DR\textunderscore ReduceSpeed
- Interface Quiescent
- Speed transition not complete
- DP8:DP8

DP9: DR\textunderscore Error
- Interface Quiescent
- Error not a failure to Awake, & ASR
- DP9:DP1 \rightarrow DR\textunderscore Reset
- Error not a failure to Awake, and No ASR
- DP9:DP9

DP10: DR\textunderscore Ready
- Xmit Words from Link
- Partial from link
- DP10:DP11
- No power management request and (No ASR, or received signal detected)
- DP10:DP10
- Slumber from link
- DP10:DP12

DP11: DR\textunderscore Partial
- Interface Quiescent
- DeviceNegates Partial & no COMWAKE from host
- DP11:DP6

DP12: DR\textunderscore Slumber
- Interface Quiescent
- DeviceNegates Slumber
- DP12:DP12

All States: See text for complete requirements
Device Idle State Diagram – Part 2 of 2

**DI2: Check_command**
Determine Command Protocol

- **DI2: Check_command**
  - Command Implemented and not SERVICE Command
  - **DI2: DND0** ➔ Non-data
  - **DI2: DPIO0** ➔ PIO_in
  - **DI2: DPIO10** ➔ PIO_data-in
  - **DI2: DPIOO0** ➔ PIO_data-out
  - **DI2: DDMAI0** ➔ DMA_in
  - **DI2: DDMAQI0** ➔ DMA_queued-in
  - **DI2: DDMAO0** ➔ DMA_out
  - **DI2: DDMAQO0** ➔ DMA_queued_out
  - **DI2: DPIOI0** ➔ PIO_in
  - **DI2: DPIOO0** ➔ PIO_out
  - READ DMA and no FPDMAQ command outstanding
  - WRITE DMA and no FPDMAQ command outstanding
  - PACKET and no FPDMAQ command outstanding
  - EXECUTE DEVICE DIAGNOSTIC and no FPDMAQ command outstanding
  - EXECUTE DEVICE DIAGNOSTIC and no FPDMAQ command outstanding
  - EXECUTE DEVICE DIAGNOSTIC and no FPDMAQ command outstanding
  - EXECUTE DEVICE DIAGNOSTIC and no FPDMAQ command outstanding
  - DEVICE RESET
  - **DI2: DDR0** ➔ Device_reset
  - READ FPDMA QUEUED EXT
  - **DI2: DFPDMAQ1** ➔ AddCommandToQueue
  - WRITE FPDMA QUEUED EXT
  - **DI2: DFPDMAQ1** ➔ AddCommandToQueue

**All States** see Text for Complete Requirements
Device Command Layer Protocol for Command Queuing Part 1 of 2

**DFPDMAQ1: AddCommandToQueue**
Append command device queue and store TAG value

- WRITE FPDMA QUEUED EXT command received → D12:DFPDMAQ1
- READ FPDMA QUEUED EXT command received → D12:DFPDMAQ1

**DFPDMAQ2: Clear InterfaceBsy**
Transmit Register DH FIS with BSY=0, DRQ=0, and I=0

- Command Appended → DFPDMAQ1: DFPDMAQ2
- FIS Transmission completed → DFPDMAQ2:DI0 → Device_idle

**DFPDMAQ12: BrokenHostClearBusy**
Halt processing and Transmit Register DH FIS with ERR=1, BSY=0, DRQ=0, I=0, ERROR=0x04

- Command Invalid → DFPDMAQ1: DFPDMAQ12
- FIS Transfer completed → DFPDMAQ12:DFPDMAQ13

**DFPDMAQ11: ERROR**
Halt Processing and send SDB FIS with appropriate status

- Not (READ/WRITE FPDMA QUEUED EXT) or DEVICE RESET command received, and FPDMAQ command outstanding → D12:DFPDMAQ13
- FIS Transmission completed → DFPDMAQ12:DFPDMAQ13

**DFPDMAQ13: WaitforClear**
Wait for host to READ LOG EXT w/Log Page 0x10h or SRST

- Any other command other than READ LOG EXT w/Log Page 0x10h → DFPDMAQ13:DFPDMAQ12
- SRST received → DFPDMAQ13:DSR0 → Software_reset_asserted

**DFPDMAQ14: SendQueueCleanACK**
Discard Pending Commands in Queue and Transmit Set Device Bits FIS with ERR=1, ERROR=0h, SActive=0xFFFFFFFF, I=0

- READ LOG EXT w/Log Page 0x10h command received → DFPDMAQ13:DFPDMAQ14
- FIS Transmission completed → DFPDMAQ14: DI0 → Check_command

**DFPDMAQ10: SendStatus**
Transmit SDB FIS with status and appropriate SActive bits

- One or more FPDMAQ EXT command completed with no error → D10:DFPDMAQ10
- FIS Transmission completed → DFPDMAQ10:DI0 → Device_idle

All States: See Text for Complete Requirements
DFPDMAQ3: DataPhaseReadSetup
Transmit First Party DMA Setup FIS to Host
Ready to Transmit data for READ FPDMA QUEUED EXT
- DI0: DFPDMAQ3
  - FIS Transmission complete: DFPDMAQ3: DFPDMAQ8
  - Transfer Count for DMA setup not complete and no errors: DFPDMAQ8:DFPDMAQ8

DFPDMAQ4: DataPhasePreWriteSetup
Determine if First Party Auto-Activate supported and enabled
Ready to Receive data for WRITE FPDMA QUEUED EXT
- DI0: DFPDMAQ4
  - First Party Auto-Activate supported and enabled: DFPDMAQ4: DFPDMAQ5
  - First Party Auto-Activate not supported or not enabled: DFPDMAQ4: DFPDMAQ6

DFPDMAQ5: DataPhaseWriteSetup
Transmit First Party DMA Setup FIS to Host
FIS Transmission Complete: DFPDMAQ4: DFPDMAQ9

DFPDMAQ6: DataPhaseOldWriteSetup
Transmit First Party DMA Setup FIS to Host
FIS Transmission Complete: DFPDMAQ6: DFPDMAQ7

DFPDMAQ7: DataPhaseXmitActivate
Transmit DMA Activate FIS to Host
DMA Activate FIS Transmission Complete: DFPDMAQ7: DFPDMAQ9
Data FIS received and transfer count for prior DMA setup not exhausted and no error: DFPDMAQ9: DFPDMAQ7

DFPDMAQ8: DataXmitRead
Transmit Data FIS to Host
Non-zero offsets enabled & Transfer count exhausted for DMA Setup, & data transfer for this command not complete, & no error
- DFPDMAQ9: DI0: Device_idle
Data transfer for this command complete, and no error
- DFPDMAQ9: DI0: Device_idle
Unrecoverable Error has occurred
- DFPDMAQ9: DI0: Device_idle

DFPDMAQ9: DataXmitWrite
Receive Data FIS from Host
Non-zero offsets enabled & Transfer count exhausted for DMA Setup, & data transfer for this command not complete, & no error
- DFPDMAQ9: DI0: Device_idle
Data transfer for this command complete, and no error
- DFPDMAQ9: DI0: Device_idle
Unrecoverable Error has occurred
- DFPDMAQ9: DI0: Device_idle

All States: see Text for Complete Requirements
Host Command Layer Protocol for Command Queuing

**HFDPMAQ1: AddCommandToQueue**
Append new command to Queue

**HFP: Idle**
Await FPDMAQ EXT command, or Device Interrupt, or Tag Availability

**HFPI0: HFPI0**
READ or WRITE FPDMA QUEUED EXT received from Higher level protocol

**HFPI0: HFPI0**
PRESETACTBit
Assign free TAG and Write SActive Register

**HFDPMAQ3: IssueCommand**
Command with assigned TAG awaiting issue and BSY=0 and not FPDMA Data Phase

**HFPI0: HFPI0**
DeviceINT
Read Status Register and save as SavedStatus

**HFPI0: HFPI0**
DeviceINT
Await FPDMA EXT command, or Device Interrupt, or Tag Availability

**HFPI0: HFPI0**
One or more commands completed

**HFPI0: HFPI0**
CompleteRequests1
Identify Completed Commands

**HFPI0: HFPI0**
CompleteRequests2
Retire TAGs and Update Stored SActive Register

**HFPI0: HFPI0**
CompleteRequests3
Test ERR in SavedStatus

**HFPI0: HFPI0**
CompleteRequests4
Retire TAGs and Update Stored SActive Register

**HFPI0: HFPI0**
CompleteRequests5
Test ERR in SavedStatus

**HFPI0: HFPI0**
CompleteRequests6
Retire Failed Command, flush pending Queue and Clean-up

**All States:** See Text for complete Requirements