To: T10 Technical Committee
From: Barry Olawsky, HP (barry.olawsky@hp.com)
Date: 14 June 2004
Subject: T10/04-182r0 SAS-1.1 Internal Wide Connector/Cable Proposal Feasibility Study

Revision History
Revision 0 (14 June 2004) First revision

Related Documents
sas1r05 - Serial Attached SCSI 1.1 revision 5
03-240r1 - SAS-1.1 Internal wide connector and cable (Rob Elliott, Hewlett Packard)
sff-8484r0.5 - Multi Lane Internal Serial Attachment Connector (Brian Miller, Amphenol)

Overview
Provide technical data (electrical) to support the feasibility of proposal 03-240r1. Specifically, demonstrate implementations of the proposal comply with existing sas1r05 electrical specifications and do not exceed the internal compliance channel budget. The intent of this data is not to provide an electrical cable assembly specification but to prove the validity of 03-240r1 as an internal interconnect option.

Suggested Changes
None. Not within scope of this document.
Internal 4-Lane Signaling Budget Feasibility Study

Prepared by Barry Olawsky
Hewlett Packard
May, 2004
Internal 4-lane Concept

- Low-end server market
- Motherboard or host bus adapter cabled to small internal drive backplane
- Additional connector interface and trace route when compared to single lane design
Purpose of Study

- Evaluate signaling margins (amplitude and data dependent jitter)
- Determine feasibility of design configuration
- Compare to compliance channel
Test Parameters

• Measurements using actual hardware
• Six backplane configurations tested
  • 4” and 8” of 0.006”, 0.013”, and 0.022”
• Two motherboard/HBA configurations tested
  • 3” and 6” of 0.006”
• 1m cable between host and backplane
• Host: right-angle, Backplane: vertical
• 400mV transmitter output
• Lonebit pattern of (D12.0-, D11.4+)
Sample Backplanes
Test Methods

• Focus testing on worst and best case configurations
• De-embed losses of test fixturing where possible
• Correlate measurements from different instrumentation where possible
• Signal sources
  • D3186, 100ps ref phy, MAX3785 buffer
• Instrumentation
  • Amplitude: CSA8000, Jitter: CSA8000 and TDS scope
### Amplitude with 400mV transmitter (mVpp)

<table>
<thead>
<tr>
<th>Configuration</th>
<th>3 Gbps</th>
<th>1.5 Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D3186</td>
<td>D3186 + buffer</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .022 backplane</td>
<td>270</td>
<td>350</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .013 backplane</td>
<td>260</td>
<td>357</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .006 backplane</td>
<td>257</td>
<td>339</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 8&quot; of .022 backplane</td>
<td>253</td>
<td>339</td>
</tr>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .022 backplane</td>
<td>242</td>
<td>220</td>
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<tr>
<td>6&quot; of .006 host &gt; cable &gt; (buffer) &gt; 8&quot; of .013 backplane</td>
<td>218</td>
<td>199</td>
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<td>208</td>
<td>189</td>
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<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 8&quot; of .013 backplane</td>
<td>320</td>
<td>358</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 8&quot; of .006 backplane</td>
<td>305</td>
<td>350</td>
</tr>
<tr>
<td>4&quot; of .022 &gt; (buffer) &gt; cable &gt; 3&quot; of .006 host</td>
<td>284</td>
<td>343</td>
</tr>
<tr>
<td>8&quot; of .006 &gt; (buffer) &gt; cable &gt; 3&quot; of .006 host</td>
<td>284</td>
<td>339</td>
</tr>
<tr>
<td>8&quot; of .006 &gt; (buffer) &gt; cable &gt; 6&quot; of .006 host</td>
<td>255</td>
<td>322</td>
</tr>
<tr>
<td>4&quot; of .022 &gt; (buffer) &gt; cable &gt; 6&quot; of .006 host</td>
<td>254</td>
<td>320</td>
</tr>
<tr>
<td>4&quot; of .013 &gt; (buffer) &gt; cable &gt; 6&quot; of .006 host</td>
<td>253</td>
<td>322</td>
</tr>
<tr>
<td>4&quot; of .006 &gt; (buffer) &gt; cable &gt; 6&quot; of .006 host</td>
<td>253</td>
<td>320</td>
</tr>
<tr>
<td>1m cable (Vert pcb connectors)</td>
<td>311</td>
<td>297</td>
</tr>
<tr>
<td>1m cable (RA pcb connectors)</td>
<td>304</td>
<td>292</td>
</tr>
<tr>
<td>4&quot; of .022 backplane</td>
<td>368</td>
<td>369</td>
</tr>
<tr>
<td>4&quot; of .013 backplane</td>
<td>353</td>
<td>364</td>
</tr>
<tr>
<td>4&quot; of .006 backplane</td>
<td>353</td>
<td>360</td>
</tr>
<tr>
<td>8&quot; of .022 backplane</td>
<td>342</td>
<td>357</td>
</tr>
<tr>
<td>8&quot; of .013 backplane</td>
<td>328</td>
<td>349</td>
</tr>
<tr>
<td>8&quot; of .006 backplane</td>
<td>318</td>
<td>339</td>
</tr>
</tbody>
</table>
Amplitude Measurement Notes

- Buffer and 100ps phy de-embedding with scaling
- The configuration column describes the ordering of components in the path from signal source to measurement instrumentation. Data in columns labeled as “+buffer” include buffer and other columns DO NOT.
- “Cable only” measurements included for reference only
- “Backplane only” measurements included for reference only
- Relative bit amplitudes using cable, backplane and host bus adapter configurations should not be used to budget individual portions to the design. Where appropriate, a network analyzer would have provided a more accurate assessment.
Cable/Short Backplane Evaluation - Receive Amplitude
With Lonebit Pattern (3Gb) in mV

- 6" of .006 host > cable > 8" of .006 backplane
- 6" of .006 host > cable > 8" of .013 backplane
- 6" of .006 host > cable > 4" of .022 backplane
- 3" of .006 host > cable > 8" of .022 backplane
- 3" of .006 host > cable > 4" of .006 backplane
- 3" of .006 host > cable > 4" of .013 backplane
- 3" of .006 host > cable > 4" of .022 backplane
- 3" of .006 host > cable > 8" of .022 backplane
- 1m cable (RA pcb connectors)
- 1m cable (Vert pcb connectors)

100ps phy
D3186
### Cable/Short Backplane Evaluation - Receiver Amplitude

With Lonebit Pattern (1.5Gb) in mV

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Receiver Amplitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; 8&quot; of .006 backplane</td>
<td>260 mV</td>
</tr>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; 8&quot; of .013 backplane</td>
<td>270 mV</td>
</tr>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; 4&quot; of .022 backplane</td>
<td>280 mV</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; 8&quot; of .022 backplane</td>
<td>290 mV</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; 4&quot; of .006 backplane</td>
<td>300 mV</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; 4&quot; of .013 backplane</td>
<td>310 mV</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; 4&quot; of .022 backplane</td>
<td>320 mV</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; 8&quot; of .006 backplane</td>
<td>330 mV</td>
</tr>
<tr>
<td>1m cable (RA pcb connectors)</td>
<td>340 mV</td>
</tr>
<tr>
<td>1m cable (Vert pcb connectors)</td>
<td>350 mV</td>
</tr>
</tbody>
</table>
Cable/Short Backplane Evaluation - Bit Amplitude Reduction With Lonebit Pattern (3Gb)

- 6" of .006 host > cable > 8" of .006 backplane
- 6" of .006 host > cable > 8" of .013 backplane
- 6" of .006 host > cable > 4" of .022 backplane
- 3" of .006 host > cable > 8" of .022 backplane
- 3" of .006 host > cable > 4" of .006 backplane
- 3" of .006 host > cable > 4" of .013 backplane
- 3" of .006 host > cable > 4" of .022 backplane
- 3" of .006 host > cable > 8" of .022 backplane
- 1m cable (RA pcb connectors)
- 1m cable (Vert pcb connectors)

Legend:
- 100ps phy
- D3186
- D3186, backplane only
# Data Dependent Jitter (ps)

<table>
<thead>
<tr>
<th>Configuration</th>
<th>3 Gbps</th>
<th>1.5 Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D3186</td>
<td>D3186</td>
</tr>
<tr>
<td></td>
<td>rt scope</td>
<td>CSA buffer</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .022 backplane</td>
<td>24</td>
<td>13</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .013 backplane</td>
<td>24</td>
<td>14</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .006 backplane</td>
<td>24</td>
<td>16</td>
</tr>
<tr>
<td>3&quot; of .006 host &gt; cable &gt; (buffer) &gt; 8&quot; of .022 backplane</td>
<td>28</td>
<td>17</td>
</tr>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .022 backplane</td>
<td>27</td>
<td>18</td>
</tr>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; (buffer) &gt; 8&quot; of .013 backplane</td>
<td>33</td>
<td>25</td>
</tr>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; (buffer) &gt; 8&quot; of .006 backplane</td>
<td>38</td>
<td>28</td>
</tr>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .013 backplane</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; (buffer) &gt; 4&quot; of .006 backplane</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>6&quot; of .006 host &gt; cable &gt; (buffer) &gt; 8&quot; of .022 backplane</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>4&quot; of .022 &gt; (buffer) &gt; cable &gt; 6&quot; of .006 host</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>8&quot; of .006 &gt; (buffer) &gt; cable &gt; 6&quot; of .006 host</td>
<td>37</td>
<td>19</td>
</tr>
<tr>
<td>4&quot; of .022 &gt; (buffer) &gt; cable &gt; 3&quot; of .006 host</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>8&quot; of .006 &gt; (buffer) &gt; cable &gt; 3&quot; of .006 host</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>1m cable (RA pcb connectors)</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>1m cable (Vert pcb connectors)</td>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>
Jitter Measurement Notes

- CSA measurement intended for correlation only - Cursors manually placed on farthest crossing points
- The configuration column describes the ordering of components in the path from signal source to measurement instrumentation. Data in columns labeled as “+buffer” include buffer and other columns DO NOT.
- “Cable only” measurements included for reference only
- Raw output of 100ps reference PHY was measured at 14ps of data dependent jitter.
Cable/Short Backplane Evaluation - Jitter due to ISI at 3Gb with Lonebit Pattern (in ps)

- 6" of .006 host > cable > 8" of .006 backplane
- 6" of .006 host > cable > 8" of .013 backplane
- 6" of .006 host > cable > 4" of .022 backplane
- 3" of .006 host > cable > 8" of .022 backplane
- 3" of .006 host > cable > 4" of .006 backplane
- 3" of .006 host > cable > 4" of .013 backplane
- 3" of .006 host > cable > 4" of .022 backplane
- 6" of .006 host > cable > 4" of .022 backplane
- 6" of .006 host > cable > 8" of .013 backplane
- 6" of .006 host > cable > 8" of .006 backplane
- 1m cable (Vert pcb connectors)
- 1m cable (RA pcb connectors)

Bar chart showing jitter in ps for different cable and backplane configurations.
Cable/Short Backplane Evaluation - Jitter due to ISI at 1.5Gb with Lonebit Pattern (in ps)

- 6" of .006 host > cable > 8" of .006 backplane
- 6" of .006 host > cable > 8" of .013 backplane
- 6" of .006 host > cable > 4" of .022 backplane
- 3" of .006 host > cable > 8" of .022 backplane
- 3" of .006 host > cable > 4" of .006 backplane
- 3" of .006 host > cable > 4" of .013 backplane
- 3" of .006 host > cable > 4" of .022 backplane
- 1m cable (Vert pcb connectors)
- 1m cable (RA pcb connectors)

Graph showing various configurations with their corresponding jitter in ps.
Internal 4x Solution Loss (includes backplane & host trace)

-15.000
-13.000
-11.000
-9.000
-7.000
-5.000
-3.000
-1.000
1.000

0
500
1000
1500
2000
2500
3000
3500
4000

MHz

db

03mRefDes
1mRefDes
TCTF
Conclusions

- SATA amplitude margins at 3Gb insufficient to support a 1m cable + worst case backplane trace + additional connector interface
- Design meets SAS-to-SAS and Gen1SATA-to-Expander margins
- Lower loss than TCTF at 1.5GHz and 3GHz
- TCTF comparison may justify modification of design criteria of loss model