To: T10 Technical Committee
From: Barry Olawsky, HP (barry.olawsky@hp.com)
Date: 14 June 2004
Subject: T10/04-182r0 SAS-1.1 Internal Wide Connector/Cable Proposal Feasibility Study

Revision History
Revision 0 (14 June 2004) First revision

Related Documents
sas1r05 - Serial Attached SCSI 1.1 revision 5
03-240r1 - SAS-1.1 Internal wide connector and cable (Rob Elliott, Hewlett Packard)
sff-8484r0.5 - Multi Lane Internal Serial Attachment Connector (Brian Miller, Amphenol)

Overview
Provide technical data (electrical) to support the feasibility of proposal 03-240r1. Specifically, demonstrate implementations of the proposal comply with existing sas1r05 electrical specifications and do not exceed the internal compliance channel budget. The intent of this data is not to provide an electrical cable assembly specification but to prove the validity of 03-240r1 as an internal interconnect option.

Suggested Changes

None. Not within scope of this document.

Internal 4-Lane Signaling Budget Feasibility Study

Prepared by Barry Olawsky
Hewlett Packard
May, 2004

Internal 4-lane Concept

- Low-end server market
- Motherboard or host bus adapter cabled to small internal drive backplane
- Additional connector interface and trace route when compared to single lane design

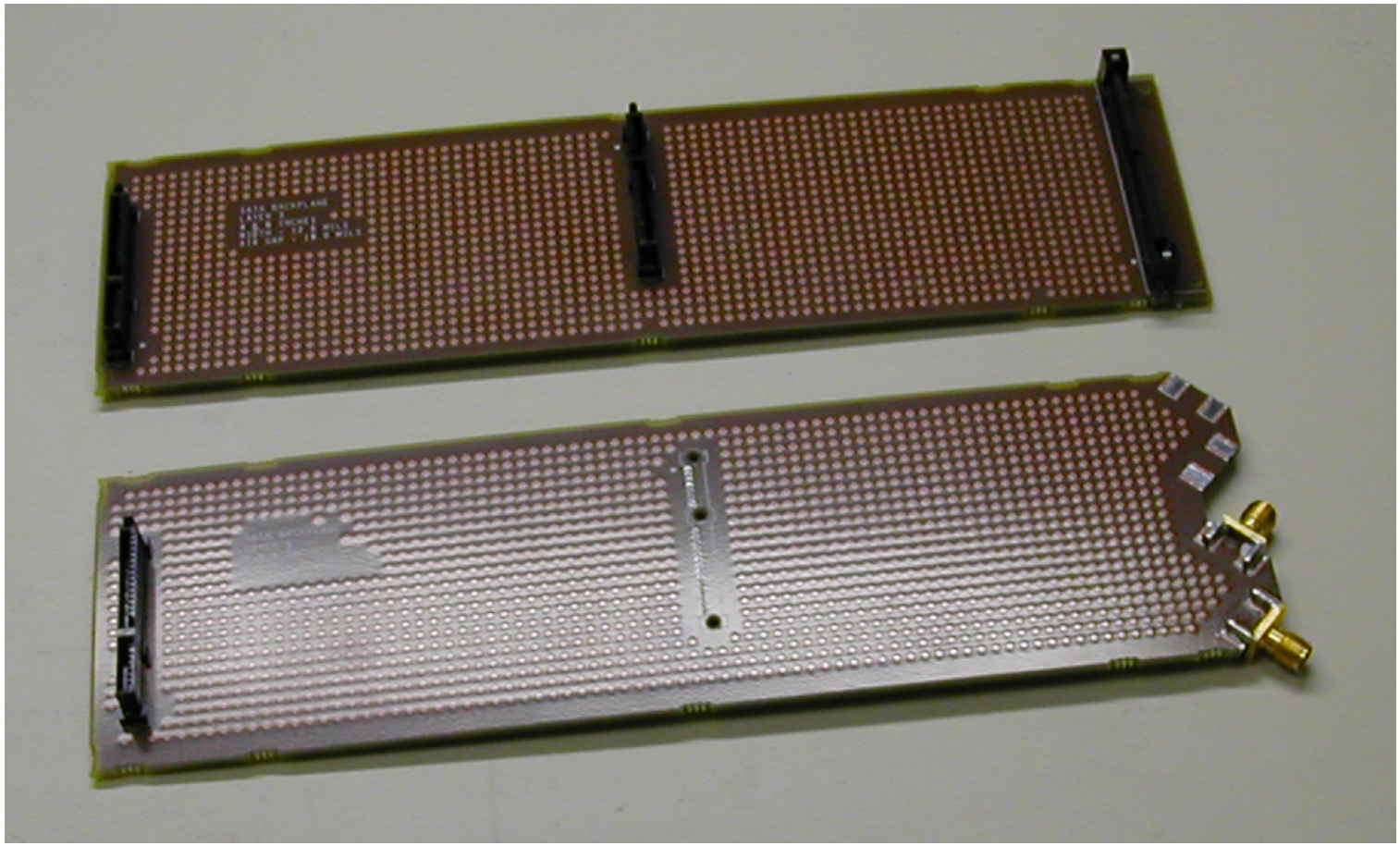
Purpose of Study

- Evaluate signaling margins (amplitude and data dependent jitter)
- Determine feasibility of design configuration
- Compare to compliance channel

Test Parameters

- Measurements using actual hardware
- Six backplane configurations tested
  - 4” and 8” of 0.006”, 0.013”, and 0.022”
- Two motherboard/HBA configurations tested
  - 3” and 6” of 0.006”
- 1m cable between host and backplane
- Host: right-angle, Backplane: vertical
- 400mV transmitter output
- Lonebit pattern of (D12.0-, D11.4+)

Sample Backplanes



Test Methods

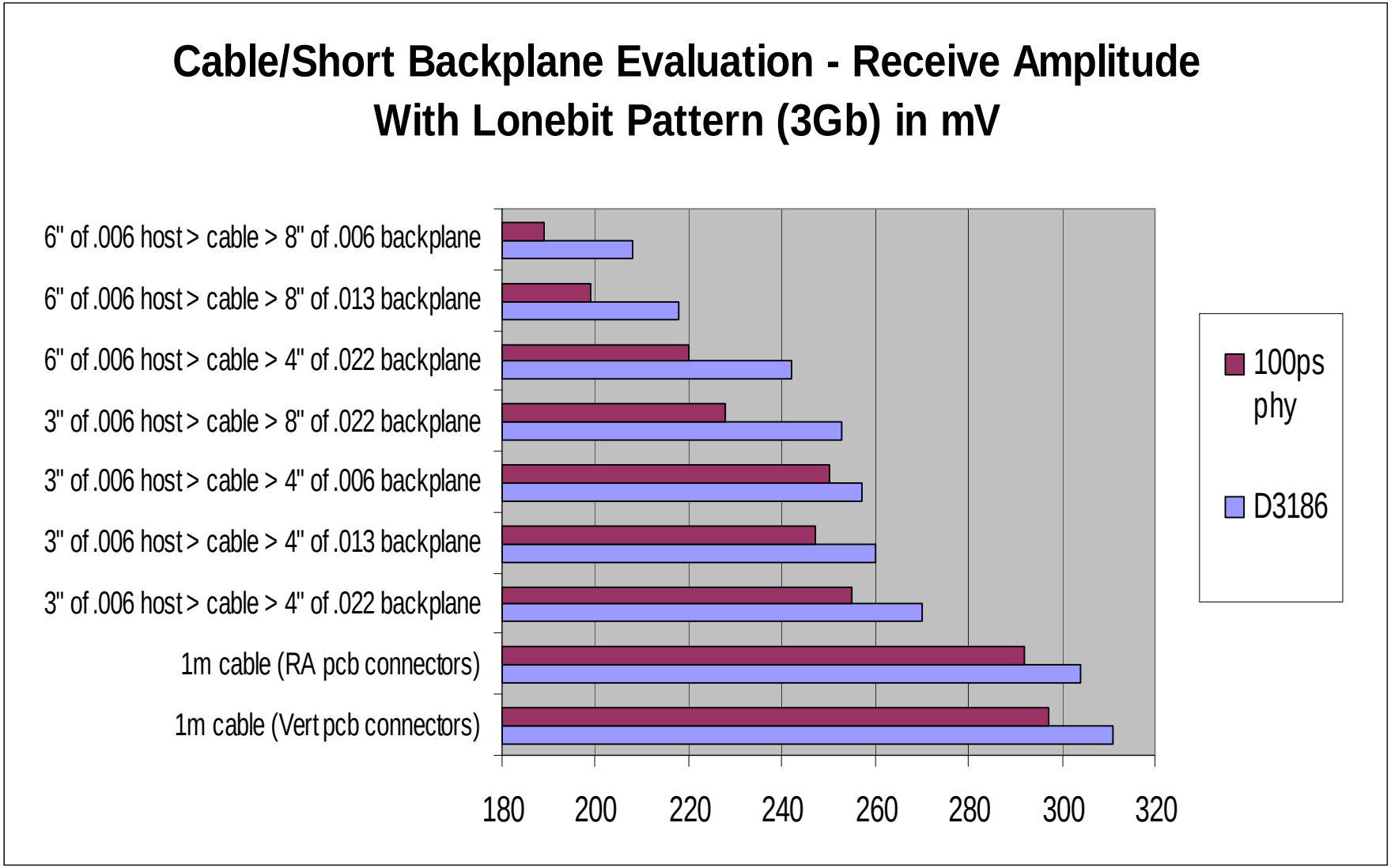
- Focus testing on worst and best case configurations
- De-embed losses of test fixturing where possible
- Correlate measurements from different instrumentation where possible
- Signal sources
  - D3186, 100ps ref phy, MAX3785 buffer
- Instrumentation
  - Amplitude: CSA8000, Jitter: CSA8000 and TDS scope

Amplitude with 400mV transmitter (mVpp)

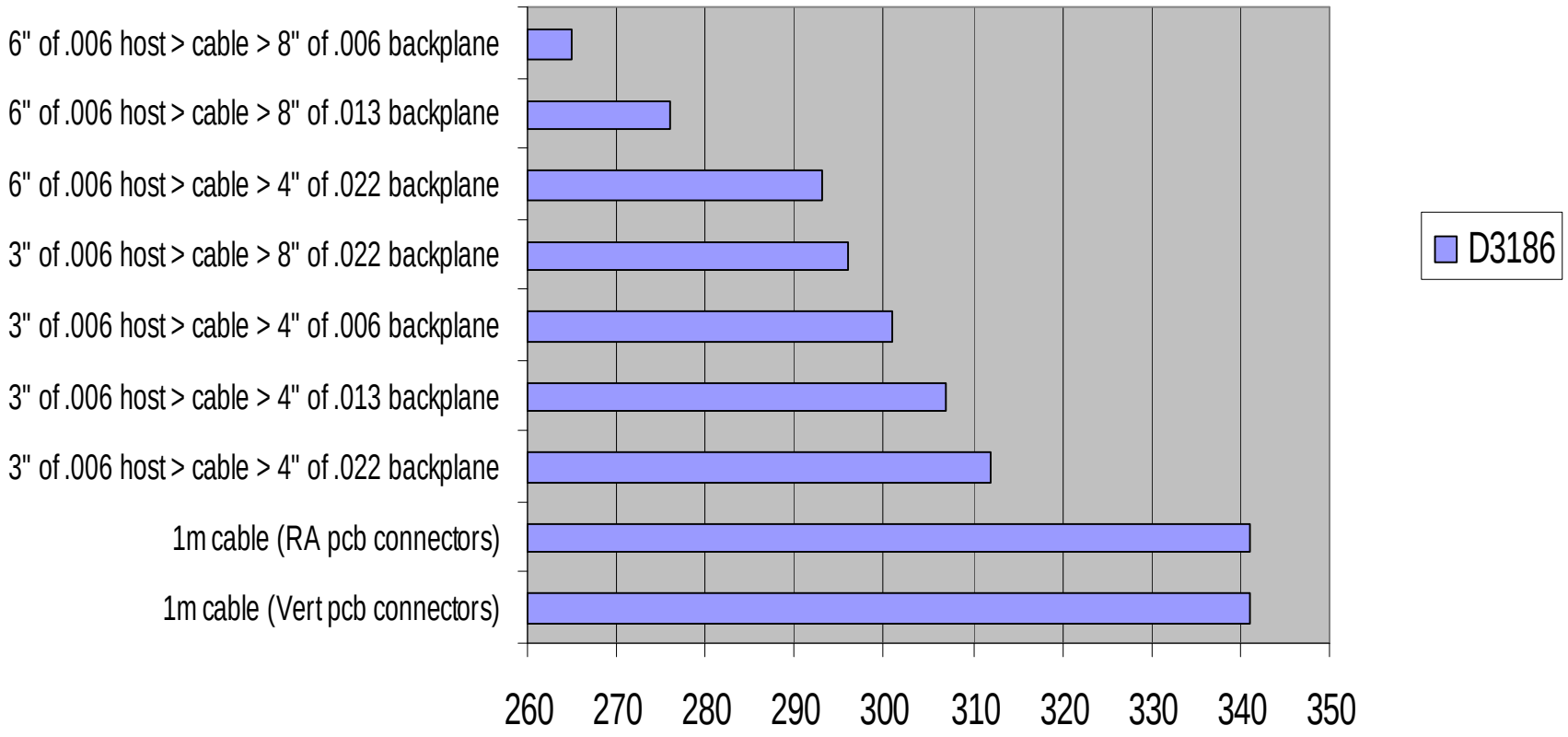
Configuration	3 Gbps			1.5 Gbps	
	D3186	D3186 + buffer	100ps phy	D3186	D3186 + buffer
3" of .006 host > cable > (buffer) > 4" of .022 backplane	270	350	255	312	380
3" of .006 host > cable > (buffer) > 4" of .013 backplane	260	357	247	307	374
3" of .006 host > cable > (buffer) > 4" of .006 backplane	257	339	250	301	374
3" of .006 host > cable > (buffer) > 8" of .022 backplane	253	339	228	296	370
6" of .006 host > cable > (buffer) > 4" of .022 backplane	242		220	293	
6" of .006 host > cable > (buffer) > 8" of .013 backplane	218		199	276	
6" of .006 host > cable > (buffer) > 8" of .006 backplane	208		189	265	
3" of .006 host > cable > (buffer) > 8" of .013 backplane		320			358
3" of .006 host > cable > (buffer) > 8" of .006 backplane		305			350
4" of .022 > (buffer) > cable > 3" of .006 host		284			343
8" of .006 > (buffer) > cable > 3" of .006 host		284			339
8" of .006 > (buffer) > cable > 6" of .006 host		255			322
4" of .022 > (buffer) > cable > 6" of .006 host		254			320
4" of .013 > (buffer) > cable > 6" of .006 host		253			322
4" of .006 > (buffer) > cable > 6" of .006 host		253			320
1m cable (Vert pcb connectors)	311		297	341	
1m cable (RA pcb connectors)	304		292	341	
4" of .022 backplane	368			369	
4" of .013 backplane	353			364	
4" of .006 backplane	353			360	
8" of .022 backplane	342			357	
8" of .013 backplane	328			349	
8" of .006 backplane	318			339	

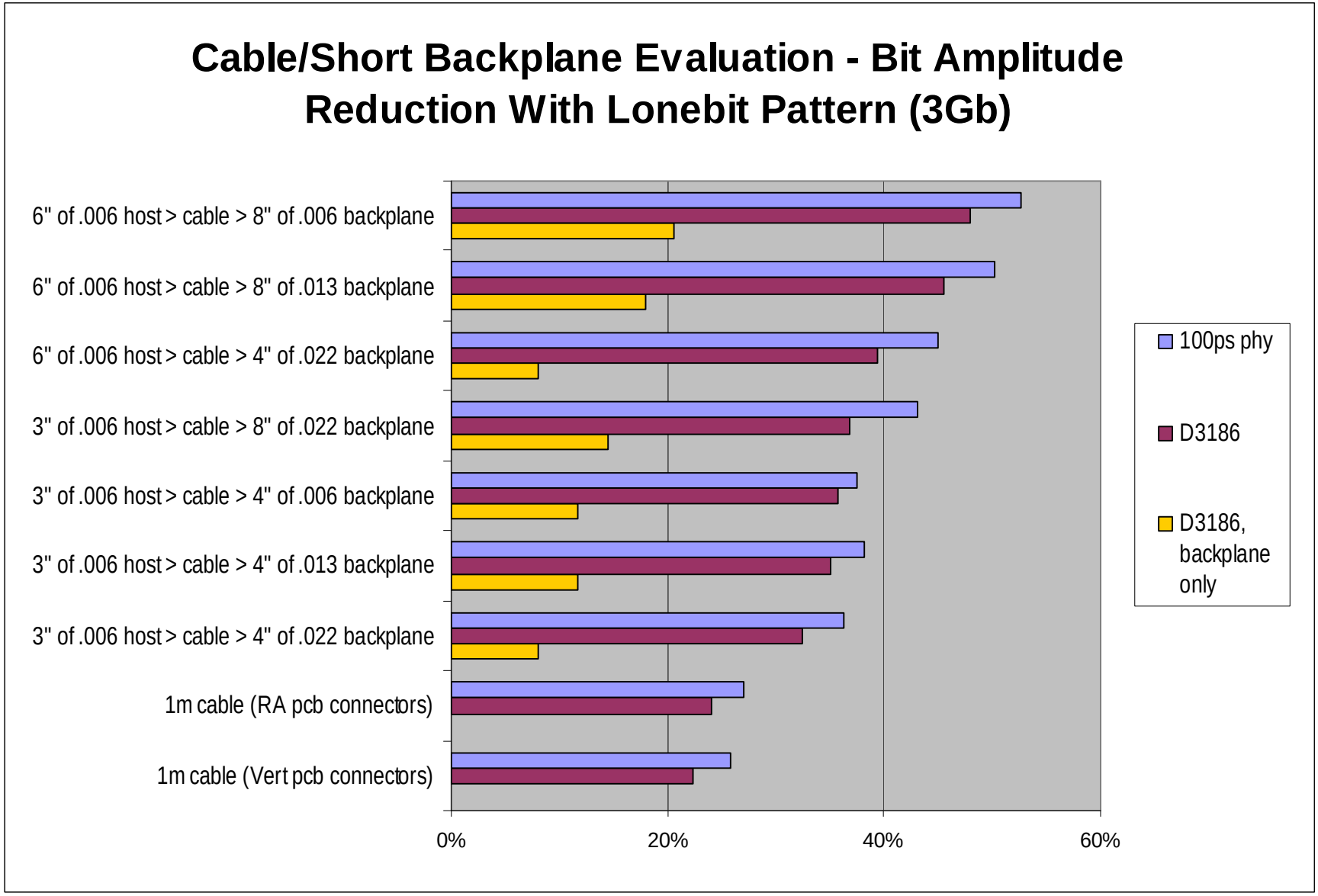
Amplitude Measurement Notes

- Buffer and 100ps phy de-embedding with scaling
- The configuration column describes the ordering of components in the path from signal source to measurement instrumentation. Data in columns labeled as “+buffer” include buffer and other columns DO NOT.
- “Cable only” measurements included for reference only
- “Backplane only” measurements included for reference only
- Relative bit amplitudes using cable, backplane and host bus adapter configurations should not be used to budget individual portions to the design. Where appropriate, a network analyzer would have provided a more accurate assessment.


Cable/Short Backplane Evaluation - Receive Amplitude
With Lonebit Pattern (3Gb) in mV
6" of .006 host > cable > 8" of .006 backplane
6" of .006 host > cable > 8" of .013 backplane
6" of .006 host > cable > 4" of .022 backplane
3" of .006 host > cable > 8" of .022 backplane
3" of .006 host > cable > 4" of .006 backplane
3" of .006 host > cable > 4" of .013 backplane
3" of .006 host > cable > 4" of .022 backplane
1m cable (RA pcb connectors)
1m cable (Vert pcb connectors)
180
200
220
240
260
280
300
320
100ps phy
D3186

Cable/Short Backplane Evaluation - Receiver Amplitude With Lonebit Pattern (1.5Gb) in mV



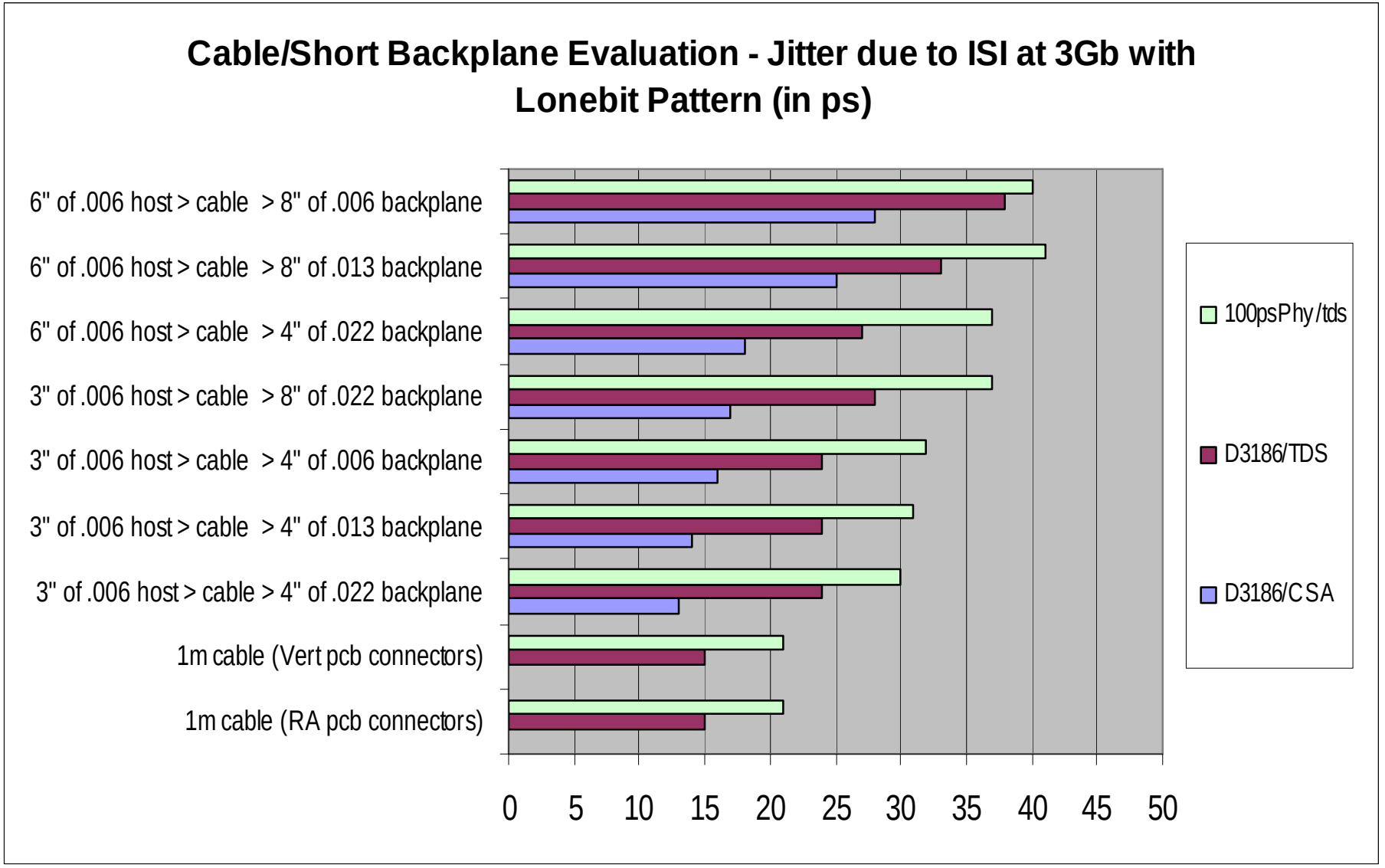

Cable/Short Backplane Evaluation - Bit Amplitude Reduction With Lonebit Pattern (3Gb)
6" of .006 host > cable > 8" of .006 backplane
6" of .006 host > cable > 8" of .013 backplane
6" of .006 host > cable > 4" of .022 backplane
3" of .006 host > cable > 8" of .022 backplane
3" of .006 host > cable > 4" of .006 backplane
3" of .006 host > cable > 4" of .013 backplane
3" of .006 host > cable > 4" of .022 backplane
1m cable (RA pcb connectors)
1m cable (Vert pcb connectors)
0%
20%
40%
60%
100ps phy
D3186
D3186, backplane only

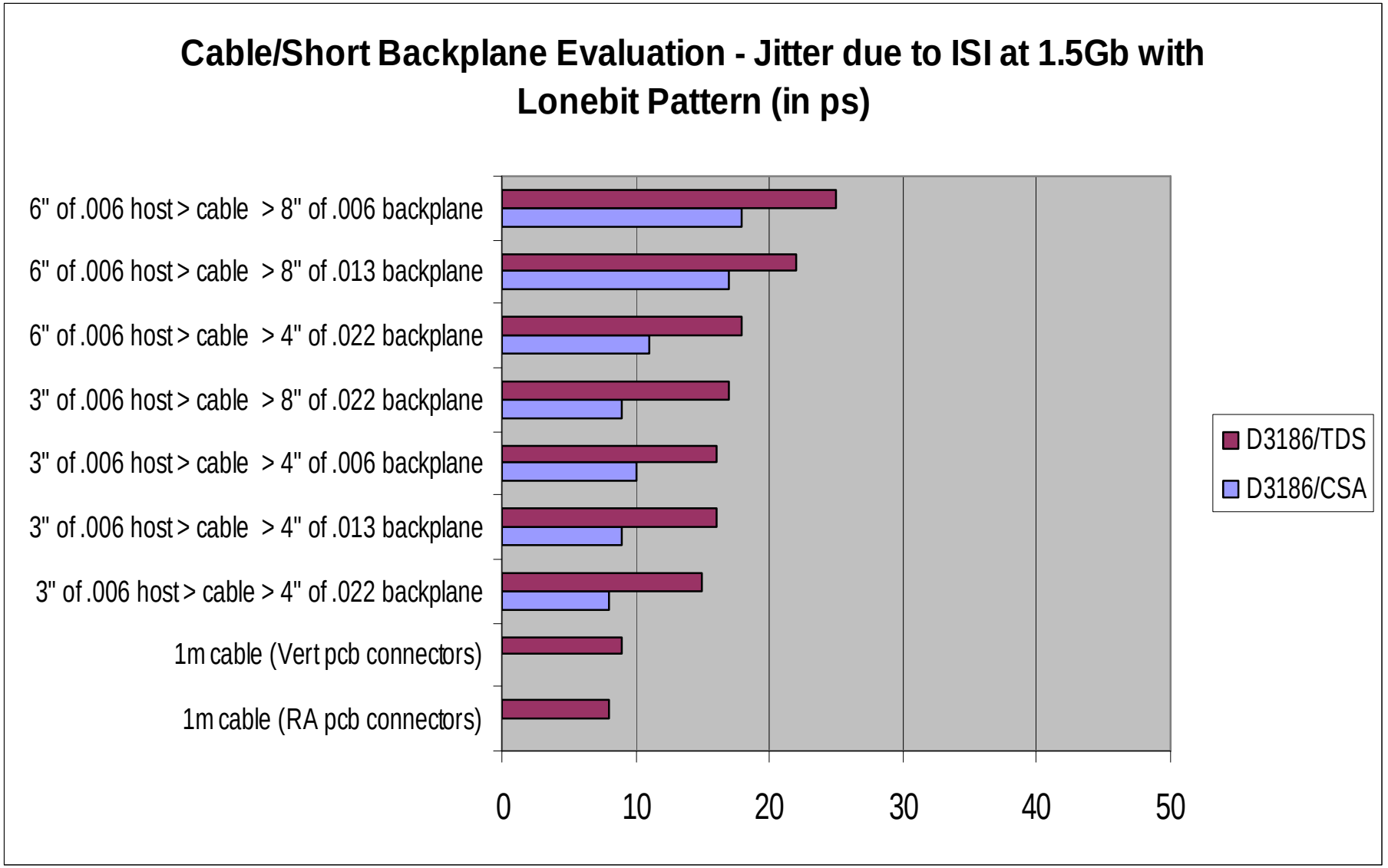
Data Dependent Jitter (ps)

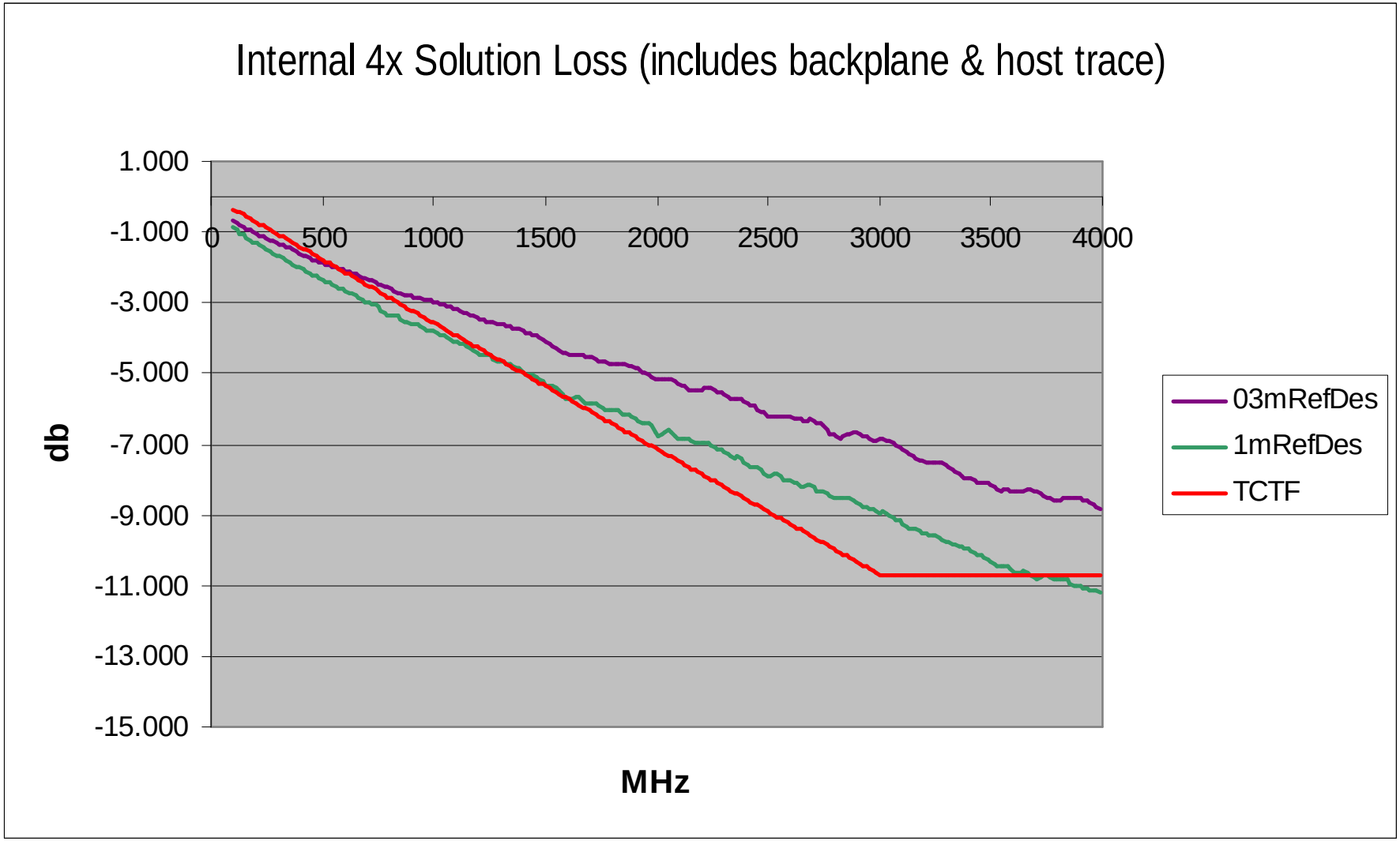
Configuration	3 Gbps					1.5 Gbps		
	D3186 rt scope	D3186 CSA	D3186 + buffer	100ps phy	100ps phy + buffer	D3186 rt scope	D3186 CSA	D3186 + buffer
3" of .006 host > cable > (buffer) > 4" of .022 backplane	24	13		30	27	15	8	
3" of .006 host > cable > (buffer) > 4" of .013 backplane	24	14		31	25	16	9	
3" of .006 host > cable > (buffer) > 4" of .006 backplane	24	16		32	23	16	10	
3" of .006 host > cable > (buffer) > 8" of .022 backplane	28	17		37	25	17	9	
6" of .006 host > cable > (buffer) > 4" of .022 backplane	27	18	10	37	25	18	11	7
6" of .006 host > cable > (buffer) > 8" of .013 backplane	33	25	12	41	25	22	17	9
6" of .006 host > cable > (buffer) > 8" of .006 backplane	38	28	14	40	30	25	18	10
6" of .006 host > cable > (buffer) > 4" of .013 backplane			11					8
6" of .006 host > cable > (buffer) > 4" of .006 backplane			11					7
6" of .006 host > cable > (buffer) > 8" of .022 backplane			12					8
4" of .022 > (buffer) > cable > 6" of .006 host			17					12
8" of .006 > (buffer) > cable > 6" of .006 host	37	19	17	46	27	25	29	13
4" of .022 > (buffer) > cable > 3" of .006 host	22		14	28	22	15		12
8" of .006 > (buffer) > cable > 3" of .006 host			14					11
1m cable (RA pcb connectors)	15			21		8		
1m cable (Vert pcb connectors)	15			21		9		

Jitter Measurement Notes

- CSA measurement intended for correlation only - Cursors manually placed on farthest crossing points
- The configuration column describes the ordering of components in the path from signal source to measurement instrumentation. Data in columns labeled as “+buffer” include buffer and other columns DO NOT.
- “Cable only” measurements included for reference only
- Raw output of 100ps reference PHY was measured at 14ps of data dependent jitter.


Cable/Short Backplane Evaluation - Jitter due to ISI at 3Gb with Lonebit Pattern (in ps)
6" of .006 host > cable > 8" of .006 backplane
6" of .006 host > cable > 8" of .013 backplane
6" of .006 host > cable > 4" of .022 backplane
3" of .006 host > cable > 8" of .022 backplane
3" of .006 host > cable > 4" of .006 backplane
3" of .006 host > cable > 4" of .013 backplane
3" of .006 host > cable > 4" of .022 backplane
1m cable (Vert pcb connectors)
1m cable (RA pcb connectors)
0
5
10
15
20
25
30
35
40
45
50
100psPhy/tds
D3186/TDS
D3186/CSA


Cable/Short Backplane Evaluation - Jitter due to ISI at 1.5Gb with Lonebit Pattern (in ps)
6" of .006 host > cable > 8" of .006 backplane
6" of .006 host > cable > 8" of .013 backplane
6" of .006 host > cable > 4" of .022 backplane
3" of .006 host > cable > 8" of .022 backplane
3" of .006 host > cable > 4" of .006 backplane
3" of .006 host > cable > 4" of .013 backplane
3" of .006 host > cable > 4" of .022 backplane
1m cable (Vert pcb connectors)
1m cable (RA pcb connectors)
0
10
20
30
40
50
D3186/TDS
D3186/CSA


Internal 4x Solution Loss (includes backplane & host trace)
1.000
-1.000
-3.000
-5.000
-7.000
-9.000
-11.000
-13.000
-15.000
db
0
500
1000
1500
2000
2500
3000
3500
4000
MHz
03mRefDes
1mRefDes
TCTF

Conclusions

- SATA amplitude margins at 3Gb insufficient to support a 1m cable + worst case backplane trace + additional connector interface
- Design meets SAS-to-SAS and Gen1SATA-to-Expander margins
- Lower loss than TCTF at 1.5GHz and 3GHz
- TCTF comparison may justify modification of design criteria of loss model