Concerns with Mathematical Modeling of CIC

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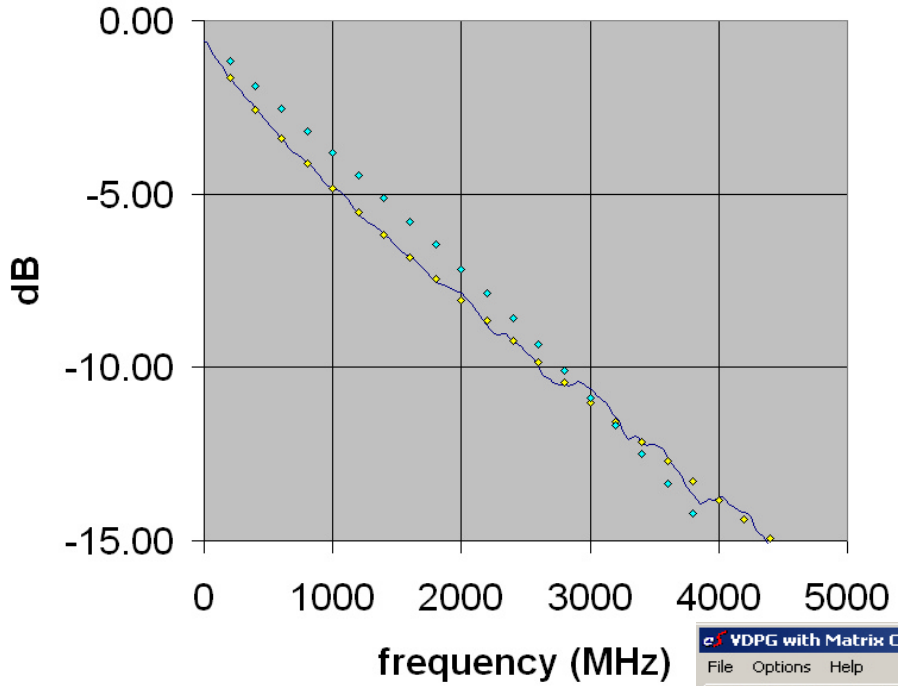
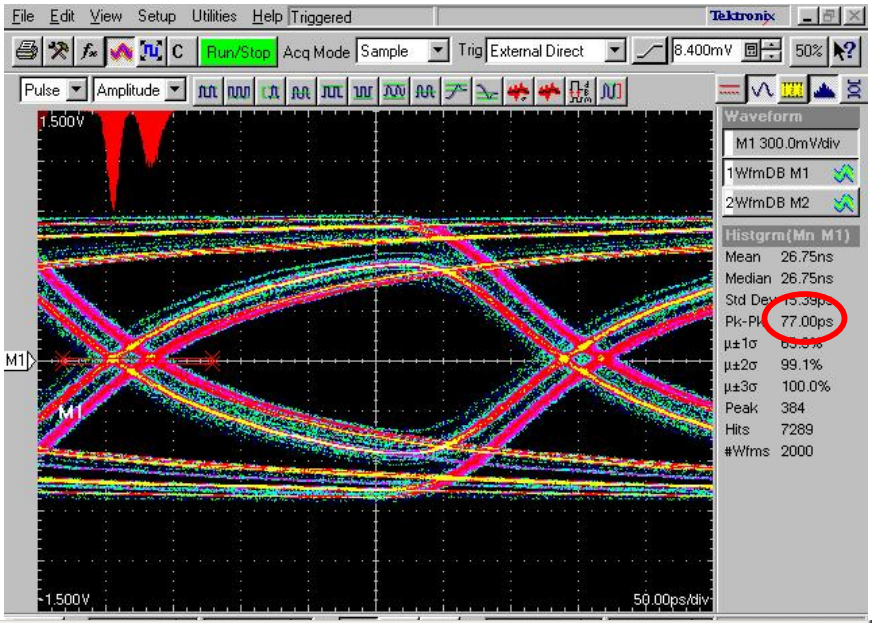
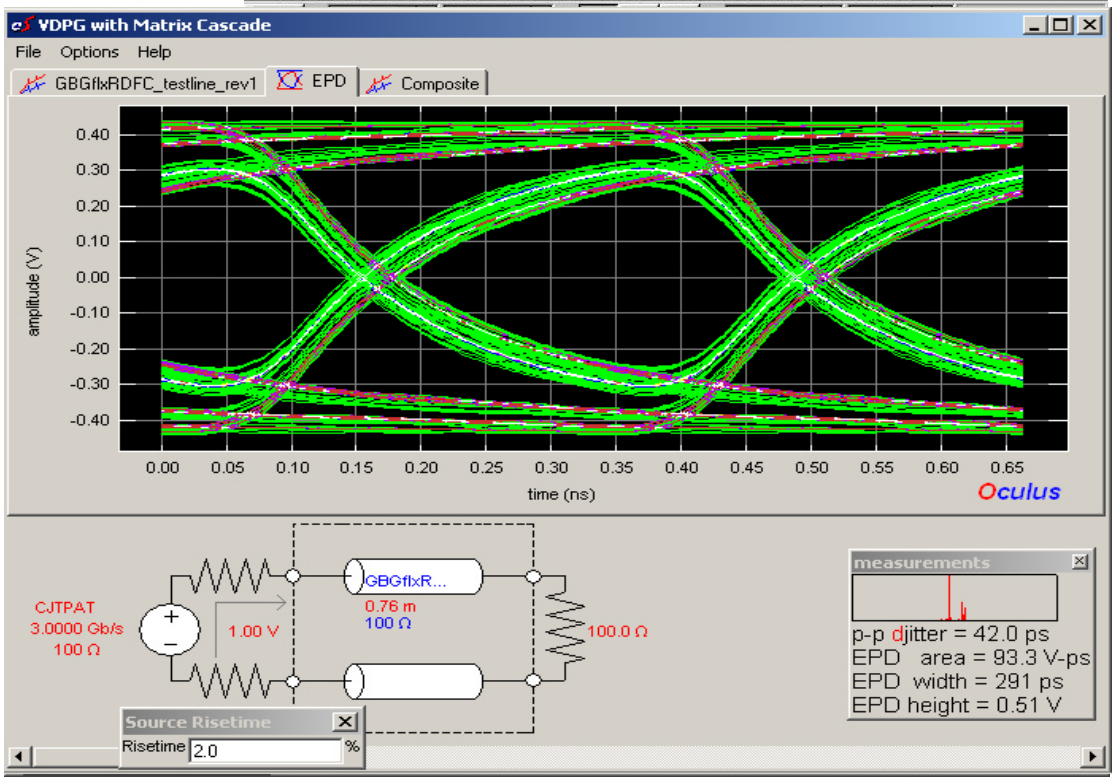
LSI Logic



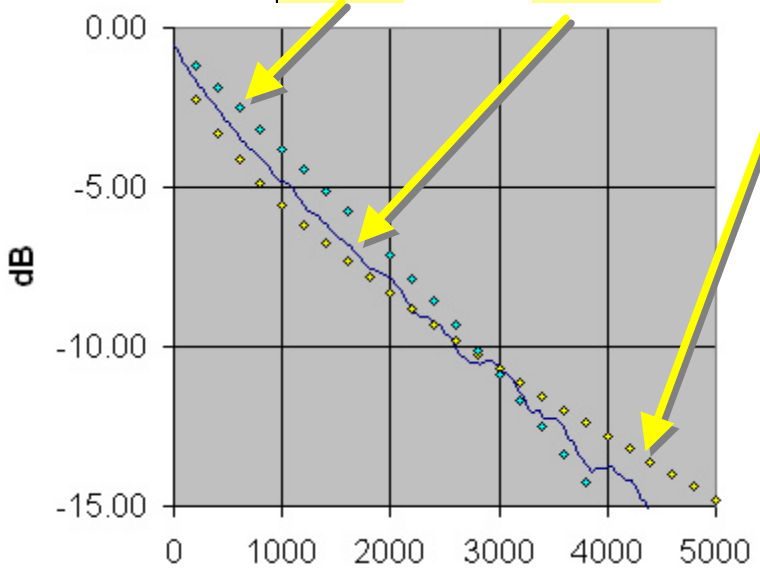


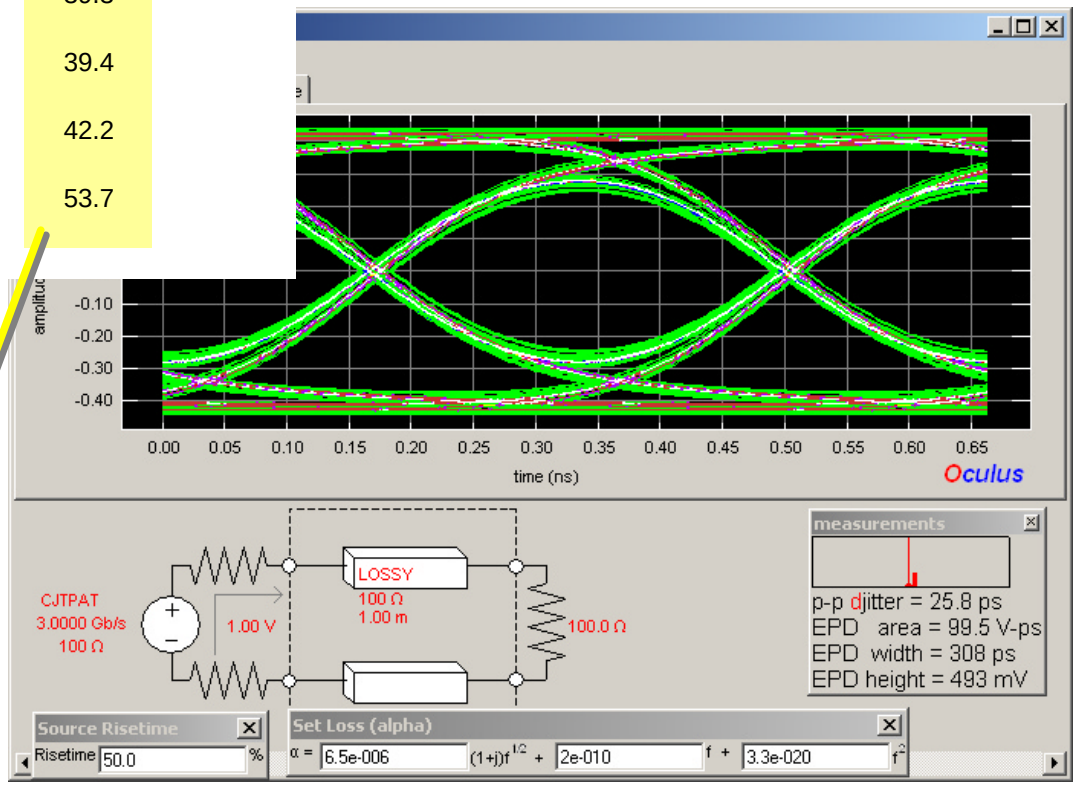
Hardware vs. Math CIC Data Eye



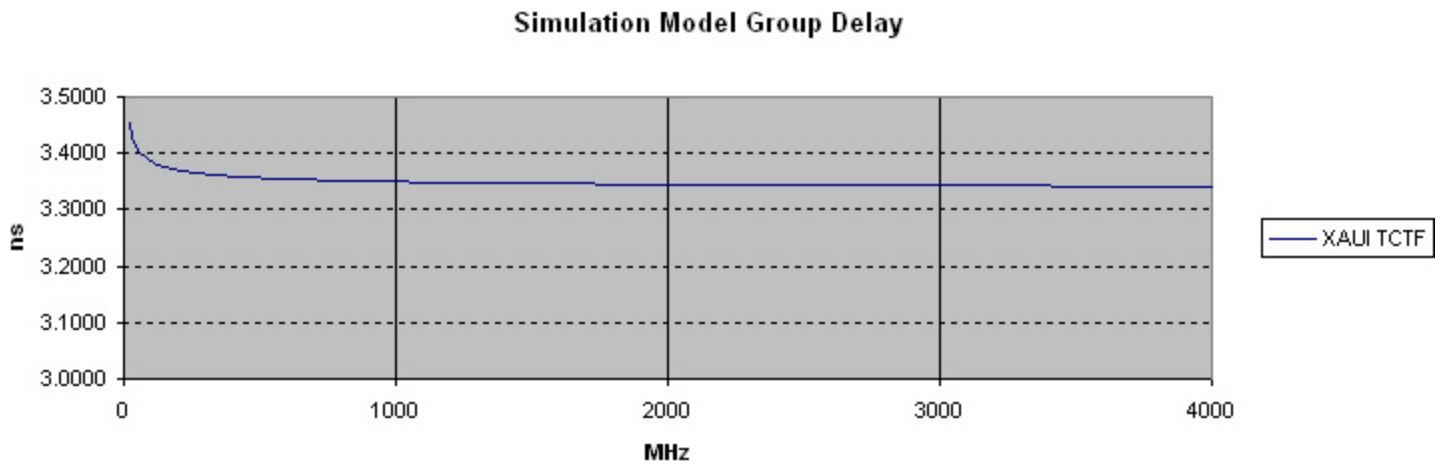
CIC Output Jitter vs. Loss Characteristic & Input T_{rise}

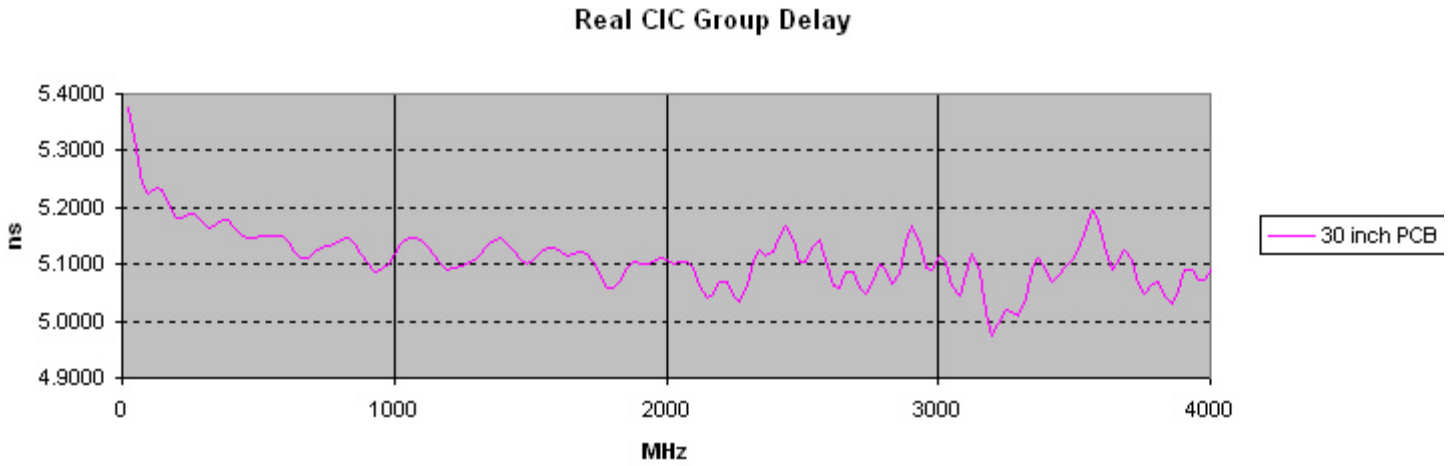
a1:	6.50E-06	1.00E-05	1.70E-05
a2:	2.00E-10	2.40E-10	1.00E-10
a3:	3.30E-20	0	0
rise time (%)			
2	17.8	25.0	39.3
10	18.2	25.6	39.4
25	20.2	29.2	42.2
50	25.8	38.6	53.7





Real vs Mathematical Model Group Delay





Conclusions

- Output jitter of mathematical CIC significantly less than hardware CIC
  - First observed by Eric Kvamme, Maxtor
  - No known explanation for this phenomenon
- Math & hardware CICs have similar attenuation, phase & group delay curves
- Output jitter strong function of input rise time and actual loss-vs-freq curve
- **Propose that math CIC option be removed from SAS PHY spec**