Proposed Draft

Serial ATA II Workgroup

Revision 1.0RC
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Serial ATA II Specification
Port Selector

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0.11	September 26, 2002	Clarified BIST support, out-of-band selection, COMINIT is only propagated and not generated by SFX, etc. ADH
0.12	October 4, 2002	Fixed some minor language. ADH
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0.14	October 31, 2002	Incorporated summit feedback. ADH
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0.16	November 28, 2002	Added overview, example applications, and power-on reset material. ADH
0.50	December 3, 2002	Moved revision to 0.5 as requested by group, accepted red-lined changes. ADH
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0.52	December 21, 2002	Highlighted wakeup budget impact out of partial/slumber, added section on orderly switch, added state machine for protocol-based port selection. ADH
0.53	January 6, 2003	Added protocol-based port selection state machine. ADH
0.70	January 13, 2003	Updated revision level for summit version of spec. ADH
0.71	January 30, 2003	Changes from summit and new marketing name. ADH
0.72	February 6, 2003	Instead of power “states” used power “conditions”. Changed reset terminology in some sections to “initialized”. ADH
0.73	February 26, 2003	When no active host port, new active host port is selected when any OOB signal is received over a host port. ADH
0.74	March 3, 2003	Updated “OOB signal” from last revision to “COMRESET or COMWAKE”. ADH
0.75	March 10, 2003	Summit version of the spec. ADH
0.76	March 20, 2003	Updates based on summit feedback. Phy control state machine included. ADH
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0.85	April 21, 2003	Summit version of the spec. ADH
0.86	May 7, 2003	Updates from summit, including informative section on preferred method to create protocol-based sequence with software. ADH
0.87	May 13, 2003	Incorporated presence detection. ADH
0.90	May 19, 2003	Group voted to move the specification to 0.9. ADH
0.91	June 12, 2003	Modified state machine for speed negotiation. ADH
0.92	June 19, 2003	Summit updates. ADH
0.92b	June 19, 2003	Included COMWAKE transmit timing exemption. ADH
1.0RC	June 23, 2003	Focus group voted to accept 0.92b as the 1.0RC. ADH

Table of Contents

1. Introduction

Port Selector is a mechanism that allows two different host ports to connect to the same device in order to create a redundant path to that device. In combination with RAID, the Port Selector allows system providers to build fully redundant solutions. The upstream ports of a Port Selector can also be attached to a Port Multiplier or a Serial ATA Switch to provide redundancy in a more complex topology. A Port Selector can be thought of as a simple multiplexer as shown in Figure 1.

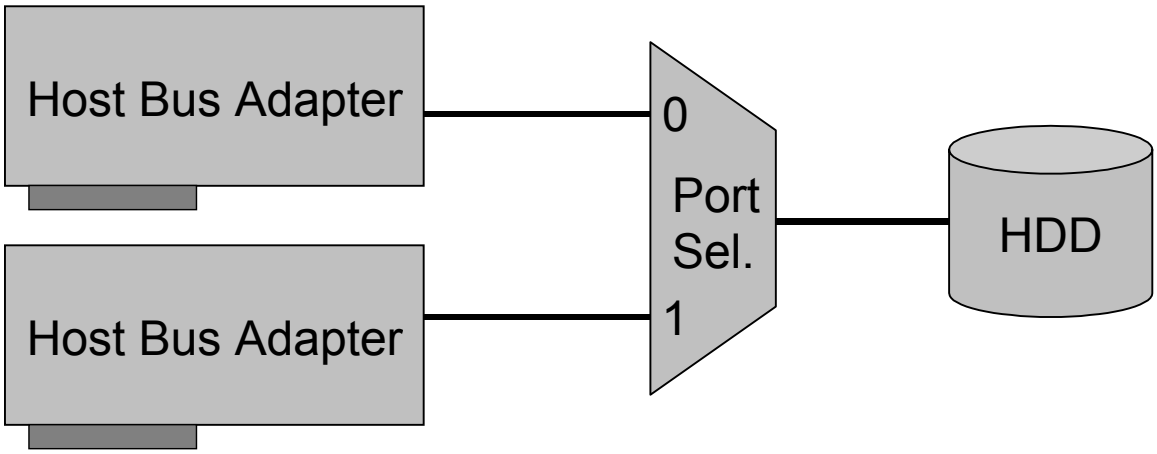

Figure 1 Port Selector Overview

1.1. Goals, Objectives, & Constraints

This specification defines an ingredient, Port Selector, that creates redundant paths to a device. The Port Selector allows system providers to build fully redundant solutions in combination with RAID.

Some of the goals and requirements for the Port Selector definition include:

- Serial ATA 1.0a devices may be attached without modification
- Serial ATA 1.0a host bus adapters may be attached with only software modifications
- Transport, Link, and Phy layer compatibility with Serial ATA 1.0a must be maintained for both hosts and devices
- No new primitives may be added as part of the definition
- No new FIS types may be added as part of the definition
- A Port Selector should not require a full Link layer or Transport layer

Some of the constraints include:

- Only two host connections are provided by the Port Selector
- Only one of the two host ports is active at a time (no active/active)
- Cascading Port Selectors is not supported

1.2. Example Applications

One example application of a Port Selector, as shown in Figure 2, is to provide a means for redundant access to a device. This ingredient, along with RAID, allows a system with no single point of failure to be built. Typically the Port Selector would be packaged in the hard drive carrier to create a single serviceable unit in case the hard drive failed. The total system would consist of two hosts each connected to a RAID array where each drive in the system had a Port Selector

attached that was connected to each host. One host could be considered the live host and the other host may be the spare. In this configuration, the live host would maintain access to all of the devices and the spare host would only take over access to the devices if the live host had a failure.

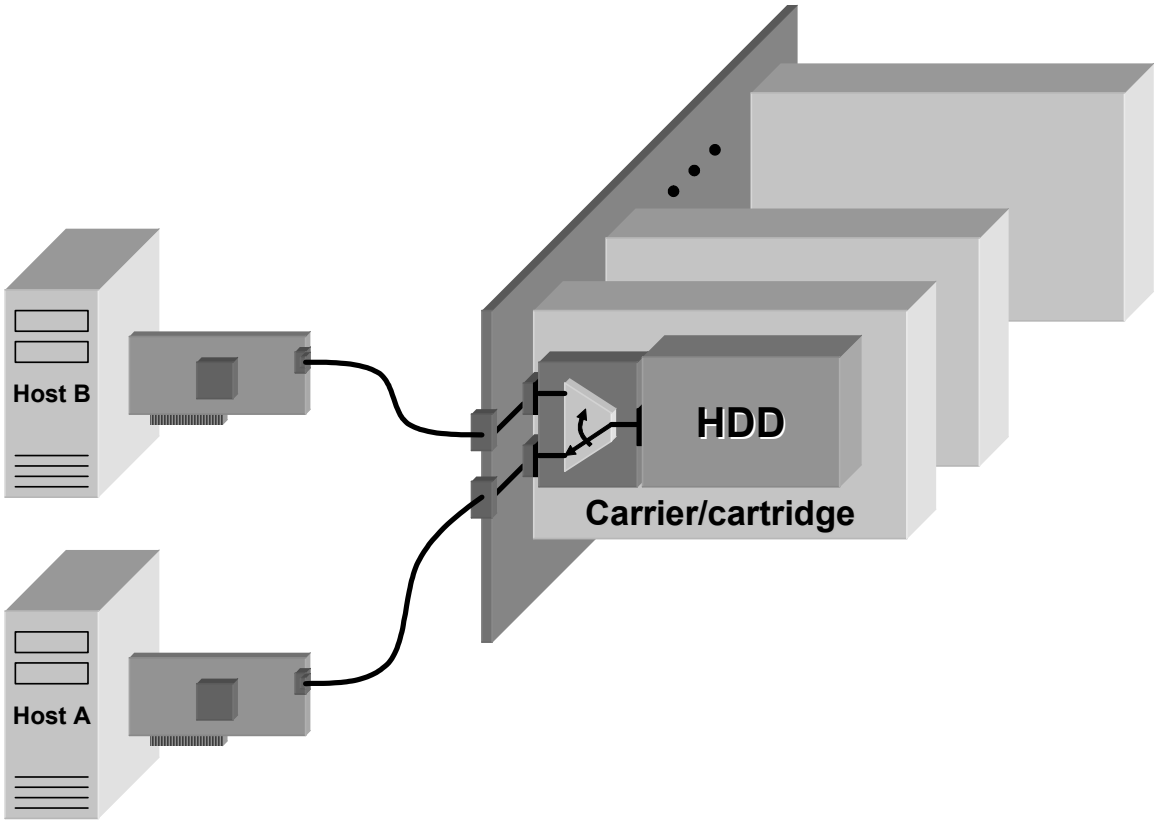

Figure 2 Example Failover Application with Two Hosts

1.3. Definitions, abbreviations, and conventions

1.3.1. Definitions and Abbreviations

The terminology used in this specification is consistent with the terminology used in the Serial ATA 1.0a and Serial ATA II specifications, and all definitions and abbreviations defined in those specifications are used consistently in this document. Additional terms and abbreviations introduced in this specification are defined in the following sections.

1.3.1.1. Active port

The active port is the currently selected host port on the Port Selector.

1.3.1.2. Device port

The device port is the port on the Port Selector that is connected to the device.

1.3.1.3. Host port

The host port is a port on the Port Selector that is connected to a host. There are two host ports on a Port Selector.

1.3.1.4. Inactive port

The inactive port is the host port that is not currently selected on the Port Selector.

1.3.1.5. Protocol-based port selection

Protocol-based port selection is a method that may be used by a host to select the host port that is active. Protocol-based port selection uses a sequence of Serial ATA out-of-band Phy signals to select the active host port.

1.3.1.6. Quiescent power condition

Entering a quiescent power condition for a particular Phy is defined as the Phy entering the idle bus condition as defined in section 6.7.5 of the Serial ATA 1.0a specification.

1.3.1.7. Side-band port selection

Side-band port selection is a method that may be used by a host to select the host port that is active. Side-band port selection uses a mechanism that is outside of the Serial ATA protocol for determining which host port is active. The port selection mechanism used in implementations that support side-band port selection is outside the scope of this specification.

1.4. References

This specification is an extension to the Serial ATA 1.0a specification. The Serial ATA 1.0a specification is presumed as the underlying baseline for this specification. This specification makes reference to the following specifications:

Serial ATA: High Speed Serialized AT Attachment revision 1.0a.

Serial ATA II Specification: Extensions to Serial ATA 1.0.

The specifications are available for download at www.serialata.org.

2. Overview

Port Selector is a mechanism that allows two different host ports to connect to the same device in order to create a redundant path to that device. Only one host connection to the device is active at a time. Effective use of a Port Selector requires coordinated access to the device between the two host ports. The host(s) must coordinate to determine which host port should be in control of the device at any given point in time. Definition of the coordination mechanism or protocol is beyond the scope of this specification.

Once the host(s) determines the host port that should be in control of the device, the host that contains the host port to be made active will take control of the device by selecting that host port to be active. The active host selects a port to be active by using either a protocol-based or side-band port selection mechanism. A side-band port selection mechanism can be as simple as a hardware select line that is pulled high to activate one host port and low to activate the other. The side-band port selection mechanism is outside the scope of this specification. A protocol-based port selection mechanism uses the Serial ATA protocol to cause a switch of active port. This specification defines a protocol-based port selection mechanism that uses a particular Morse coding of COMRESET signals to cause a switch of active host port. A Port Selector shall only support one selection mechanism at any point in time. The externally visible behavior of a Port Selector is the same regardless of whether a protocol-based or side-band port selection mechanism is used.

A Port Selector that supports protocol-based port selection can be detected in the signal path if the optional presence detection feature is supported by the Port Selector and the host has an enhanced SError register that can latch this event. The detection mechanism for a Port Selector that supports side-band port selection is outside the scope of this specification.

3. Active Port Selection

The Port Selector has a single active host port at a time. The Port Selector shall support one of two mechanisms for determining which of the two host ports is active. The first mechanism is called side-band port selection. Side-band port selection uses a mechanism outside of the Serial ATA protocol for determining which host port is active. The second mechanism is called protocol-based port selection. Protocol-based port selection uses a sequence of Serial ATA out-of-band Phy signals to select the active host port.

Whether a protocol-based or side-band port selection mechanism is used, the Port Selector shall exhibit the behavior defined within this specification.

After selection of a new active port, the device and is in an unknown state. The device may have active commands outstanding from the previous active host that need to be flushed. After an active port switch has been performed it is strongly suggested that the active host issue a COMRESET to the device to ensure that the device is in a known state.

3.1. Protocol-based Port Selection

Protocol-based port selection is an active port selection mechanism that uses a sequence of Serial ATA out-of-band Phy signals to select the active host port. A Port Selector that supports protocol-based port selection shall have no active host port selected upon power-up. The first COMRESET or COMWAKE received over a host port shall select that host port as active. The host may then issue explicit switch signals to change the active host port.

Reception of the protocol-based port selection signal on the inactive host port causes the Port Selector to deselect the currently active host port and select the host port over which the selection signal is received. The protocol-based port selection signal is defined such that it can be generated using the Serial ATA 1.0a superset Status and Control registers and such that it can be received and decoded without the need for the Port Selector to include a full Link or Transport layer (i.e. direct Phy detection of the signal).

3.1.1. Port Selection Signal Definition

The port selection signal is based on a pattern of COMRESET out-of-band signals transmitted from the host to the Port Selector. As illustrated in Figure 3, the Port Selector shall qualify only the timing from the assertion of a COMRESET signal to the assertion of the next COMRESET signal in detecting the port selection signal.

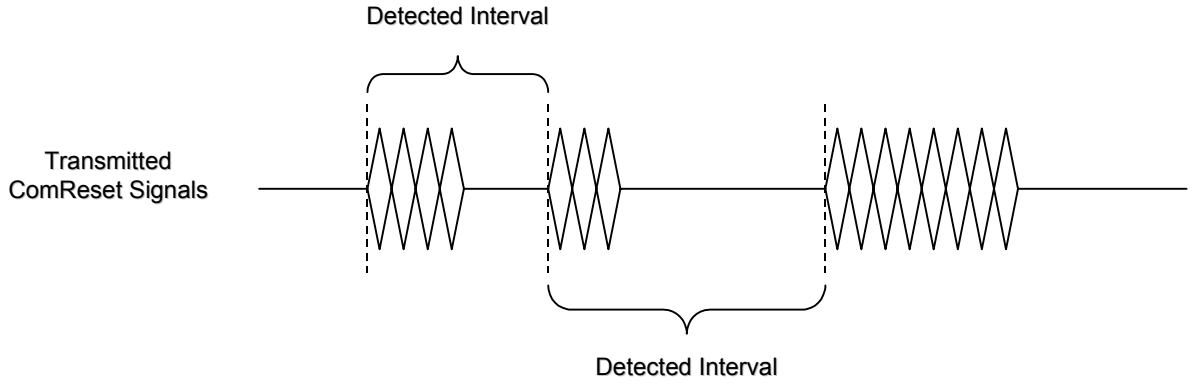

Figure 3 Port selection signal based on assertion of COMRESET to assertion of following COMRESET

The port selection signal is defined as a series of COMRESET signals with the timing from the assertion of one COMRESET signal to the assertion of the next as defined in Table 1 and illustrated in Figure 4. The Port Selector shall select the port, if inactive, on the de-assertion of COMRESET after receiving two complete back-to-back sequences with specified inter-burst spacing over that port (i.e. two sequences of two COMRESET intervals comprising a total of five COMRESET bursts with four inter-burst delays). Specifically, after receiving a valid port selection signal, the Port Selector shall not select that port to be active until the entire fifth COMRESET burst has been de-asserted. The Port Selector is only required to recognize the port selection signal over an inactive port. Reception of COMRESET signals over an active port is propagated to the device without any action taken by the Port Selector, even if the COMRESET signals constitute a port selection signal. This may result in multiple device resets.

The timings detailed in Table 1 shall be independent of the signaling speed used on the link. For example, the inter-reset timings are the same for links using Gen1 or Gen2 speeds.

	Nom	Min	Max	Units	Comments
T1	2.0	1.6	2.4	ms	Inter-reset assertion delay for first event of the selection sequence
T2	8.0	7.6	8.4	ms	Inter-reset assertion delay for the second event of the selection sequence

Table 1 Port selection signal inter-reset timing requirements

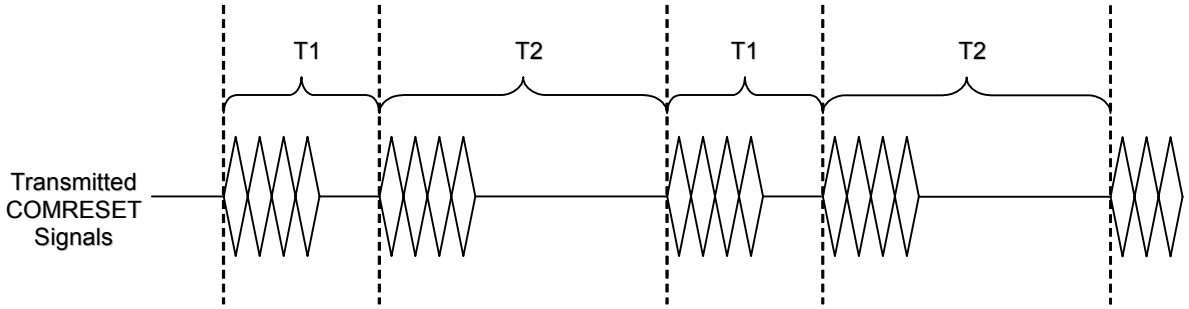

Figure 4 Complete port selection signal consisting of two sequences with requisite inter-reset spacings

The interpretation and detection of the COMRESET signal by the Port Selector is in accordance with the Serial ATA 1.0a definition, i.e. the COMRESET signal is detected upon receipt of the fourth burst that complies with the COMRESET signal timing definition. The inter-reset timings referred to here for the port selection signal are from the detection of a valid COMRESET signal to the next detection of such a signal, and are not related to the bursts that comprise the COMRESET signal itself.

3.1.2. Presence Detection

Presence detection is the ability for a host to detect that a Port Selector is present on a port. If a Port Selector supports presence detection capabilities, a host will be able to determine whether a Port Selector is connected to a host port. The host may determine this regardless of whether the Port Selector port to which it is connected is the active or inactive link.

Presence detection capabilities are defined for Port Selectors utilizing protocol-based port selection only. Systems utilizing side-band port selection must be preconfigured for side-band port selection and therefore those systems can also be preconfigured to support presence detection. Presence detection is an optional feature of protocol-based Port Selectors.

3.1.2.1. Host port Phy state machine enhancements

If presence detection is supported, the Port Selector host port Phy state machine as described in the Serial ATA 1.0a specification shall be modified as shown. A Port Selector shall remain in the DR_PS_Wait state when the Phy is offline and presence detection is enabled.

DP1: DR_Reset[1]	Interface quiescent	
1. COMRESET not detected and power-on reset deasserted ***and presence detection not enabled and Phy not offline***	→	DR_COMINIT
2. COMRESET not detected and power-on reset deasserted and presence detection enabled	→	***DR_PS_Presence***
3. COMRESET detected or power-on reset asserted	→	DR_Reset
NOTE : 1. This state is entered asynchronously any time in response to power-on reset or receipt of a COMRESET signal from the host		

DP12: DR_PS_Presence	***Transmit COMWAKE[1]***	
1. Phy online	→	***DR_COMINIT***
2. Phy offline	→	***DR_PS_Wait***
NOTE: ***1. The COMWAKE signal transmitted need not comply with the "COMWAKE Transmit Spacing" specification of Serial ATA 1.0a but must comply with the "COMWAKE Detector On Threshold" specification of Serial ATA 1.0a.***		

DP13: DR_PS_Wait	***Interface quiescent***	
1. Phy online	→	***DR_COMINIT***
2. Phy offline	→	***DR_PS_Wait***

3.1.2.2. Host Phy state machine impact (Informative)

A host connected to a Port Selector performing presence detection will receive a COMWAKE signal while in the HP2: HR_AwaitCOMINIT state of the Serial ATA 1.0a Phy state machine. This state, as shown in Figure 5, is insensitive to receiving a COMWAKE and only performs a transition to a new state when COMINIT is received. Host designers must ensure that their implementations are insensitive to receiving a COMWAKE in this state. If the host design is capable of latching the event of receiving a COMWAKE while in this state, the host should expose that event using the SError register enhancement detailed in section 3.1.2.3.

HP2: HR_AwaitCOMINIT	Interface quiescent		
1. COMINIT detected from device		→	HR_AwaitNoCOMINIT
2. COMINIT not detected from device		→	HR_AwaitCOMINIT

Figure 5 HR_AwaitCOMINIT from Serial ATA 1.0a Phy state machine

3.1.2.3. SError Register Enhancement for Presence Detection

The Serial ATA interface error register (SError) as defined in the Serial ATA 1.0a specification and Serial ATA II: Extensions to Serial ATA 1.0 specification includes indications for various events that may have occurred on the interface such as a change in the PhyRdy state, detection of disparity, errors, and so on.

In order to facilitate a means for notifying host software that a Port Selector presence detection signal was received, an additional bit in the DIAG field of the SError superset register is defined as indicated in Figure 6.

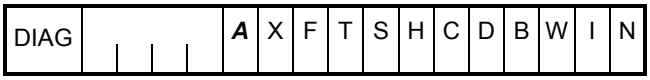

Figure 6 Location of A bit in DIAG field

N	As defined in Serial ATA 1.0a
I	As defined in Serial ATA 1.0a
W	As defined in Serial ATA 1.0a
B	As defined in Serial ATA 1.0a
D	As defined in Serial ATA 1.0a
C	As defined in Serial ATA 1.0a
H	As defined in Serial ATA 1.0a
S	As defined in Serial ATA 1.0a
T	As defined in Serial ATA 1.0a
F	As defined in Serial ATA 1.0a
X	As defined in Serial ATA II: Extensions to Serial ATA 1.0
A	Port Selector presence detected: This bit is set to one when COMWAKE is received while the host is in state HP2: HR_AwaitCOMINIT. On power-up reset this bit is cleared to 0. The bit is cleared to 0 when the host writes a '1' to this bit location.

3.1.3. Host Transmission Considerations (Informative)

In order to ensure the port selection signal is reliably conveyed to the Port Selector, the host should account for any other interface activity that may interfere with the transmitted COMRESET port selection sequence. For example, if the host periodically issues a COMRESET signal as part of a hardware-polled device presence detection mechanism, a periodic COMRESET signal could occur during the port selection signaling sequence, thereby corrupting the port selection sequence. In order to avoid such interactions, the host may elect to continually transmit the port selection sequence while monitoring the Phy status in the associated superset Status and Control register. When the port selection signal is recognized by the Port Selector and has taken effect,

the host can detect a change in the PhyRdy status since the associated port will be activated and communications with it will be established. It is recommended that the host check the PhyRdy signal immediately before issuing each COMRESET burst in the protocol-based selection signal and only issue the next COMRESET burst if PhyRdy is not present.

3.2. Side-band Port Selection

The active host port may be selected by a side-band mechanism. Side-band port selection uses a mechanism outside of the Serial ATA protocol for selecting which host port is active. One example of a side-band port selection mechanism is a hardware select line. The side-band selection mechanism used is outside the scope of this specification. A Port Selector that supports side-band port selection shall exhibit the behavior defined within this specification.

3.3. Behavior during a change of active port

During a change of active port, the previous host connection is broken and all internal state other than the active host port is initialized before the connection with the new active host is made. When a new active host port is selected, the Port Selector shall perform the following procedure:

1. The Port Selector shall stop transmitting and enter the quiescent power condition on the previously active host port Phy (now the inactive host port).
2. The Port Selector shall initialize all internal state other than the state of the selection bit for the active host port.
3. The Port Selector shall enter the active power condition on the new active host port.
4. The Port Selector shall allow out-of-band and in-band traffic to proceed between the new active host port and the device.

3.3.1. Device State after a change of active port (Informative)

A Port Selector may support an orderly switch to a new active host port. A Port Selector that supports an orderly switch ensures that primitive alignment with the device Phy is maintained during the switch to the new active host port. Maintaining primitive alignment ensures that PhyRdy remains present between the Port Selector and the device throughout the switch to the new active host port.

After selection of a new active port, the device may be in an unknown state. The device may have active commands outstanding from the previously active host port that need to be flushed. The new active host can issue a COMRESET to the device in order to return the device to a known state.

4. Behavior and Policies

4.1. Control State Machine

The Port Selector Control state machine is based on a model of a Port Selector consisting of three Serial ATA Phys interconnected and controlled by an overall control logic block as depicted in
Figure 7. For convenience, the three ports of a Port Selector are abbreviated “A,” “B,” and “D” corresponding to Host Port A, Host Port B, and Device Port respectively.

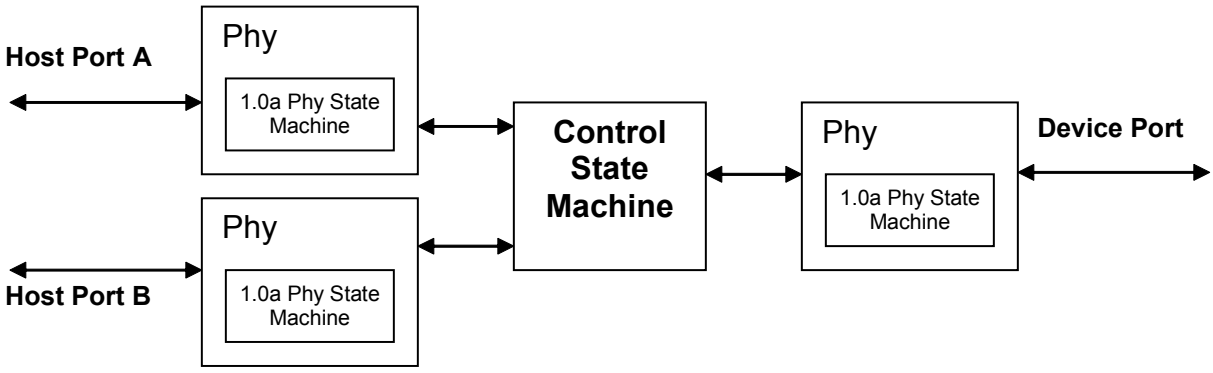

Figure 7 Control State Machine

The Phys depicted in Figure 7 are presumed to have the basic capabilities and controls indicated in Figure 8. Figure 8 is a variant of Figure 18 in the Serial ATA 1.0a specification. The changes to the original Serial ATA 1.0a figure are:

- Loopback controls were removed since those controls were not relevant in this state machine.
- Explicit ONLINE and OFFLINE signals were added, including a register latch for these signals so that the signals do not need to be asserted in every state. The Serial ATA 1.0a specification specifies a mechanism for the host to put the Phy in offline mode using the SControl register. Therefore, it is reasonable to expect that the Phy has signals ONLINE and OFFLINE that can be utilized.
- A PORTSELECT signal was added. A Port Selector using protocol-based port selection shall set the PORTSELECT signal to the output of the Sequence Detect block. The Sequence Detect block is asserted when the protocol-based selection signal is received, otherwise the signal is de-asserted. A Port Selector using side-band port selection shall set the PORTSELECT signal when a change in active port is requested.

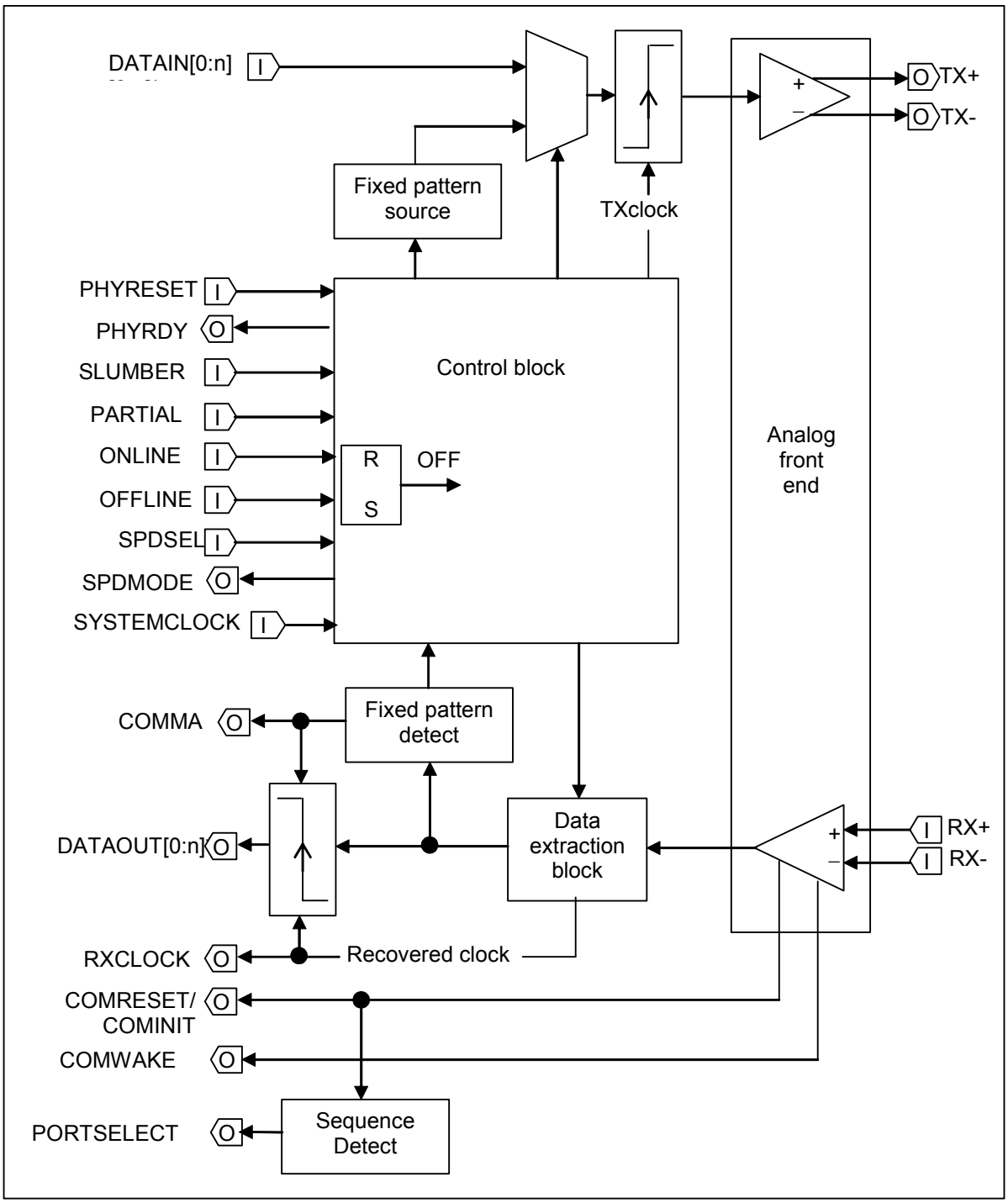

Figure 8 Phy Block Diagram

The following state diagram specifies the behavior of the Port Selector control logic block. The Port Selector shall have the externally visible behavior described by this state machine.

Reception of a COMRESET signal from the selected host port shall unconditionally force the control state machine to transition to state PS15: ResetDevice. Reception of a COMINIT signal

from the device shall unconditionally force the control state machine to transition to state PS14: ResetHost if not in the ResetDevice state. For the sake of brevity, this implied transition has been omitted from most states.

PS1: PORReset[1]	Set internal PS state to initial conditions including MaxNegSpeed=Max and SelHostPort=none. Assert A.OFFLINE. Assert B.OFFLINE. Assert D.OFFLINE.	
1. Power-on reset and explicit reset request deasserted and Mode = SideBand	→	SetHostPortSideBand
2. Power-on reset and explicit reset request deasserted and Mode = ProtocolBased	→	AwaitHostSelection
3. Power-on reset or explicit reset request asserted	→	PORReset
NOTE : 1. This state is entered asynchronously any time in response to power-on reset or an explicit reset request. An explicit reset request is a reset line/button on the Port Selector itself, not a COMRESET signal from a host.		

PS2: SetHostPortSideBand	Set SelHostPort based on value of side-band selection signal.	
1. COMRESET received from SelHostPort		ResetDevice
2. COMINIT received from D and COMRESET not received from SelHostPort		ResetHost
3. COMRESET not received from SelHostPort and COMINIT not received from D	→	SetHostPortSideBand

PS3: ComInitPropToBoth	Assert A.ONLINE. Assert A.PHYRESET. Assert B.ONLINE. Assert B.PHYRESET.	
1. Unconditional	→	AwaitHostSelection

PS4: AwaitHostSelection		
1. COMINIT received from D and (COMRESET or COMWAKE) not received from (A or B)	→	ComInitPropToBoth
2. (COMRESET or COMWAKE) received from A	→	SelectA
3. (COMRESET or COMWAKE) not received from A and (COMRESET or COMWAKE) received from B	→	SelectB
4. No OOB signal detected	→	AwaitHostSelection

PS5: SelectA	Assert B.OFFLINE. Set SelHostPort=A. Assert SelHostPort.ONLINE. Assert D.ONLINE. Assert SelHostPort.PHYRESET. Assert D.PHYRESET.	
1. Unconditional	→	WaitforComm

PS6: SelectB	Assert A.OFFLINE. Set SelHostPort=B. Assert SelHostPort.ONLINE. Assert D.ONLINE. Assert SelHostPort.PHYRESET. Assert D.PHYRESET.	
1. Unconditional	→	WaitforComm

PS7: WaitForComm		
1. SelHostPort.PHYRDY and D.PHYRDY and no change in PORTSELECT signal	→	CheckSpeeds
2. (!SelHostPort.PHYRDY or !D.PHYRDY) and timeout[1] not exceeded and no change in PORTSELECT signal	→	WaitForComm
3. (!SelHostPort.PHYRDY or !D.PHYRDY) and timeout[1] exceeded and no change in PORTSELECT signal	→	PowerManageCheck
4. PORTSELECT signal received for non-selected host port	→	ChangePort
NOTE: 1. The timeout is vendor specific but shall be larger than 1760 microseconds.		

PS8: CheckSpeeds[1]		
1. SelHostPort.SPDMODE = D.SPDMODE	→	Online
2. SelHostPort.SPDMODE > D.SPDMODE	→	SetDeviceSpeed
3. SelHostPort.SPDMODE < D.SPDMODE	→	SetHostSpeed
NOTE: 1. A larger value for the SPDMODE signal shall indicate a higher speed than a smaller value for SPDMODE.		

PS9: Online	Transfer DATA received on D to SelHostPort. Transfer DATA received on SelHostPort to D.	
1. PORTSELECT signal received for non-selected host port	→	ChangePort
2. SelHostPort.PHYRDY deasserted or D.PHYRDY deasserted	→	PowerManageCheck

PS10: SetDeviceSpeed	Set MaxNegSpeed=D.SPDMODE	
1. Unconditional	→	ReComm

PS11: SetHostSpeed	Set MaxNegSpeed=SelHostPort.SPDMODE	
1. Unconditional	→	ReComm

PS12: ReComm	Assert D.PHYRESET	
1. Unconditional	→	WaitForComm

PS13: ChangePort	Assert SelHostPort.OFFLINE. Assert !SelHostPort.ONLINE. Set SelHostPort=!SelHostPort. Set MaxNegSpeed=Max.	
1. Unconditional	→	WaitForComm

PS14: ResetHost	Assert SelHostPort.ONLINE. Assert D.ONLINE. Assert SelHostPort.PHYRESET	
1. Unconditional	→	WaitForComm
NOTE: 1. This state is entered unconditionally upon receipt of D.COMINIT if SelHostPort != none and the Port Selector is not in state ResetDevice.		

PS15: ResetDevice[1]	Assert SelHostPort.ONLINE. Assert D.ONLINE. Assert D.PHYRESET.		
1. Unconditional		→	WaitForComm
NOTE: 1. This state is entered unconditionally upon receipt of SelHostPort.COMRESET if SelHostPort != none.			

PS16: PowerManageCheck			
1. Port Selector determined that low power state entered is SLUMBER		→	PowerManageSlumber
2. Port Selector has not determined that low power state entered is SLUMBER		→	PowerManagePartial

PS17: PowerManagePartial	Assert SelHostPort.Partial. Assert D.Partial.		
1. SelHostPort.COMWAKE detected or D.COMWAKE detected		→	WaitForComm
2. PORTSELECT signal received for non-active host port		→	ChangePort
3. COMWAKE not received and no change in PORTSELECT signal		→	PowerManagePartial

PS18: PowerManageSlumber	Assert SelHostPort.Slumber. Assert D.Slumber.		
1. SelHostPort.COMWAKE detected or D.COMWAKE detected		→	WaitForComm
2. PORTSELECT signal received for non-active host port		→	ChangePort
3. COMWAKE not received and no change in PORTSELECT signal		→	PowerManageSlumber

4.2. BIST support

A Port Selector is not required to support the BIST Activate FIS. The resultant behavior of sending a BIST Activate FIS through a Port Selector is undefined.

4.3. Flow control signaling latency

The Port Selector must satisfy the flow control signaling latency specified in section 7.4.7 of the Serial ATA 1.0a specification. The Port Selector shall ensure that the flow control signaling latency is met on a per link basis. Specifically, the Port Selector shall ensure that the flow control signaling latency is met between:

1. The Port Selector active host port and the host it is connected to
2. The Port Selector device port and the device it is connected to

The Port Selector shall not reduce the flow control signaling latency budget of the active host it is connected to or the device it is connected to.

4.4. Power Management

The Port Selector must maintain the active host port across power management events and only allow an active host port change after receiving a valid port selection signal.

The Phy on the inactive host port shall be in the quiescent power condition. Upon detecting that the PhyRdy signal is not present for the active host port or device port, the Port Selector shall place that Phy in a quiescent power condition.

If the PhyRdy signal is not present between the device and the Port Selector, the Phy connected to the active host port shall enter the quiescent power condition and squelch the Phy transmitter. If the PhyRdy signal is not present between the active host and the Port Selector, the Phy connected to the device shall enter the quiescent power condition and squelch the Phy transmitter. During these periods while PhyRdy is not present, OOB signals shall still be propagated between the active host and the device to ensure that communication can be established.

If the Port Selector is able to determine that the active host and device negotiated a SLUMBER power management transition, the Port Selector may recover from the quiescent power condition in the time defined by the SLUMBER power state. If the Port Selector is not able to determine the power state entered by the host and device, the Port Selector shall recover from the quiescent power condition in the time defined by the PARTIAL power state.

4.4.1. Wakeup Budget

The wakeup budget out of PARTIAL or SLUMBER may increase when a Port Selector is connected to a device. When the active host Phy comes out of low power condition, the Port Selector active host Phy may wakeup before causing the Port Selector device Phy to wakeup which in turn will wakeup the device. The host shall allow the device at least 20 microseconds to wakeup from the PARTIAL power management state.

4.5. Out of Band (OOB) Phy signals

The Port Selector shall propagate COMRESET received from the active host to the device as specified in the Control State Machine in section 4.1. The Port Selector shall propagate COMINIT received from the device to the active host port as specified in the Control State Machine in section 4.1. If no active host port is selected, the Port Selector shall propagate COMINIT received from the device to the active host port as specified in the Control State Machine in section 4.1. The Port Selector is allowed to delay delivery of propagated OOB signals.

The Port Selector shall not respond to COMRESET signals received over the inactive host port. The inactive host port Phy shall remain in the quiescent power condition when COMRESET is received over the inactive host port.

4.6. Hot Plug

The Port Selector shall only generate a COMINIT over a host port when a COMINIT signal is received from the device or as part of an active speed negotiation as specified in the Control State Machine in section 4.1. If a drive connected to a Port Selector is hot plugged, the drive will issue a COMINIT sequence as part of its normal power-up sequence in accordance with Serial ATA 1.0a. The Port Selector shall propagate the COMINIT over the active host port (or both host ports if both host ports are inactive). The host will see the COMINIT signal and then interrogate the port to determine whether a drive is attached.

If a drive connected to a Port Selector is hot unplugged, the Port Selector shall squelch the transmitter for the active host port as detailed in section 4.4. The active host will determine that the PhyRdy signal is no longer present and will determine that there is no longer a drive present.

4.7. Speed Negotiation

Speed is negotiated on a per link basis. Specifically, the Port Selector shall negotiate speed between:

1. The Port Selector active host port and the host to which it is connected
2. The Port Selector device port and the device to which it is connected

The Port Selector starts speed negotiation at the highest speed rate that it supports. The Port Selector then negotiates speed on each link to the appropriate supported speed. After negotiating speed on the active host link and on the device link, the Port Selector shall check whether the two speeds match. If the speeds do not match, the Port Selector limits the maximum speed rate it supports to the lower of the two speeds negotiated. Then the Port Selector forces speed to be renegotiated to reach a common speed rate.

4.8. Spread spectrum clocking

The Port Selector shall support spread spectrum clocking receive on all of its ports. The Port Selector may support spread spectrum transmit. It is recommended that a configuration jumper be used to enable/disable spread spectrum clocking if it is settable. There is no means within the Serial ATA protocol provided to enable/disable spread spectrum clocking if it is statically configurable.

If spread spectrum clocking is used, the spreading domain between the host and the Port Selector is not required to be the same as the spreading domain between device and the Port Selector. The signals passing through a Port Selector may be re-spread.

5. Power-up and Resets

5.1. Power-up

Upon power-up, the Port Selector shall reset all internal state, including the active host port. This will cause no active host port to be selected when protocol-based port selection is used.

5.1.1. Presence detection of Port Selector

For protocol-based port selection, presence detection can be performed using the optional mechanism outlined in section 3.1.2. Presence detection for Port Selectors implementing side-band port selection is outside the scope of this specification.

5.2. Resets

5.2.1. COMRESET

When COMRESET is received over the active host port the Port Selector shall reset all internal state, the active host port shall remain unchanged, the maximum speed shall remain unchanged, and the COMRESET signal shall be propagated to the device. The Port Selector shall take no reset action upon receiving a COMRESET signal over the inactive host port except as specified in section 3.1 when there is no active host port selected after power-up.

5.2.2. Software reset and DEVICE RESET

The Port Selector shall not reset in response to receiving a Software reset or the DEVICE RESET command.

APPENDIX A. HOST IMPLEMENTATION (INFORMATIVE)

A.1 Software Method for Protocol-based Selection (Informative)

The preferred software method for producing a protocol-based port selection signal is detailed in this section. Software for HBAs that implement the SControl and SStatus registers may use this method to create the protocol-based port selection signal.

If the Phy is left on for long periods during the generation of the sequence, a hardware based COMRESET polling algorithm may interfere and corrupt the sequence. This method tries to minimize any impact of host based COMRESET polling algorithms by leaving the Phy online for very short sequences during the creation of the signal. The procedure outlined is appropriate for any HBA design that has a COMRESET polling interval greater than 25 microseconds.

1. Set Phy to offline by writing SControl.DET to 4h.
2. Set Phy to reset state by writing SControl.DET to 1h.
3. Wait 5 microseconds to allow charging time for DC coupled Phy designs.
4. Set Phy to online state by writing SControl.DET to 0h.
5. Wait 20 microseconds to allow COMRESET burst to be transmitted to the device.
6. Set Phy to offline by writing SControl DET to 4h.
7. Wait 1.975 milliseconds to satisfy T1 timing as specified in Table 1.

8. Repeat steps 2-6.
9. Wait 7.975 milliseconds to satisfy T2 timing as specified in Table 1.

10. Repeat steps 2-6.
11. Wait 1.975 milliseconds to satisfy T1 timing as specified in Table 1.

12. Repeat steps 2-6
13. Wait 7.975 milliseconds to satisfy T2 timing as specified in Table 1.

14. Set Phy to reset state by writing SControl.DET to 1h.
15. Wait 5 microseconds to allow charging time for DC coupled Phy designs.
16. Set Phy to online state by writing SControl.DET to 0h.
17. Wait up to 10 milliseconds for SStatus.DET = 3h
18. If SStatus.DET != 3h, go to step 1 to restart the process.

The procedure is also outlined in pseudocode on the following page.

```
//
// Continue to perform this procedure until SStatus.DET == 3.
//
while (SStatus.DET != 3)
{
   SControl.DET = 4;             // Turn off Phy

   //
   // Mimic out the COMRESET bursts at the appropriate T1/T2 timing intervals.
   //
   for (i = 0; i < 4; i++)
   {
      SControl.DET = 1;          // Place HBA in reset state
      Sleep(5);                  // Wait for PHY to charge, in microseconds
      SControl.DET = 0;          // Issue COMRESET
      Sleep(20);                 // Wait for COMRESET to be sent
      SControl.DET = 4;          // Turn off Phy

      if ((i == 0) || (i == 2))
      {
         Sleep(1975);            // Wait T1 time minus time already waited
      }
      else if ((i == 1) || (i == 3))
      {
         Sleep(7975);            // Wait T2 time minus time already waited
      }
   }

   //
   // Issue final COMRESET of the burst.
   //
   SControl.DET = 1;             // Place HBA in reset state
   Sleep(5);                     // Wait for PHY to charge, in microseconds
   SControl.DET = 0;             // Issue COMRESET


   //
   // Wait up to 10 milliseconds for PhyRdy.
   //
   for (i = 0; i < 10000; i++)
   {
      if (SStatus.DET == 3)
      {
         break;                  // Stop procedure if SStatus.DET == 3
      }
      Sleep(1);                  // Wait 1 microsecond
   }
}
```