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Subject: SAM-3, SPC-3, and SBC-2 power conditions proposal

Introduction

There have been several modifications and clarification to power conditions (e.g., moving several items from SBC to SPC and deleting the SLEEP condition). The following is an attempt to complete reconciliation of all of these, perform some clean-up, and remove duplication. This proposal is based on SAM-3r05, SPC-3r12, and SBC-2r08. Revision 2 of this proposal separated the subclauses for SPC and SBC that were recommended in revision 1 so that there is a model subclause for each of those draft standards. Revision 3 of this proposal includes some very minor editorial modifications that were recommended at the May 7th CAP working group meeting.

In SAM-3: In Table 31 - Task Management Functions, delete WAKEUP. This was previously defined to cause a device to return from SLEEP, and all other references to this condition have been deleted.

In SAM-3: Delete subclause 7.9 WAKEUP.

In SPC-3: Replace subclause 5.8 with the following:

5.8 Power conditions

5.8.1 Power conditions overview

The optional Power Condition mode page (see 7.4.11) allows an application client to modify the behavior of a target port and/or logical unit in a manner that may reduce power consumption. This behavior modification is invoked by enabling and setting the idle condition timer and/or the standby condition timer using the mode page.

In addition to the Power Condition mode page, the power condition of a target port and/or logical unit may be controlled by the START STOP UNIT command (see SBC-2 or RBC). If both the Power Condition mode page and the START STOP UNIT command methods are being used to control the power condition of the same target port and/or logical unit, then any START STOP UNIT command's power condition specification shall override the Power Condition mode page's power control and may disable the idle condition and standby condition timers.

There shall be no notification to the application client that a target port and/or logical unit has transitioned from one power condition to another. An application client may determine the current power condition of a logical unit by issuing a REQUEST SENSE command (see 6.25).

No power condition shall affect the supply of any power required for proper operation of the service delivery subsystem.

Logical units that contain cache memory shall write all cached data to the medium for the logical unit (as a logical unit would do in response to a SYNCHRONIZE CACHE command as described in SBC-2) prior to entering into any power condition that prevents accessing the media (e.g., before a hard drive stops its spindle motor during transition to the standby power condition).

Table 36 describes the power conditions.

Table 36 — Power condition description

Power condition	Description
active	While in the active power condition: a) a device server is capable of responding to all of its supported commands including media access requests; b) a logical unit completes processing of operations in the shortest time when compared to the time required for completion while in the idle or standby power conditions; and c) a logical unit may consume more power than when in the idle or standby power conditions (e.g., a disk drive's spindle motor may be active).
idle	While in the idle power condition: a) a device server is capable of responding to all of its supported commands including media access requests; b) a logical unit may take longer to complete processing a command than it would while in the active power condition (e.g., the device may have to activate some circuitry before processing a command); and c) a logical unit may consume less power than when in the active power condition.
standby	While in the standby power condition: a) device server is not capable of processing media access commands; and b) logical unit may consume less power than when in the idle power condition (e.g., a disk drive's spindle motor is stopped).

5.8.2 Power condition state machine

5.8.2.1 Power condition state machine overview

The PC (power condition) state machine describes the logical unit power states and transitions resulting from Power Condition mode page settings.

The PC states are as follows:

a) PC0:Powered_on (see 5.8.2.2) (initial state);
b) PC1:Active (see 5.8.2.3);
c) PC2:Idle (see 5.8.2.4); and
d) PC3:Standby (see 5.8.2.5).

The PC state machine stall start in the PC0:Powered_on state after power on.
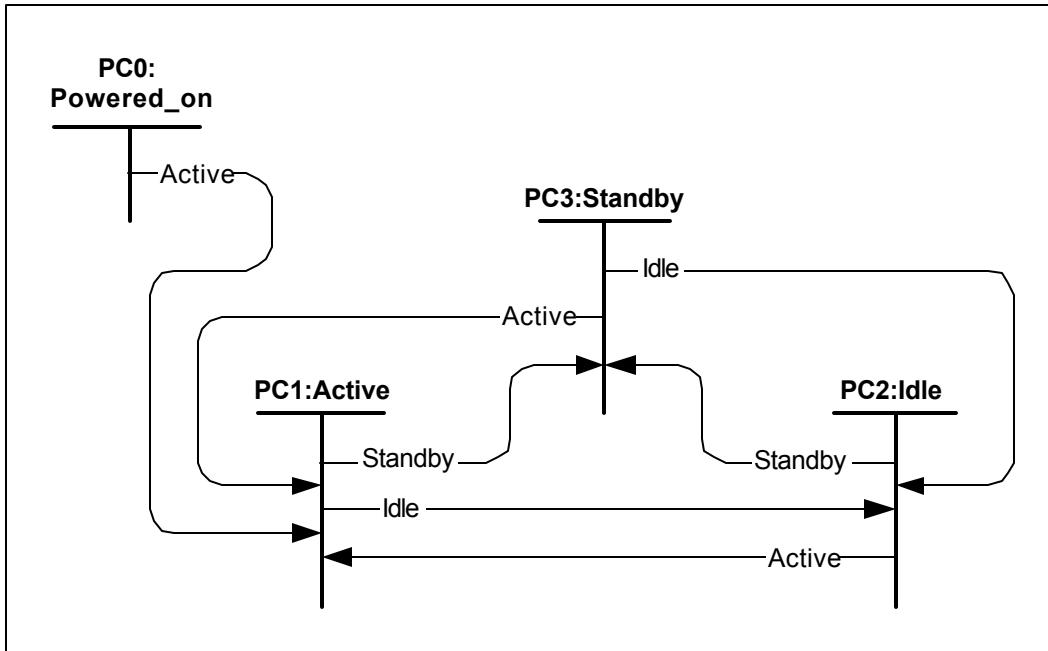
Figure a describes the PC state machine.

Figure a — Power condition state machine

5.8.2.2 PC0:Powered_on state

5.8.2.2.1 PC0:Powered_on state description

The logical unit shall enter this state upon power on. This state consumes zero time.

5.8.2.2.2 Transition PC0:Powered_on to PC1:Active

This transition shall occur after the logical unit is ready to begin its power on initialization.

5.8.2.3 PC1:Active state

5.8.2.3.1 PC1:Active state description

While in this state, if power on initialization is not complete, then the logical unit shall complete its power on initialization.

While in this state, if power on initialization is complete, then:

   a) a logical unit is in the active power condition;
   b) if the idle condition timer is active, then the idle condition timer is running; and
   c) if the standby condition timer is active, then the standby condition timer is running.

5.8.2.3.2 Transition PC1:Active to PC2:Idle

This transition shall occur after:

   a) the idle condition timer is active; and
   b) the idle condition timer is zero.

5.8.2.3.3 Transition PC1:Active to PC3:Standby

This transition shall occur after:

   a) the standby condition timer is active; and
   b) the standby condition timer is zero.

5.8.2.4 PC2:Idle state

5.8.2.4.1 PC2:Idle state description

While in this state:

    a)   a logical unit is in the idle power condition; and
    b)   if the standby condition timer is active, then the standby condition timer is running.

5.8.2.4.2 Transition PC2:Idle to PC1:Active

This transition shall occur after the device server receives a command that requires the logical unit to be in the PC1:Active state to process the command.

5.8.2.4.3 Transition PC2:Idle to PC3:Standby

This transition shall occur after:

    a)   the standby condition timer is active; and
    b)   the standby condition timer is zero.

5.8.2.5 PC3:Standby state

5.8.2.5.1 PC3:Standby state description

While in this state:

    a)   a logical unit is in the standby power condition.

5.8.2.5.2 Transition PC3:Standby to PC1:Active

This transition shall occur after the device server receives a command that requires the logical unit to be in the PC1:Active state to process the command.

5.8.2.5.3 PC3:Standby to PC2:Idle

This transition shall occur after the device server receives a command that requires the logical unit to be in the PC2:Idle state to process the command.

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In SPC-3: Replace subclause 7.4.11 with the following:

7.4.11 Power Condition mode page

The Power Condition mode page provides an application client methods to control the power condition of a target port and/or logical unit (see 5.8). These methods include causing the target port and/or logical unit to transition to a specified power condition without delay and activating and setting of idle condition and standby condition timers to specify that the logical unit wait for a period of inactivity before transitioning to a specified power condition.

When a device server receives a command while in a power condition based on a setting in the Power Condition mode page, the logical unit shall transition to the power condition that allows the command to be processed. If either the idle condition timer or the standby condition timer has been set, they shall be reset on receipt of the command. On completion of the command, the timer(s) shall be started.

Logical units that contain cache memory shall write all cached data to the medium for the logical unit (as a logical unit would do in response to a SYNCHRONIZE CACHE command as described in SBC-2) prior to entering into any power condition that prevents accessing the media (e.g., before a hard drive stops its spindle motor during transition to the standby power condition).

The logical unit shall use the values in the Power Condition mode page to control its power condition after a power on or a hard reset until a START STOP UNIT command setting a power condition is received.

Table 236 defines the Power Condition mode page.

[Insert the table from the current draft here. There are no proposed changes for this table.]

The IDLE and STANDBY bits specify which timers are active.

If the IDLE bit is set to one and the STANDBY bit is set to zero, then the idle condition timer is active and the device server shall transition to the idle power condition when the idle condition timer is zero. If the IDLE bit is set to zero, then the device server shall ignore the idle condition timer.

If the STANDBY bit is set to one and the IDLE bit is set to zero, then the standby condition timer is active and the device server shall transition to the standby power condition when the standby condition timer is zero. If the STANDBY bit is set to zero, then the device server shall ignore the standby condition timer.

If both the IDLE and STANDBY bits are set to one, then both timers are active and run concurrently. When the idle condition timer is zero the device server shall transition to the idle power condition. When the standby condition timer is zero the device server shall transition to the standby power condition. If the standby condition timer is zero before the idle condition timer is zero, then the logical unit shall transition to the standby power condition.

The value in the IDLE CONDITION TIMER field specifies the inactivity time in 100 millisecond increments that the logical unit shall wait before transitioning to the idle power condition when the IDLE bit is set to one. The idle condition timer is expired when:

   a) the IDLE CONDITION TIMER field is set to zero; or
   b) the number of milliseconds specified by the value in the IDLE CONDITION TIMER field times 100 milli-seconds has elapsed since the last activity.

The value in the STANDBY CONDITION TIMER field specifies the inactivity time in 100 millisecond increments that the logical unit shall wait before transitioning to the standby power condition when the STANDBY bit is set to one. The standby condition timer is expired when:

   a) the STANDBY CONDITION TIMER field is set to zero; or
   b) the number of milliseconds specified by the value in the STANDBY CONDITION TIMER field times 100 milliseconds has elapsed since the last activity.

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In SBC-2: Add the following in the Models clause.

4.2.1.0 START STOP UNIT and power conditions

4.2.1.0.1 START STOP UNIT and power conditions overview

The START STOP UNIT command (see 5.2.24) allows an application client to control the power condition of a logical unit in a manner that may reduce power consumption. This behavior modification includes specifying that the device server enable or disable the block device for media access operations by controlling certain power conditions and timers.

In addition to the START STOP UNIT command, the power condition of a logical unit may be controlled by the Power Condition mode page (see SPC-3). If both the START STOP UNIT command and the Power Condition mode page methods are being used to control the power condition of the same logical unit, then any START STOP UNIT command's power condition specification shall override the Power Condition mode page's power control.

There shall be no notification to the initiator that a logical unit has transitioned from one power condition to another. An application client may determine the current power condition of a logical unit by issuing a REQUEST SENSE command (see SPC-3).

No power condition shall affect the supply of any power required for proper operation of the service delivery subsystem.

4.2.1.0.2 START STOP UNIT and power conditions state machine

4.2.1.0.2.1 START STOP UNIT and power conditions state machine overview

The SSU_PC (start stop unit power condition) state machine for logical units implementing the START STOP UNIT command describes the logical unit power states and transitions resulting from settings by the START STOP UNIT command and settings in the Power Condition mode page (see SPC-3).

The SSU_PC states are as follows:

 a) SSU_PC0:Powered_on (see 4.2.1.0.2.2) (initial state);
 b) SSU_PC1:Active (see 4.2.1.0.2.3);
 c) SSU_PC2:Idle(see 4.2.1.0.2.4);
 d) SSU_PC3:Standby (see 4.2.1.0.2.5); and
 e) SSU_PC4:Stopped (see 4.2.1.0.2.6).

The SSU_PC state machine stall start in the SSU_PC0:Powered_on state after power on.

> NOTE 1 - The SSU_PC state machine is an enhanced version of the Power Condition state machine described in SPC-3.
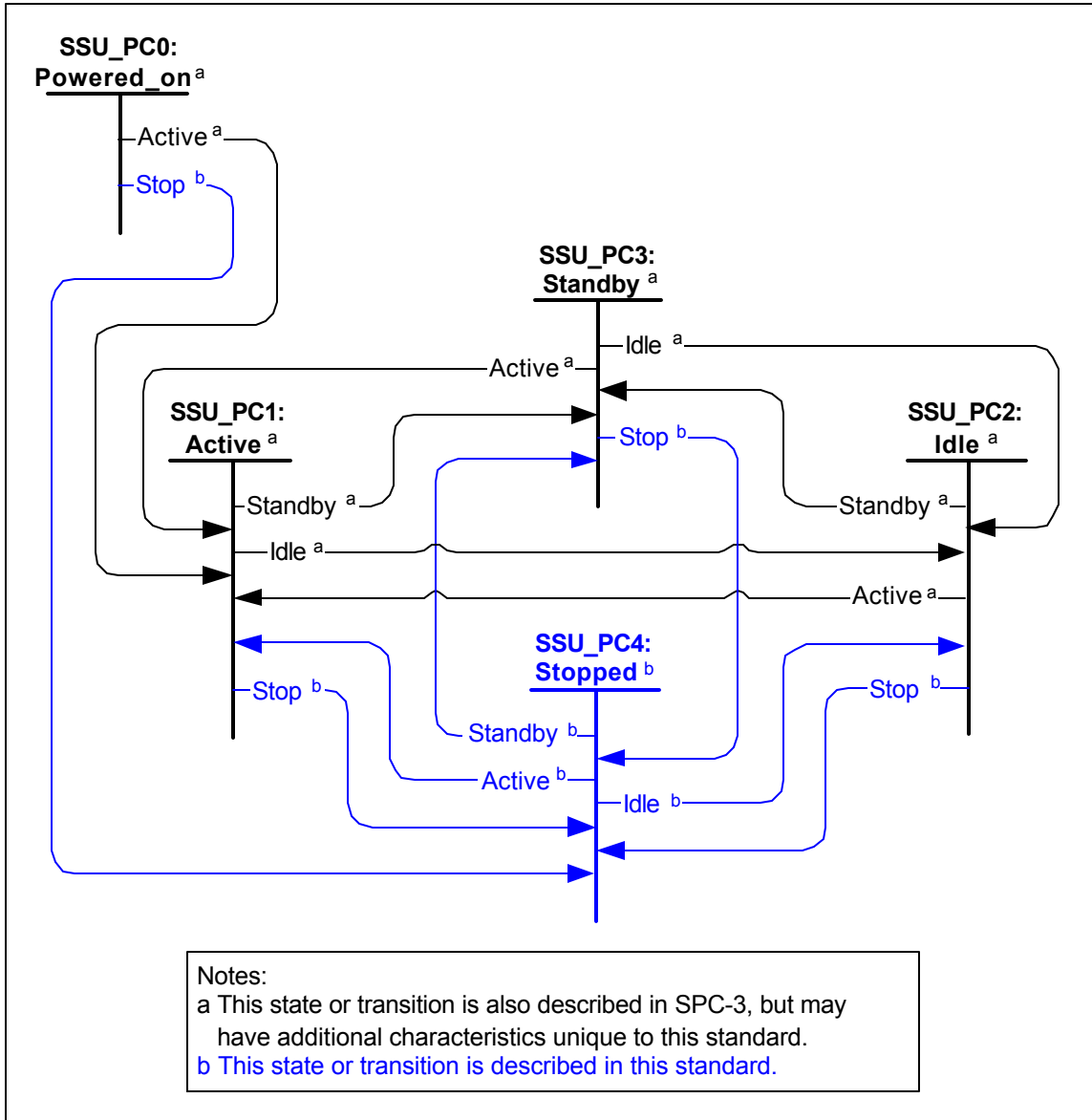
Figure b describes the SSU_PC state machine.

Figure b — Power condition state machine for logical units implementing the START STOP UNIT command

4.2.1.0.2.2 SSU_PC0:Powered_on state

4.2.1.0.2.2.1 SSU_PC0:Powered_on state description

This logical unit shall enter this state upon power on. This state consumes zero time.

4.2.1.0.2.2.2 Transition SSU_PC0:Powered_on to SSU_PC1:Active

This transition shall occur if the logical unit has been configured to transition to the SSU_PC1:Active state.

4.2.1.0.2.2.3 Transition SSU_PC0:Powered_on to SSU_PC4:Stopped

This transition shall occur if the logical unit has been configured to transition to the SSU_PC4:Stopped state.

4.2.1.0.2.3 SSU_PC1:Active state

4.2.1.0.2.3.1 SSU_PC1:Active state description

While in this state, if power on initialization is not complete, then the logical unit completes its power on initialization.

While in this state, after power on initialization is complete, then:

   a) a logical unit is in the active power condition (see SPC-3);
   b) if the idle condition timer is active (see SPC-3) and not disabled (see 5.2.24), then the idle condition timer is running; and
   c) if the standby condition timer is active (see SPC-3) and not disabled (see 5.2.24), then the standby condition timer is running.

4.2.1.0.2.3.2 Transition SSU_PC1:Active to SSU_PC2:Idle

This transition shall occur after:

   a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to IDLE;
   b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to FORCE_IDLE_0; or
   c) the idle condition timer is active (see SPC-3), enabled (see 5.2.24), and zero.

4.2.1.0.2.3.3 Transition SSU_PC1:Active to SSU_PC3:Standby

This transition shall occur after:

   a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to STANDBY);
   b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to FORCE_STANDBY_0; or
   c) the standby condition timer is active (see SPC-3), enabled (see 5.2.24), and zero.

4.2.1.0.2.3.4 Transition SSU_PC1:Active to SSU_PC4:Stopped

This transition shall occur after the device server receives a START STOP UNIT command with the START bit set to zero and the POWER CONDITION field set to START_VALID.

4.2.1.0.2.4 SSU_PC2:Idle state

4.2.1.0.2.4.1 SSU_PC2:Idle state description

While in this state:

   a) a logical unit is in the idle power condition (see SPC-3); and
   b) if the standby condition timer is active (see SPC-3) and not disabled (see 5.2.24), then the standby condition timer is running.

4.2.1.0.2.4.2 Transition SSU_PC2:Idle to SSU_PC1:Active

This transition shall occur after:

   a) the device server receives a START STOP UNIT command with the START bit set to one;
   b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to ACTIVE; or
   c) the device server receives a command that requires the logical unit to be in the SSU_PC1:Active state to process the command.

4.2.1.0.2.4.3 Transition SSU_PC2:Idle to SSU_PC3:Standby

This transition shall occur after:

   a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to STANDBY;
   b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to FORCE_STANDBY_0; or
   c) the standby condition timer is active (see SPC-3), enabled (see 5.2.24), and expired.

4.2.1.0.2.4.4 Transition SSU_PC2:Idle to SSU_PC4:Stopped

This transition shall occur after the device server receives a START STOP UNIT command with the START bit set to zero.

4.2.1.0.2.5 SSU_PC3:Standby state

4.2.1.0.2.5.1 SSU_PC3:Standby state description

While in this state a logical unit is in the standby power condition (see SPC-3).

4.2.1.0.2.5.2 Transition SSU_PC3:Standby to SSU_PC1:Active

This transition shall occur after:

   a) the device server receives a START STOP UNIT command with the START bit set to one;
   b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to ACTIVE; or
   c) the device server receives a command that requires the logical unit to be in the SSU_PC1:Active state to process the command.

4.2.1.0.2.5.3 SSU_PC3:Standby to SSU_PC2:Idle

This transition shall occur after:

   a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to IDLE;
   b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to FORCE_IDLE_0; or
   c) the device server receives a command that requires the logical unit to be in the SSU_PC2:Idle state to process the command.

4.2.1.0.2.5.4 SSU_PC3:Standby to SSU_PC4:Stopped

This transition shall occur after the device server receives a START STOP UNIT command with the START bit set to zero.

4.2.1.0.2.6 SSU_PC4:Stopped state

4.2.1.0.2.6.1 SSU_PC4:Stopped state description

While in this state:

   a) the device server is not capable of processing media access commands. Any media access commands received while in this state shall cause the device server to terminate the command with a CHECK CONDITION status with a sense key of NOT READY and an additional sense code of LOGICAL UNIT NOT READY, INITIALIZING CMD REQUIRED; and
   b) the logical unit may consume less power than when in the SSU_PC1:Active, SSU_PC2:Idle, or SSU_PC3:Standby states.

4.2.1.0.2.6.2 Transition SSU_PC4:Stopped to SSU_PC1:Active

This transition shall occur after:

   a) the device server receives a START STOP UNIT command with the START bit set to one; or
   b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to ACTIVE.

4.2.1.0.2.6.3 Transition SSU_PC4:Stopped to SSU_PC2:Idle

This transition shall occur after:

   a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to IDLE; or
   b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to FORCE_IDLE_0.

4.2.1.0.2.6.4 Transition SSU_PC4:Stopped to SSU_PC3:Standby

This transition shall occur after:

   a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to STANDBY; or
   b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to FORCE_STANDBY_0.

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In SBC-2: Replace subclause 5.2.24 with the following:

5.2.24 START STOP UNIT

5.2.24.1 START STOP UNIT description

The START STOP UNIT command (see 5.2.24) provides an application client a method to control the power condition of a logical unit (see 4.2.1.0). This includes specifying that the device server enable or disable the block device for media access operations by controlling certain power conditions and timers.

Logical units that contain cache memory shall write all cached data to the medium for the logical unit (as a logical unit would do in response to a SYNCHRONIZE CACHE command, see x.y) prior to entering into any power condition that prevents accessing the media (e.g., before a hard drive stops its spindle motor during transition to the stopped power condition).

See 4.2.1.8 for reservation requirements for this command.

Table 58 defines the START STOP UNIT command CDB.

[Insert the table from the current draft here. There are no proposed changes for this table.]

If the immediate (IMMED) bit is set to zero, then status shall be returned after the operation is completed. If the IMMED bit set to one, then status shall be returned as soon as the command descriptor block has been validated.

The optional POWER CONDITION field is used to specify that the logical unit be placed into a power condition or to adjust a timer as defined in table 59. If this field is supported and has a value other than 0h then the START and LOEJ bits shall be ignored.

Table 59 — POWER CONDITIONS field

Code	Name	Description
0h	START_VALID	The START and LOEJ bits are valid.
1h	ACTIVE	Place the device into the active power condition.
2h	IDLE	Place the device into the idle power condition.
3h	STANDBY	Place the device into the standby power condition.
4h	Reserved	Reserved
5h	Obsolete	Obsolete
6h	Reserved	Reserved
7h	LU_CONTROL	Transfer control of power conditions to the block device.
8h-9h	Reserved	Reserved
Ah	FORCE_IDLE_0	Force the idle condition timer to zero.
Bh	FORCE_STANDBY_0	Force the standby condition timer to zero.
Ch-Fh	Reserved	Reserved

If the START STOP UNIT command is issued with the POWER CONDITIONS field set to ACTIVE, IDLE, or STANDBY, then:

a) the logical unit shall transition to the specified power condition;
b) the logical unit shall change power conditions only after receipt of another START STOP UNIT command or a logical unit reset;
c) the device server shall disable the idle condition and standby condition timers if they are active (see SPC-3) until another START STOP UNIT command is received that returns control of the power condition to the logical unit, or a logical unit reset occurs; and
d) the device server shall terminate any command received that requires more power than allowed by the START STOP UNIT command's most recent power condition setting. The command shall be terminated with a CHECK CONDITION status with the sense key set to ILLEGAL REQUEST and the additional sense code set to LOW POWER CONDITION ACTIVE.

If the START STOP UNIT command is issued with the POWER CONDITIONS field set LU_UCONTROL, then the device server shall enable the idle condition timer and the standby condition timer if they are active (see SPC-3).

If the START STOP UNIT command is issued with the POWER CONDITIONS field set to FORCE_IDLE_0 or FORCE_STANDBY_0, then the device server shall:

a) force the selected timer to zero, cause the logical unit to transition to the selected power condition, and return control of the power condition to the device server; or
b) terminate the START STOP UNIT command that selects a timer that is not supported by the device server or a timer that is not active. The command shall be terminated with a CHECK CONDITION status with the sense key set to ILLEGAL REQUEST and the additional sense code set to INVALID FIELD IN CDB.

It is not an error to specify that the logical unit transition to a power condition in which it currently is.

If the load eject (LOEJ) bit is set to zero, then the logical unit shall take no action regarding loading or ejecting the medium. If the LOEJ bit is set to one, then the logical unit shall unload the medium if the START bit is set to zero. If the LOEJ bit is set to one, then the logical unit shall load the medium if the START bit is set to one.

If the START bit is set to zero, then the logical unit shall transition to the stopped power condition and, if activated, disable the idle condition and standby condition timers. If the START bit set to one, then the logical unit shall transition to the active power condition and, if activated, enable the idle condition and standby condition timers.