Maxtor Corporation
500 McCarthy Boulevard
Milpitas, CA 95035 USA

To: **T10 CAP Working Group**
Contact: **Mark Evans**
Phone: 408-894-5310
Email: mark_evans@maxtor.com
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Subject: SAM-3, SPC-3, and SBC-2 power conditions proposal

Introduction

There have been several modifications and clarification to power conditions of late (e.g., moving several items from SBC to SPC and deleting the SLEEP condition). The following is an attempt to complete reconciliation of all of these, perform some clean-up, and remove duplication. This proposal is based on SAM-3r03, SPC-3r09, and SBC-2r08.

For SAM-3:

In Table 32 - Task Management Functions, delete WAKEUP. This was previously defined to cause a device to return from SLEEP, and all other references to this condition have been deleted.

Delete subclause 7.9 WAKEUP.

For SPC-3:

Delete subclause 5.8 Power conditions.

Replace subclause 8.4.11 with the following:

8.4.11 Power Condition mode page

8.4.11.1 Power Condition mode page description

The Power Condition mode page (see table 231) provides the application client methods to control the power state of a logical unit. These methods include causing the logical unit to immediately transition to a specified power state and the setting of idle condition and standby condition timers to specify that the logical unit wait for a period of inactivity before transitioning to a specified power state.

In addition to the Power Condition mode page, the power state of a logical unit may be controlled by the START STOP UNIT command (see SBC-2 or RBC). If both the Power Condition mode page and the START STOP UNIT command methods are being used to control the power state of the same logical unit, then any START STOP UNIT command's power state specification shall override the Power Condition mode page's power control.

There shall be no notification to the initiator that a logical unit has transitioned from one power state to another. The application client may determine the current power state of a logical unit by issuing a REQUEST SENSE command (see 7.24).

No power state shall affect the supply of any power required for proper operation of the service delivery subsystem.

When a device server receives a command while in a power state based on a setting in the Power Condition mode page, the logical unit shall transition to the power state that allows the command to execute. If either the idle timer or the standby timers have been set, they shall be reset on receipt of the command. On completion of the command the timer(s) shall be restarted.

Logical units that contain cache memory shall implicitly perform a SYNCHRONIZE CACHE command (see SBC-2) for the entire medium prior to entering into any power state that prevents accessing the media (e.g., before a hard drive stops its spindle motor during transition to the standby power state).

The logical unit shall use the Power Condition mode page to control its power state after a power on or a hard reset until a START STOP UNIT command is received that sets its power state.

Table 231 - Power Condition mode page [no change, included for reference]

Bit / Byte	0	1	2	3	4	5	6	7
0	PS	SPF (0b)	PAGE CODE (1Ah)					
1	PAGE LENGTH (0Ah)							
2	Reserved							
3	Reserved						IDLE	STANDBY
4	(MSB)	IDLE CONDITION TIMER						
7								(LSB)
8	(MSB)	STANDBY CONDITION TIME						
11								(LSB)

If the IDLE bit is set to one and the STANDBY bit is set to zero, then the device server shall use the idle condition timer to determine when to transition to the idle state. If the IDLE bit is set to zero, then the device server shall not use the idle condition timer to determine when to transition to the idle state.

If the STANDBY bit is set to one and the IDLE bit is set to zero, then the device server shall use the standby condition timer to determine when to transition to the standby state. If the STANDBY bit is set to zero, then the device server shall not use the standby condition timer to determine when to transition to the standby state.

If both the IDLE and STANDBY bits are set to one, then both timers run concurrently. The device server shall use the idle condition timer to determine when to transition to the idle state and the standby condition timer to determine when to transition to the standby state. If the standby condition timer expires before the idle condition time, then the logical unit shall transition to the standby state.

The value in the IDLE CONDITION TIMER field specifies the inactivity time in 100 millisecond increments that the logical unit shall wait before transitioning to the idle state when the IDLE bit is set to one. The idle condition timer is zero when:

a) the IDLE CONDITION TIMER field is set to zero; or
b) the number of milliseconds specified by the value in the IDLE CONDITION TIMER field times 100 milliseconds has elapsed since the last activity.

The value in the STANDBY CONDITION TIMER field specifies the inactivity time in 100 millisecond increments that the logical unit shall wait before transitioning to the standby state when the STANDBY bit is set to one. The standby condition timer is zero when:

a) the STANDBY CONDITION TIMER field is set to zero; or
b) the number of milliseconds specified by the value in the STANDBY CONDITION TIMER field times 100 milliseconds has elapsed since the last activity.

8.4.11.2 Power condition state machine

The power condition state machine (PC) describes the logical unit power states and transitions resulting from Power Condition mode page settings.

The PC states are as follows:

a) PC_0:Powered_on;
b) PC_1:Active;
c) PC_2:Idle; and
d) PC_3:Standby.

The PC state machine stall start in the PC_0:Powered_on state after power on.

Figure PC describes the PC state machine.

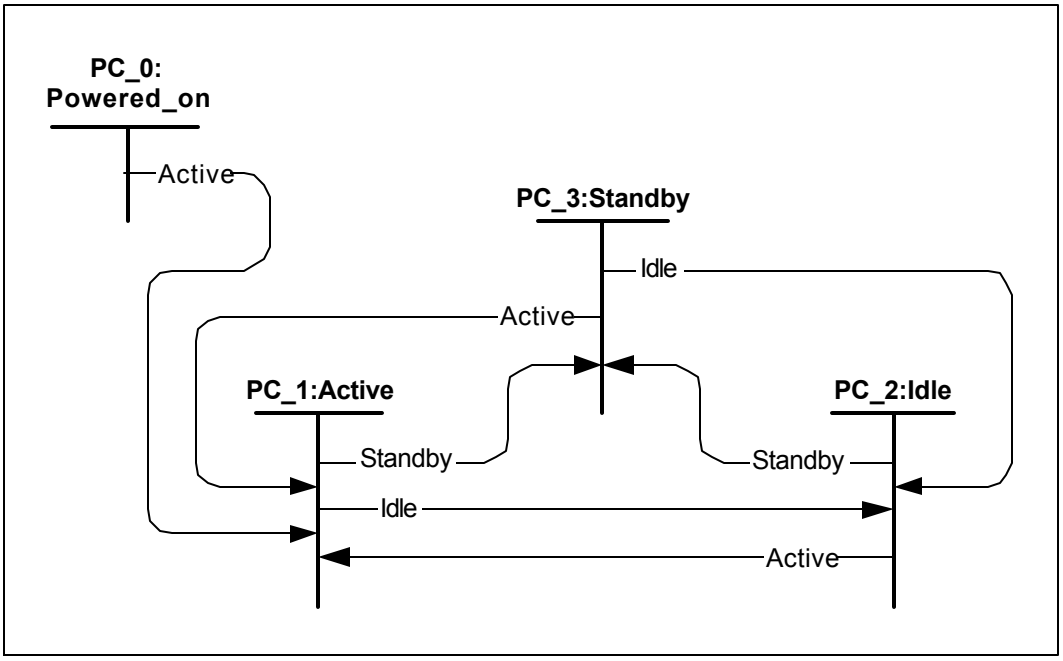

Figure PC – Power condition state machine

8.4.11.2.1 PC_0:Powered_on state

8.4.11.2.1.1 PC_0:Powered_on state description

The logical unit shall enter this state upon power on. This state consumes zero time.

8.4.11.2.1.2 Transition PC_0:Powered_on to PC_1:Active

This transition shall occur when:

a) the logical unit is ready to begin its power on initialization.

8.4.11.2.2 PC_1:Active state

8.4.11.2.2.1 PC_1:Active state description

While in this state, if power on initialization is not complete, then:

a) the logical unit completes its power on initialization.

While in this state, if power on initialization is complete, then:

a) the device server is capable of responding to all of its supported commands including media access requests;
b) the logical unit completes processing operations in the shortest time when compared to the time required for completion while in the PC_2:Idle or PC_3:Standby states;
c) the logical unit may consume more power than when in the PC_2:Idle or PC_3:Standby states (e.g., a disk drive's spindle motor may be active);
d) if the IDLE bit is set to one, then the idle condition timer is running; and
e) if the STANDBY bit is set to one, then the standby condition timer is running.

8.4.11.2.2.2 Transition PC_1:Active to PC_2:Idle

This transition shall occur when:

a) the IDLE bit is set to one; and
b) the idle condition timer is zero.

8.4.11.2.2.3 Transition PC_1:Active to PC_3:Standby

This transition shall occur when:

a) the STANDBY bit is set to one; and
b) the standby condition timer is zero.

8.4.11.2.3 PC_2:Idle state

8.4.11.2.3.1 PC_2:Idle state description

While in this state:

a) the device server is capable of responding to all its supported commands including media access requests;
b) the logical unit may take longer to complete processing a command than it would while in the PC_1:Active state (e.g., the device may have to activate some circuitry before processing a command);
c) the logical unit may consume less power than when in the PC_1:Active state; and
d) if the STANDBY bit is set to one, then the standby condition timer is running.

8.4.11.2.3.2 Transition PC_2:Idle to PC_1:Active

This transition shall occur when:

a) the device server receives a command that requires the logical unit to be in the PC_1:Active state to process the command.

8.4.11.2.3.3 Transition PC_2:Idle to PC_3:Standby

This transition shall occur when:

a) the STANDBY bit is set to one; and
b) the standby timer is zero.

8.4.11.2.4 PC_3:Standby state

8.4.11.2.4.1 PC_3:Standby state description

While in this state:

a) the device server is not capable of processing media access commands; and
b) the logical unit may consume less power than when in the PC_2:Idle state (e.g., a disk drive's spindle motor is stopped).

8.4.11.2.4.2 Transition PC_3:Standby to PC_1:Active

This transition shall occur when:

a) the device server receives a command that requires the logical unit to be in the PC_1:Active state to process the command.

8.4.11.2.4.3 PC_3:Standby to PC_2:Idle

This transition shall occur when:

a) the device server receives a command that requires the logical unit to be in the PC_2:Idle state to process the command.

For SBC-2:

In the Definitions subclause delete 3.1.30. wakeup and 3.1.31. wakeup event.

Replace subclause 5.2.24 with the following:

5.2.24 START STOP UNIT

5.2.24.1 START STOP UNIT description

The START STOP UNIT command (see Table 56) provides the application client a method to control the power state of a logical unit. This includes specifying that the device server enable or disable the block device for media access operations by controlling certain power states and timers. In addition to the START STOP UNIT command, the power state of a logical unit may be controlled by the Power Condition mode page (see SPC-3). If both the START STOP UNIT command and the Power Condition mode page methods are being used to control the power state of the same logical unit, then any START STOP UNIT command's power state specification shall override the Power Condition mode page's power control.

There shall be no notification to the initiator that a logical unit has transitioned from one power state to another. The application client may determine the current power state of a logical unit by issuing a REQUEST SENSE command (see SPC-3).

No power state shall affect the supply of any power required for proper operation of the service delivery subsystem.

Table 56. START STOP UNIT command [no change, included for reference]

Bit / Byte	0	1	2	3	4	5	6	7
0	OPERATION CODE (1Bh)							
1	Reserved							IMMED
2	Reserved							
3	Reserved							
4	POWER CONDITIONS				Reserved		LOEJ	START
5	Control							

See 4.2.1.8 for reservation requirements for this command.

If the immediate (IMMED) bit is set to zero, then status shall be returned after the operation is completed. If the IMMED bit set to one, then status shall be returned as soon as the command descriptor block has been validated.

The optional POWER CONDITIONS field is used to specify that the logical unit be placed in a power state or to adjust a timer as defined in Table 57. If this field is supported and has a value other than 0h then the START and LOEJ bits shall be ignored. If this field is not supported and has value other than 0h, then the device server shall return a CHECK CONDITION status with the sense key set to ILLEGAL REQUEST and the additional sense code set to INVALID FIELD IN CDB.

Table 57. POWER CONDITIONS field

Code	Name	Description
0h	START_VALID	The START and LOEJ bits are valid.
1h	ACTIVE	Place the device into the active state.
2h	IDLE	Place the device into the idle state.
3h	STANDBY	Place the device into the standby state.
4h	Reserved.	Reserved
5h	Obsolete.	Obsolete
6h	Reserved.	Reserved
7h	LU_CONTROL	Transfer control of power states to the block device.
8h-9h	Reserved.	Reserved
Ah	FORCE_IDLE_0	Force the idle condition timer to zero.
Bh	FORCE_STANDBY_0	Force the standby condition timer to zero.
Ch-Fh	Reserved.	Reserved

If the START STOP UNIT command is issued with the POWER CONDITIONS field set to ACTIVE (1h), IDLE (2h), or STANDBY (3h), then:

a) the logical unit shall transition to the specified power state;
b) the logical unit shall change power states only on receipt of another START STOP UNIT command or a logical unit reset;
c) the device server shall reset the idle condition and standby condition timers (see SPC-3), if they are active, until another START STOP UNIT command is received that returns control of the power state to the logical unit, or a logical unit reset occurs; and

d) the device server shall terminate any command received that requires more power than allowed by the START STOP UNIT command's most recent power state setting with a CHECK CONDITION status with the sense key set to ILLEGAL REQUEST and the additional sense code set to LOW POWER CONDITION ACTIVE.

If the START STOP UNIT command is issued with the POWER CONDITIONS field set FORCE_IDLE_0 (Ah) or FORCE_STANDBY_0 (Bh), then the device server shall:

a) force the selected timer to be zero. Forcing the timer to zero shall place the logical unit into the same power condition that would have occurred if the timer would have timed out. After the timer is set to be zero, control of the power state is returned to the device server; or
b) terminate any START STOP UNIT command that selects a timer that is not supported by the device server (or a timer that has been disabled) with a CHECK CONDITION status with the sense key set to ILLEGAL REQUEST and the additional sense code set to INVALID FIELD IN CDB.

It is not an error to specify that the logical unit transition to a power state in which it currently is.

If the load eject (LOEJ) bit is set to zero, then the logical unit shall take no action regarding loading or ejecting the medium. If the LOEJ bit is set to one, then the logical unit shall unload the medium if the START bit is set to zero. If the LOEJ bit is set to one, then the logical unit shall load the medium if the START bit is set to one.

If the START bit is set to zero, then the logical unit shall transition to the stopped power state and, if enabled by the Power Condition mode page, disable the idle condition and standby condition timers. If the START bit set to one, then the logical unit shall transition to the active power state and, if enabled by the Power Condition mode page, enable the idle condition and standby condition timers.

Logical units that contain cache memory shall implicitly perform a SYNCHRONIZE CACHE command for the entire medium prior to executing the STOP UNIT command.

5.2.24.2 Power condition state machine for logical units implementing START STOP UNIT

The power condition state machine for logical units implementing the START STOP UNIT command (PC_SSU) describes the logical unit power states and transitions resulting from settings by the START STOP UNIT command and settings in the Power Condition mode page (see the Power Conditions mode page subclause in SPC-3).

The PC_SSU states are as follows:

a) PC_SSU_0:Powered_on;
b) PC_SSU_1:Active;
c) PC_SSU_2:Idle;
d) PC_SSU_3:Standby; and
e) PC_SSU_4:Stopped.

The PC_SSU state machine stall start in the PC_SSU_0:Powered_on state after power on.

Note: The PC_SSU state machine is an enhanced version of the Power Condition state machine described in SPC-3. The PC_SSU_0:Powered_on, PC_SSU_1:Active, PC_SSU_2:Idle, and PC_SSU_3:Standby states and their transitions to each other described in this standard are analogous to the PC_0:Powered_on, PC_1:Active, PC_2:Idle, and PC_3:Standby states and their transitions, respectively, as described in the Power Condition mode page subclause in SPC-3. The PC_SSU_4:Stopped state and its related transitions are unique for block devices.

Figure PC_SSU describes the PC_SSU state machine.

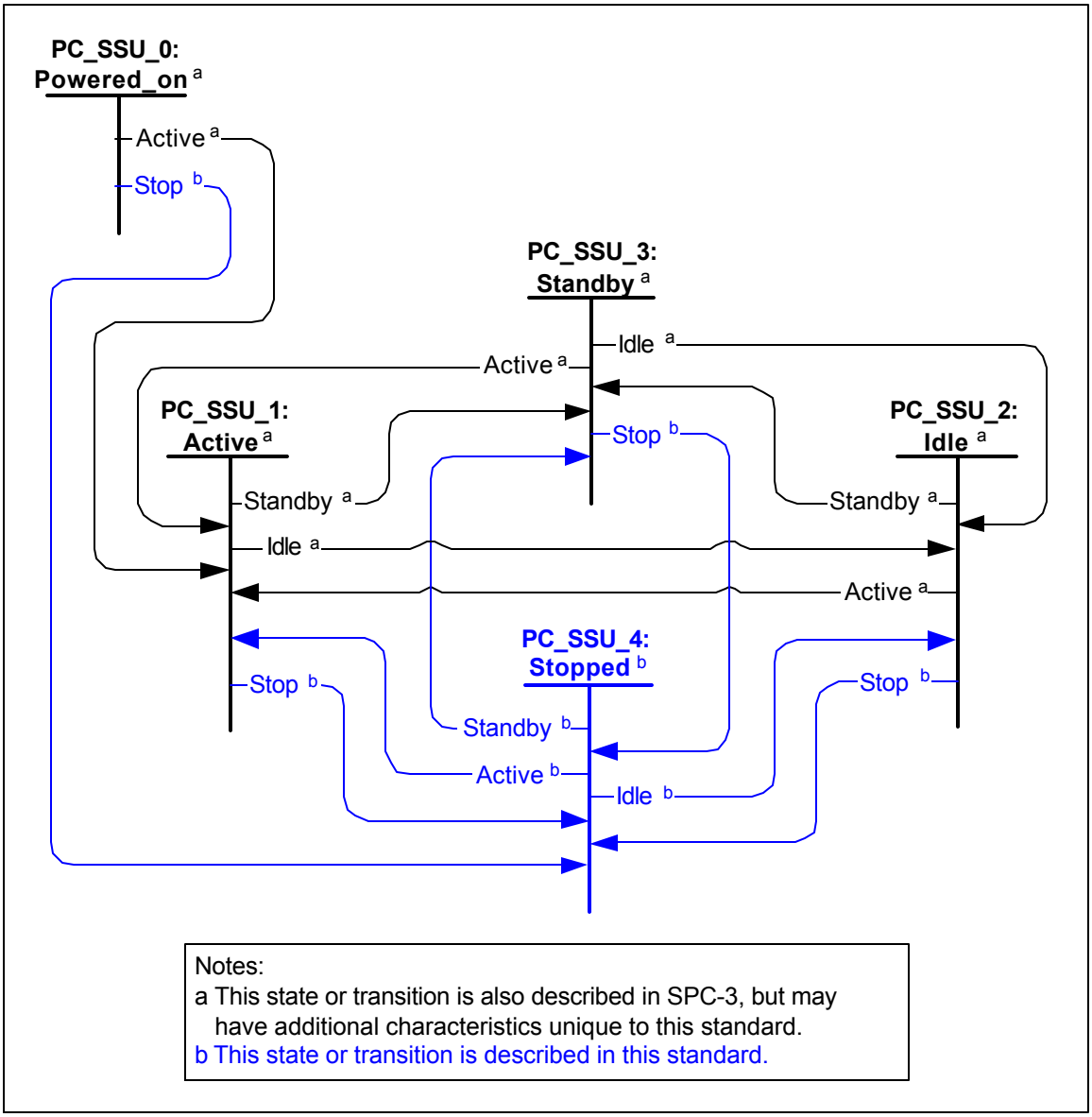

Figure PC_SSU – Power condition state machine for logical units implementing the START STOP UNIT command

5.2.24.2.1 PC_SSU_0:Powered_on state

5.2.24.2.1.1 PC_SSU_0:Powered_on state description

This logical unit shall enter this state upon power on. This state consumes zero time.

5.2.24.2.1.2 Transition PC_SSU_0:Powered_on to PC_SSU_1:Active

This transition shall occur when:

a) the logical unit has no vendor specific or protocol specific method to prevent transition to the PC_SSU_1:Active state.

5.2.24.2.1.2 Transition PC_SSU_0:Powered_on to PC_SSU_4:Stopped

This transition shall occur when:

a) the logical unit has implemented a vendor specific or protocol specific method to prevent transition to the PC_SSU_1:Active state.

5.2.24.2.2 PC_SSU_1:Active state

5.2.24.2.2.1 PC_SSU_1:Active state description

While in this state, if power on initialization is not complete, then:

a) the logical unit completes its power on initialization.

While in this state, if power on initialization is complete, then:

a) the device server is capable of responding to all of its supported commands including media access requests;
b) the logical unit completes processing operations in the shortest time when compared to the time required for completion while in the PC_SSU_2:Idle or PC_SSU_3:Standby states; and
c) the logical unit may consume more power in this state than when in the PC_SSU_2:Idle, PC_SSU_3:Standby, or PC_SSU_4:Stopped states (e.g., a disk drive's spindle motor may be active);
d) if the IDLE bit is set to one, then the idle condition timer is running; and
e) if the STANDBY bit is set to one, then the standby condition timer is running.

5.2.24.2.2.2 Transition PC_SSU_1:Active to PC_SSU_2:Idle

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to 2h (IDLE);
b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to Ah (FORCE_IDLE_0); or
c) the IDLE bit is set to one in the Power Condition mode page, the idle condition timer is not disabled by a START STOP UNIT command, and the idle condition timer is zero.

5.2.24.2.2.3 Transition PC_SSU_1:Active to PC_SSU_3:Standby

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to 3h (STANDBY);
b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to Bh (FORCE_STANDBY_0); or
c) the STANDBY bit is set to one in the Power Condition mode page, the standby condition timer is not disabled by a START STOP UNIT command, and the standby condition timer is zero.

5.2.24.2.2.4 Transition PC_SSU_1:Active to PC_SSU_4:Stopped

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the START bit set to zero and the POWER CONDITION field set to 0h (START_VALID).

5.2.24.2.3 PC_SSU_2:Idle state

5.2.24.2.3.1 PC_SSU_2:Idle state description

While in this state:

a) the device server is capable of responding to all its supported commands including media access requests;
b) the logical unit may take longer to complete processing a command than it would while in the PC_SSU_1:Active state (e.g., the logical unit may have to activate some circuitry before processing a command);
c) the logical unit may consume less power than when in the PC_SSU_1:Active state; and
d) the logical unit may consume more power in this state than when in the PC_SSU_3:Standby or PC_SSU_4:Stopped states (e.g., a disk drive's spindle motor may be active).

5.2.24.2.3.2 Transition PC_SSU_2:Idle to PC_SSU_1:Active

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the START bit set to one;
b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to 1h (IDLE); or
c) the device server receives a command that requires the logical unit to be in the PC_SSU_1:Active state to process the command.

5.2.24.2.3.3 Transition PC_SSU_2:Idle to PC_SSU_3:Standby

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to 3h (STANDBY);
b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to Bh (FORCE_STANDBY_0); or
c) the STANDBY bit is set to one in the Power Condition mode page, the standby condition timer is not disabled by a START STOP UNIT command, and the standby condition timer is zero.

5.2.24.2.3.3 Transition PC_SSU_2:Idle to PC_SSU_4:Stopped

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the START bit set to zero and the POWER CONDITION field set to 0h (START_VALID).

5.2.24.2.4 PC_SSU_3:Standby state

5.2.24.2.4.1 PC_SSU_3:Standby state description

While in this state:

a) the device server is not capable of processing media access commands;
b) the logical unit may consume less power than when in the PC_SSU_1:Active or PC_SSU_2:Idle states (e.g., a disk drive's spindle motor is stopped); and
c) the logical unit may consume more power in this state than when in the PC_SSU_4:Stopped state.

5.2.24.2.4.2 Transition PC_SSU_3:Standby to PC_SSU_1:Active

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the START bit set to one;
b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to 1h (ACTIVE); or
c) the device server receives a command that requires the logical unit to be in the PC_SSU_1:Active state to process the command.

5.2.24.2.4.3 PC_SSU_3:Standby to PC_SSU_2:Idle

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to 2h (IDLE);
b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to Ah (FORCE_IDLE_0); or
c) the device server receives a command that requires the logical unit to be in the PC_SSU_2:Idle state to process the command.

5.2.24.2.4.3 PC_SSU_3:Standby to PC_SSU_4:Stopped

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the START bit set to zero and the POWER CONDITION field set to 0h (START_VALID).

5.2.24.2.5 PC_SSU_4:Stopped state

5.2.24.2.5.1 PC_SSU_4:Stopped state description

While in this state:

a) the device server is not capable of processing media access commands; and
b) the logical unit may consume less power than when in the PC_SSU_1:Active, PC_SSU_2:Idle, or PC_SSU_3:Standby states.

5.2.24.2.5.2 Transition PC_SSU_4:Stopped to PC_SSU_1:Active

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the START bit set to one and the POWER CONDITION field set to 0h (START_VALID); or
b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to 1h (ACTIVE).

5.2.24.2.5.2 Transition PC_SSU_4:Stopped to PC_SSU_2:Idle

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to 2h (IDLE); or
b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to Ah (FORCE_IDLE_0).

5.2.24.2.5.2 Transition PC_SSU_4:Stopped to PC_SSU_3:Standby

This transition shall occur when:

a) the device server receives a START STOP UNIT command with the POWER CONDITION field set to 3h (STANDBY); or
b) the device server receives a START STOP UNIT command with the POWER CONDITION field set to Bh (FORCE_STANDBY_0).