

Oct.26, 2002

To: T10 Technical Committee

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Subject: SAS Bit Ordering Diagrams Change Proposal

Revision History:

Revision 2: Modified diagrams as requested during SAS Meeting in Las Vegas on 10-24-02.

Revision 1: Modified proposed diagrams as requested during SAS Protocol WG Conference Call on 10-22-02. Also modified STP diagrams to swap the byte order and remove the byte transpose blocks which were shown.

Overview

Figures 35 and 36 in sas-r02a show bit transposition logic required *prior* to 8b/10b encoding and *after* 10b/8b decoding. While bit transposition within a byte is actually required for 8b/10b encoding and decoding as defined by the original 8b/10b encoding patent, the bit transposition is done *inside of* the 8b/10b encoder and 10b/8b decoder, *not outside of* the them, as depicted in the current figures. This document proposes a modification to Figures 35 and 36 in order to better correlate them to Tables 22 and 24, as well as to show that one does not have to perform a bit transposition on an 8-bit value prior to looking up the associated 10b encoding in Table 24.

Three figures in sas-r02a are incorrectly lacking bit transposition logic and/or bit inversion logic associated with SAS CRC functionality.

Additionally, in order to provide clarity for the distinction between SSP, SMP, and STP CRC generation and checking requirements, this document proposes the inclusion of three new figures that indicate the byte ordering, bit ordering, and CRC requirements for STP transmit and receive data paths.

Proposed Changes to sas-r02a Specification:

1) Figures 35 and 36 show bit transposition being done within each byte of a dword outside of the 8b/10 encoding/decoding logic. Propose that these diagrams get replaced with the following diagrams:

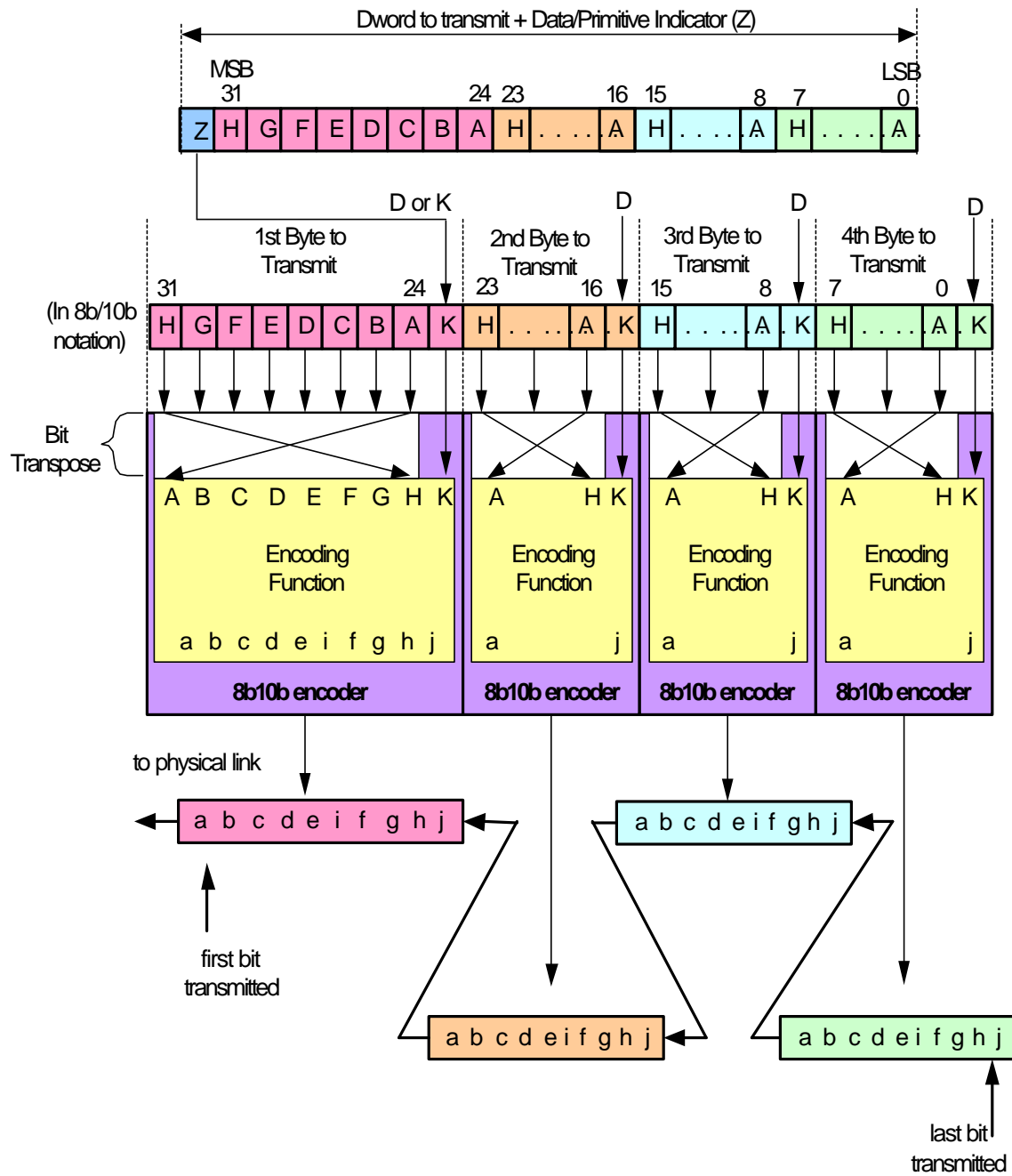


Figure 35 – SAS bit transmission logic

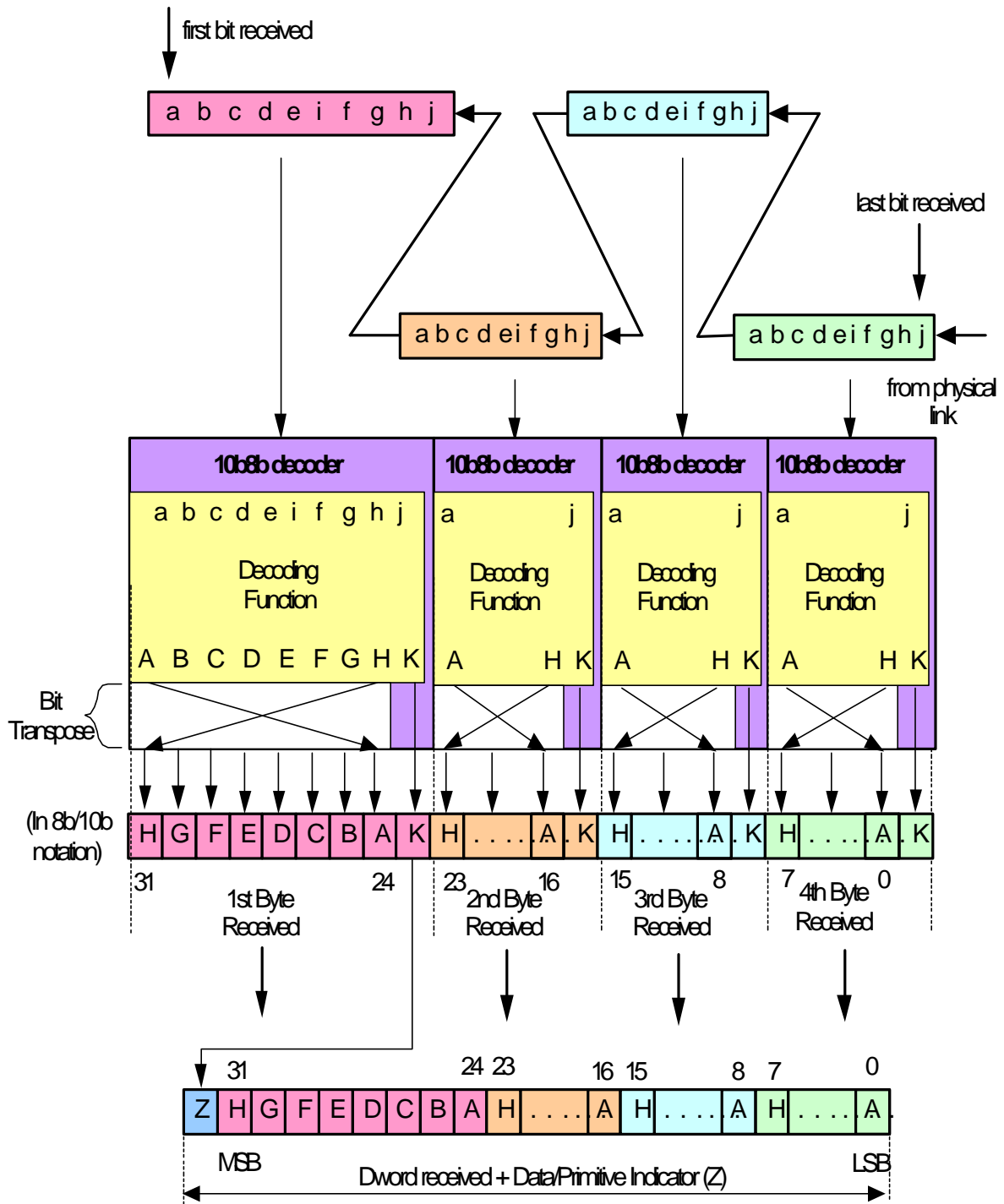


Figure 36 – SAS bit reception logic

2) Figure 55 is missing bit inversion at the output of the CRC generator. Propose to replace with the following figure which shows the outputs being inverted, and shows the bit ordering within each byte:

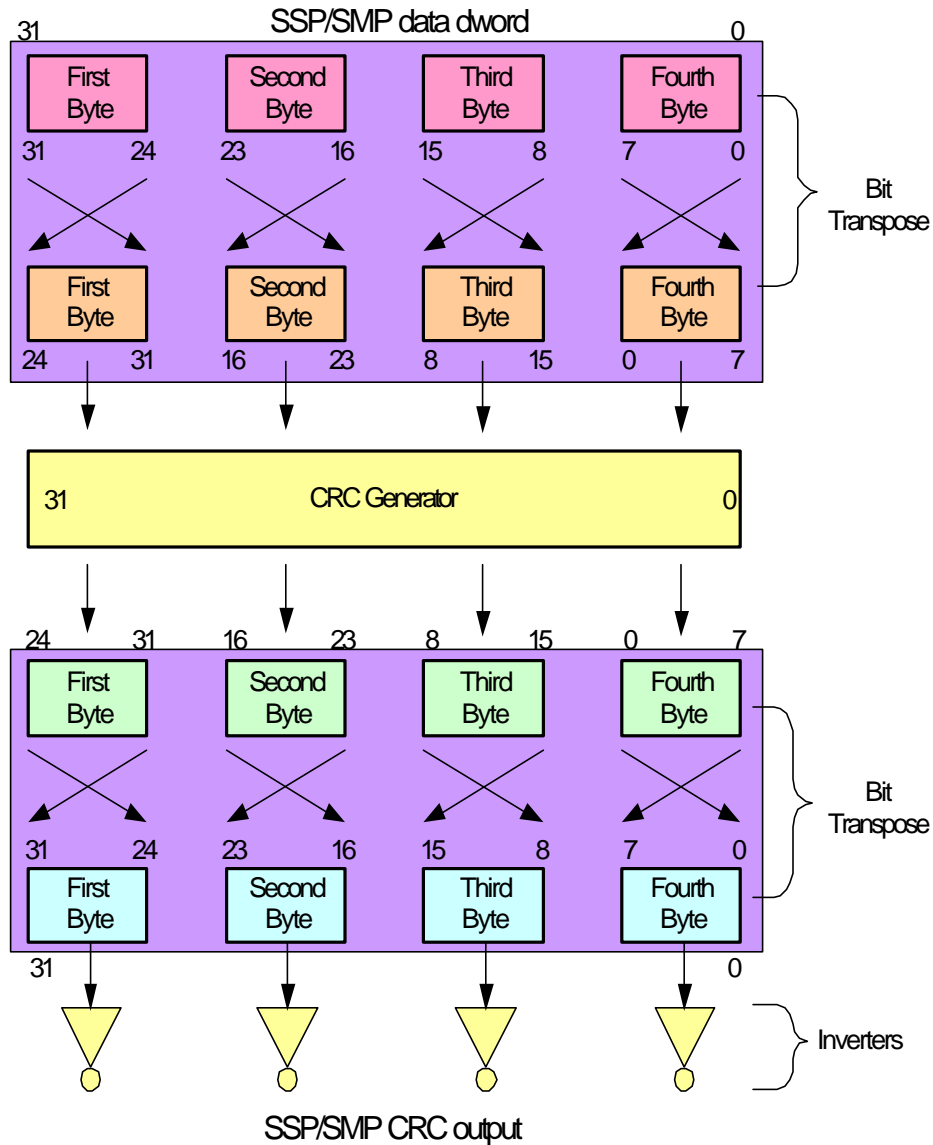


Figure 55 – SSP/SMP CRC generator/checker byte and bit order

3) Figures 56 and 57 do not show the bit transposition and inversion logic associated with the SSP/SMP CRC generator/checker. Propose to replace with the following figures:

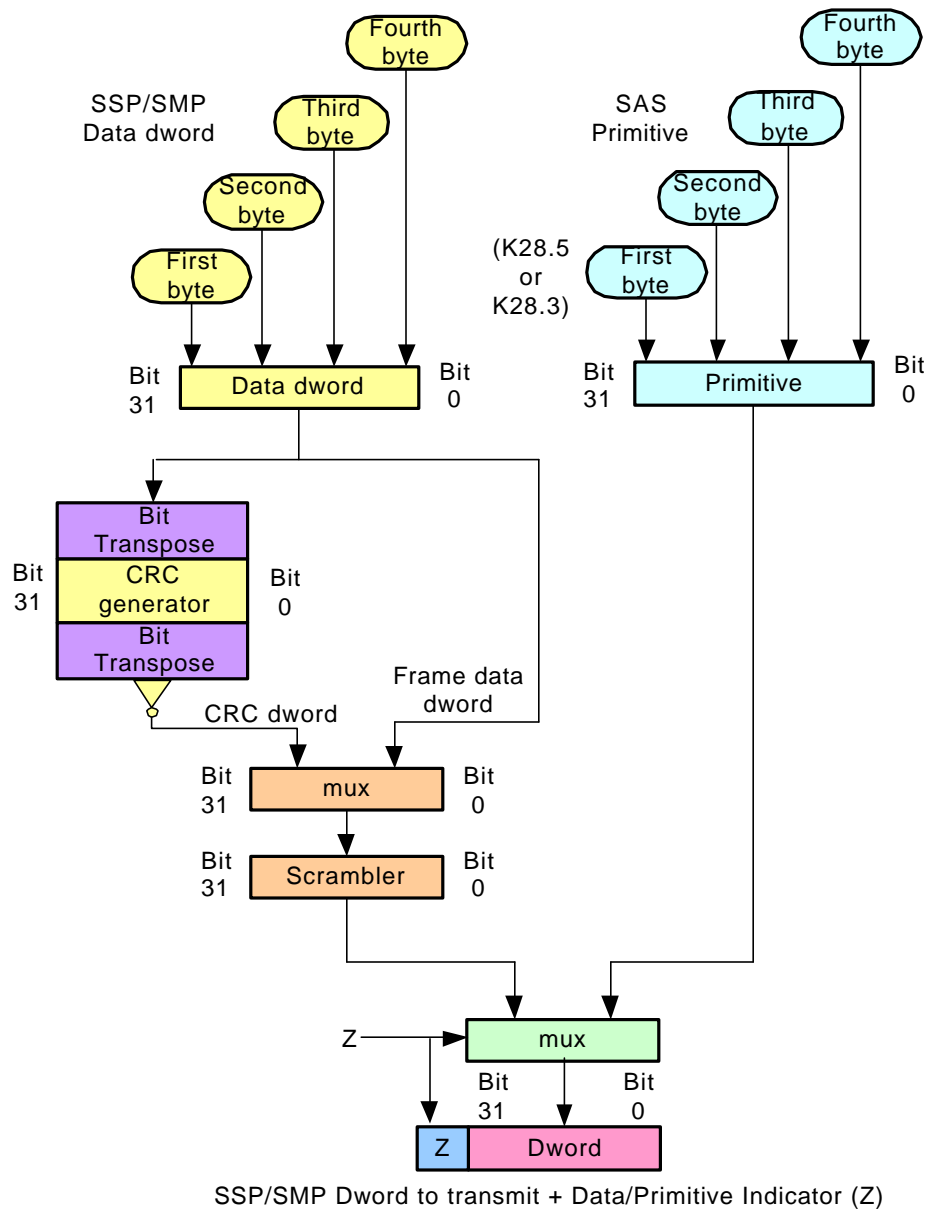


Figure 56 – SSP/SMP Transmit path byte and bit ordering

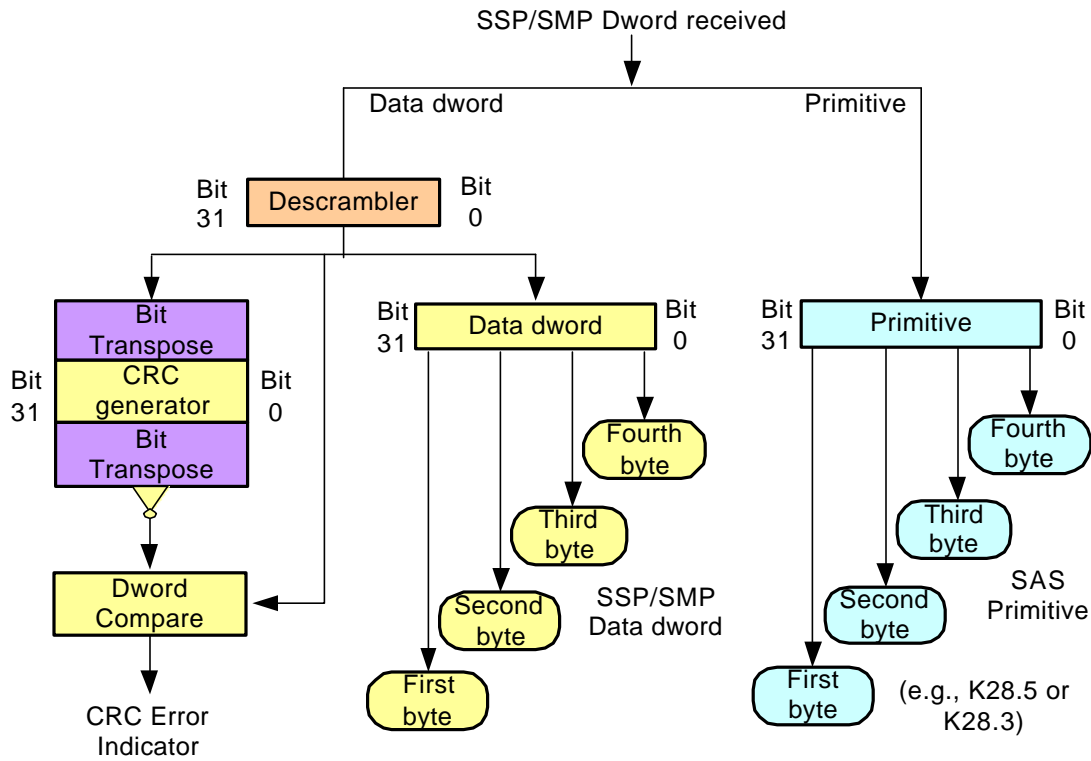


Figure 57 – SSP/SMP Receive path byte and bit ordering

4) Propose that three diagrams be added *to the Appendix* to clarify the byte ordering for STP data paths and the difference between SSP, SMP and STP CRC requirements.

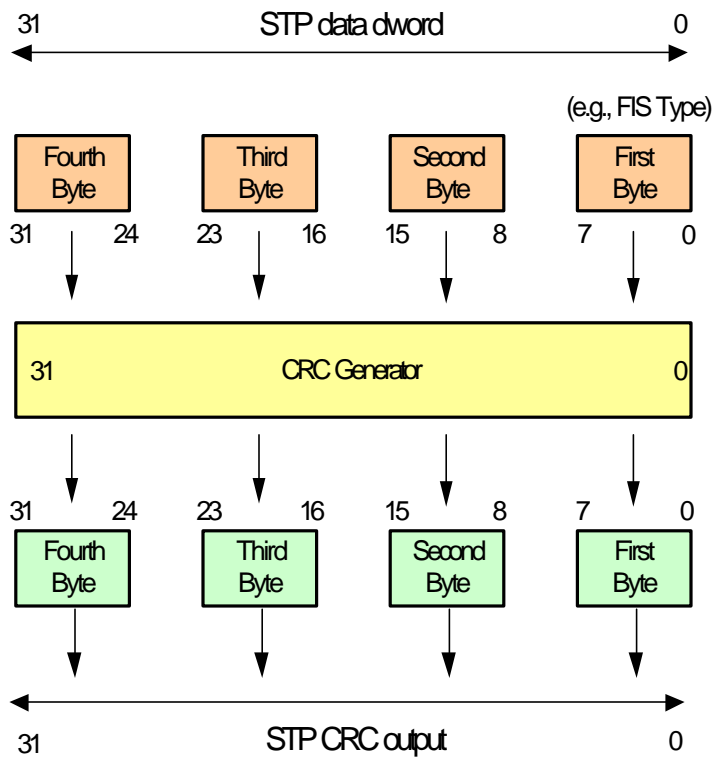


Figure XX - STP CRC generator/checker byte and bit ordering

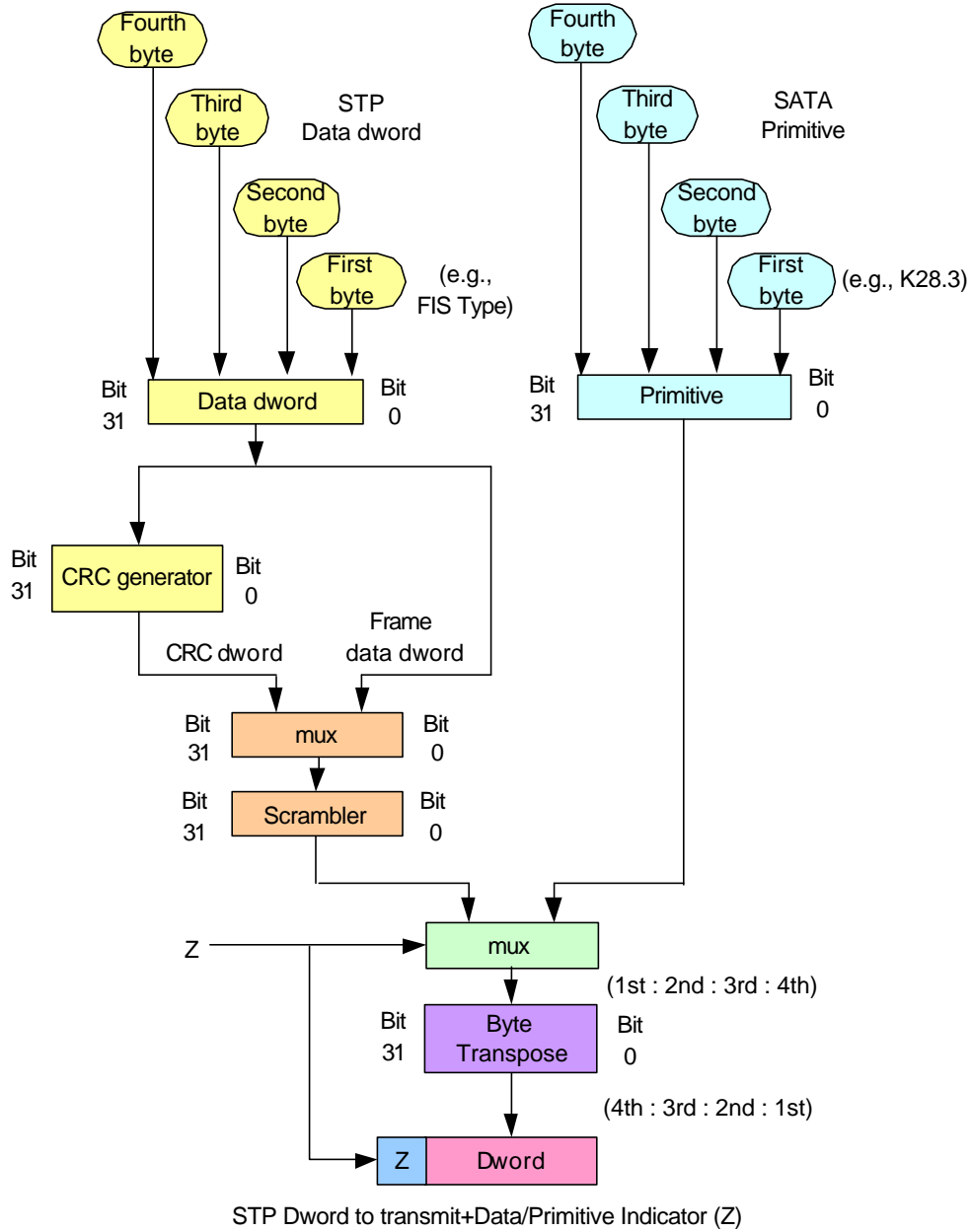


Figure XX – STP Transmit path byte and bit ordering

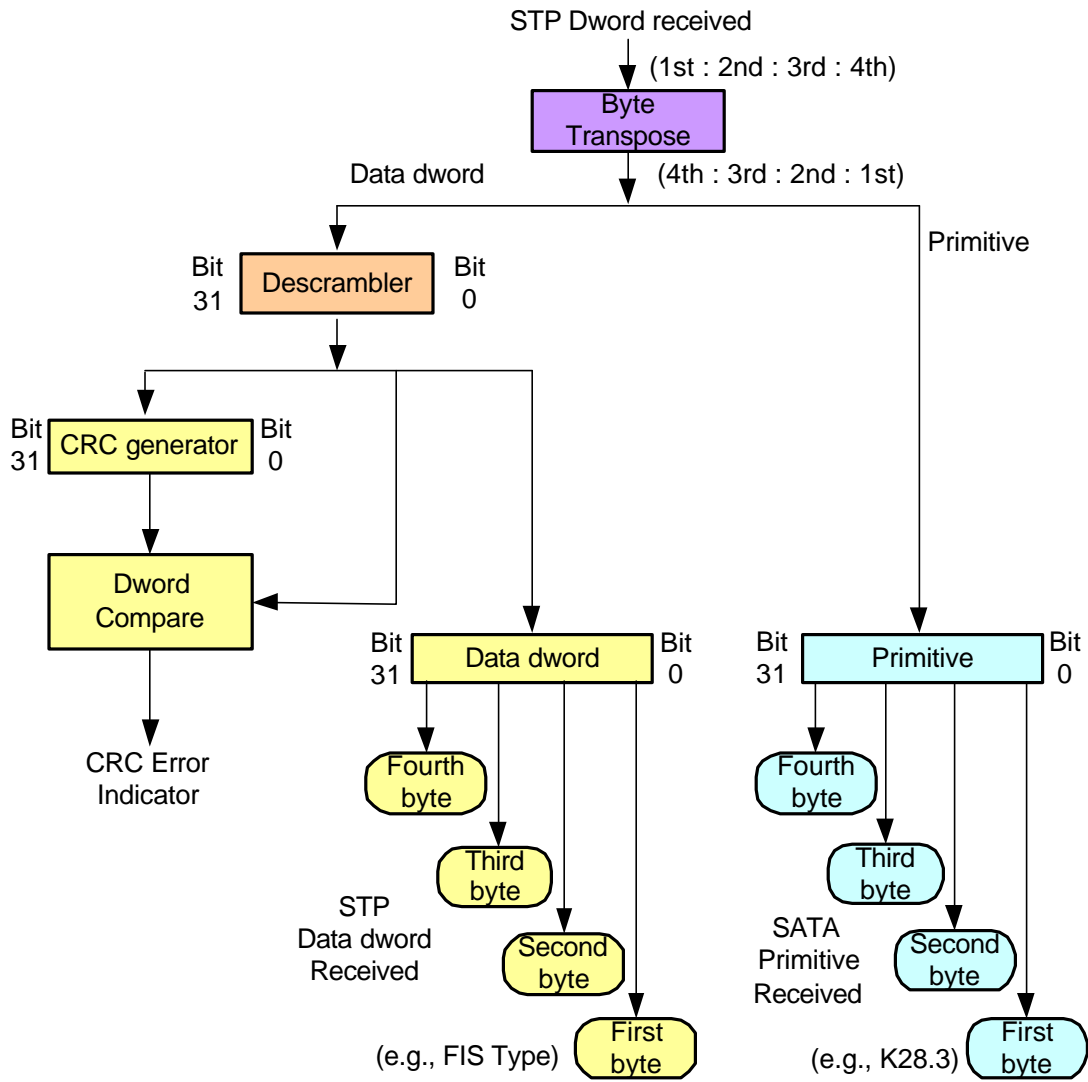


Figure XX – STP Receive path byte and bit ordering