Date: October 30, 2002
To: T10 Technical Committee
From: Alvin Cox (alvin.cox@seagate.com)
Subject: SAS Test Loads

The following changes to text and test load figure are made to aid the testing process by clarifying and defining the compliance channel test load and zero-length test load. The changes to the rev 0 version are significant and not highlighted in an effort to make this version more readable. Revision 2 adds a statement explaining the purpose of compliance channel testing.

5.7.11 ~~Driver~~ Transmitter characteristics

Compliance channel testing for the verification transmitter characteristics is the primary test methodology promoted by this specification. This test methodology verifies the delivered signal at the receiver rather than the actual output at the transmitter. For valid test of the transmitter, the output characteristics of the transmitter must be run at the same settings (pre-emphasis, voltage swing, etc.) with both the zero-length test load and the compliance channel test load and meet the received signal specifications under each of these loading conditions. Alternately, transmitter characteristics are listed in a separate table to support traditional test methodology.

For all inter-enclosure TxRx connections, the output shall be A. C. coupled to the cable through a transmission network.

For intra-enclosure TxRx connections the expander shall be A. C. coupled to the media. Other drivers may be A. C. or D. C. coupled.

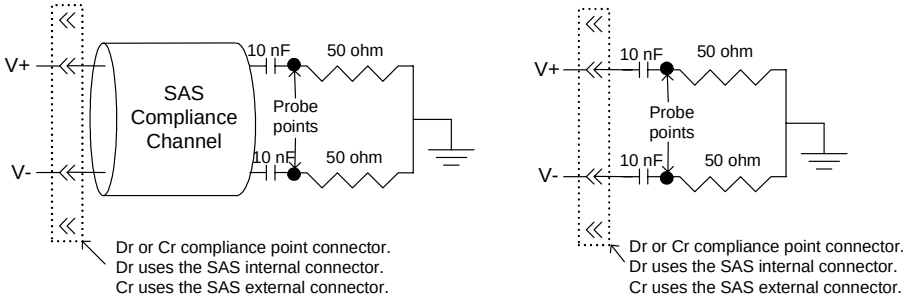
The driver shall have the output voltages and timing listed in table **~~24~~ 25** and table 26 measured at the designated interoperability points. The default **mask** is **Cr** for inter-cabinet TxRx connections and **Dr** for intra-cabinet TxRx connections. The measurements shall be made across a load equivalent to **the zero-length load ~~that~~** shown in figure 39 **unless otherwise specified**.

The driver shall also meet the output voltages and timing listed in table 25 and table 26 at the designated interoperability points. The default mask is Cr for inter-cabinet TxRx connections and Dr for the intra-cabinet TxRx connections. The measurements shall be made across a load equivalent to the compliance channel test load shown if figure 39 unless otherwise specified. The transmission magnitude response, [S_{21}], of the compliance channel in dB satisfies the following equation:

$$|S_{21}| \leq -20 \log (e) \{[6.5 \times 10^{-6}(f^{0.5})]+[2.0 \times 10^{-10}(f)]+[3.3 \times 10^{-20}(f^{2})]\} \text{ dB}$$

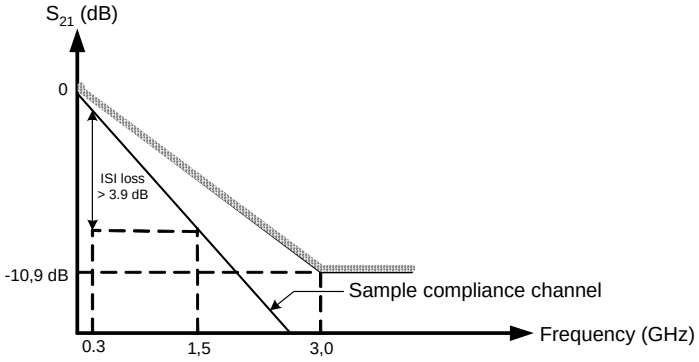
A compliance channel magnitude response and ISI loss example for 3 Gbps is shown in figure 39.

The eye masks are shown in 5.7.4. **~~The normalized amplitudes, Y1 and Y2, allow signal undershoots. The driver shall meet both the normalized and absolute values.~~**



Compliance channel test load

Zero-length test load



Compliance channel magnitude response and ISI loss example for 3,0 Gbps

Figure 39 — ~~Test~~ Transmitter test loads

5.7.12 Receiver characteristics

The receiver shall be A. C. coupled to the media through a receive network. The receive network shall terminate the TxRx connection by a 100 ohm equivalent impedance as specified in table 28.

The receiver shall operate within a BER of 10^{-12} when a SAS signal with valid voltage and timing characteristics is delivered to the interoperability point from a 100 ohm source. The delivered SAS signal shall be considered valid if it meets the voltage and timing limits specified in **table 25 and** table 26 ~~**when measured across a load equivalent to those of figure 39**~~.

Additionally the receiver shall also operate within the BER objective when the signal at a receiving phy has the additional sinusoidal jitter present that is specified in the table 27. Jitter tolerance figures are given in 5.7.4.4 for all interoperability points in a TxRx connection. The figures given assume that any external interference occurs prior to the point at which the test is applied. When testing the jitter tolerance capability of a receiver the additional 0,1 UI of sinusoidal jitter may be reduced by an amount proportional to the actual externally induced interference between the application point of the test and the input to the receiving phy. The addition of additional jitter reduces the eye opening in both voltage and time; see the Jitter tolerance masks in 5.7.8.