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To: **T10 Serial Attached SCSI PHY Working Group**
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Subject: SAS driver and receiver electrical characteristics additions

Introduction

This proposal adds common mode specifications to define differential signal balance, defines common mode transients during mode changes and hot plug events, and defines a receiver common mode tolerance (i.e., rejection) requirement. Revision 2 incorporates changes from SAS PHY working group discussions, changes "common mode transients" to "transients" to be more general, and replaces the common mode signal component requirement with a transmitter balance requirement. Table and other references are to SAS-r02b. Revision 3 of this proposal corrects minor editorial errors that were in revision 2. Revision 4 includes a change to the Table 23 entry for Physical link rate tolerance at XR to match that in SATA errata 030.

Table 23. General interface characteristics

Add the following to Table 23:

a) a maximum AC coupling capacitor value and limits on transients during mode change events (these additions, combined with the impedance specifications, define the design requirements for the hot-plug / mode change transient stress problem);
b) receiver common mode voltage and frequency tolerance specifications;
c) notes at the bottom of the table for clarification of a) and b).
d) Change the Physical link rate tolerance at XR value to match SATA errata 030

Characteristic	Units	1,5 Gbps	3,0 Gbps
.....			
Physical link rate tolerance at XR [b]	ppm	+350 / -5 350	+350 / -5 350
AC coupling capacitor [c]	nF	12 max	12 max
Transmitter transients [d]	V	+/- 1,2 max	+/- 1,2 max
Receiver transients [d]	V	+/- 1,2 max	+/- 1,2 max
Receiver AC common mode voltage tolerance V_{cm} [e]	mV p-p	150 min	150 min
Receiver AC common mode frequency tolerance range F_{cm} [e]	MHz	2 - 200	2 - 200

Notes: ..... [c] The coupling capacitor value for AC coupled transmit and receive pairs. [d] The maximum transmitter and receiver transients are measured at nodes V_P and V_N on the test loads shown in figures xxa (for the transmitter) and xxb (for the receiver) during all power state and mode transitions. Test conditions shall include the system power supply ramping at the fastest possible power ramp (up and down). [e] Receivers must tolerate sinusoidal common mode noise components within the peak-to-peak amplitude (V_{cm}) and the frequency range (F_{cm}).

Add the following figures after the table:

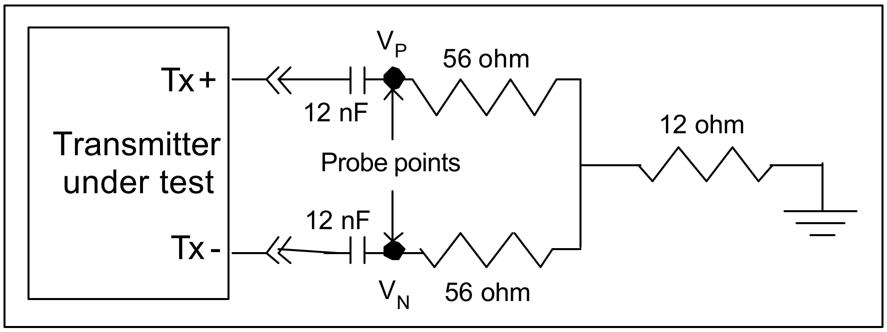

Figure xxa. Transmitter transient test circuit

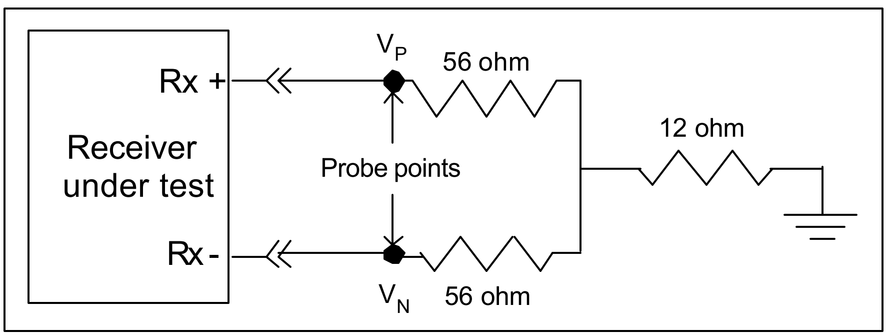

Figure xxb. Receiver transient test circuit

Table 24. Transmitted signal characteristics at Tx compliance points

Add a specification for transmitter imbalance and a note into the table (see below).

Discussion:

There are two main common mode components in the transmitted signal, skew and driver imbalance.

For skew: if we assume linear ramps, the peak common mode transient due to skew between the T+ and T- signals is given by:

$$V_{cm}\ pk = 0.25 * (t_{skew} / t_{rise}) * V_{dpp}$$

With maximum skews, minimum rise times, and maximum V_{pp} differential levels as in table 24, we get:

for Dt: V_{cm} pk = 45 mV @ 1,5 Gbps, and 60 mV @ 1,5 Gbps for Ct: V_{cm} pk = 60 mV @ 1,5 Gbps, and 60 mV @ 1,5 Gbps

The specification for skew in the table already handles this component.

Driver imbalance contributes another common mode term, which shows up as a difference in common mode levels between the logic 1 and logic 0 output states.

For a T+ driver peak-to-peak swing of V_p, and a T- driver pk-pk swing of V_m, the peak-to-peak driver imbalance common mode term is:

$$V_{cm} \text{ pk-pk} = (V_p - V_m) / 2$$

For 1600 mV pk-pk differential, V_p and V_m would be 800 mV pk-pk nominal. A 5% mismatch [is this a reasonable value?] between V_p and V_m give V_p - V_m = 40 mV, and a common mode term of V_{cm} = 20 mV pk-pk. This is small when compared to the skew term.

We propose that:

a) we let the skew spec handle the common mode transient at data transitions;
b) we withdraw the proposed maximum common mode signal component specification; and
c) add a specification for maximum transmitter output imbalance to table 24 (as follows).

Add the following to the Dt, Ct, Xt, and It rows for a specification for transmitter signal balance at the transmitter output:

Compliance Point	Signal Characteristic	Units	SATA 1.0	1.5 Gbps	3.0 Gbps
.....					
	Maximum transmitter output imbalance [j]	%		10	10
.....					

Notes:
.....
[j] The maximum difference between the V+ and V- AC RMS transmitter amplitudes measured on a CJTPAT test pattern into the test load in Figure 33, as a percentage of the average of the V+ and V- AC RMS amplitudes.

5.7.12 Receiver characteristics

Add a common mode rejection requirement in the third paragraph of the subclause (the change is underlined):

Additionally the receiver shall also operate within the BER objective when the signal at a receiving phy has the additional sinusoidal jitter present that is specified in the Table 27 and the common mode signal V_{cm} over frequency range F_{cm} as is specified in Table 23. Jitter tolerance figures are given in 5.7.4.4 for all interoperability points in a TxRx connection. The figures given assume that any external interference occurs prior to the point at which the test is applied. When testing the jitter tolerance capability of a receiver the additional 0,1 UI of sinusoidal jitter may be reduced by an amount proportional to the actual externally induced interference between the application point of the test and the input to the receiving phy. The addition of additional jitter reduces the eye opening in both voltage and time (see the jitter tolerance masks in 5.7.8).