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To: **T10 Parallel SCSI Working Group**
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Subject: Proposed modifications to SPI-5 timing clause

Introduction

The following proposes some minor corrections and clarifications for SPI-5, clause 9. Also included is a reorganization of the timing budget templates (tables 39 and 40) to more clearly indicate the fast-160 and fast-320 transmitter and receiver timing error terms and to separately identify the remaining timing budget available for crosstalk, ISI and reflection errors in the cable plant. Clause number and other references in this proposal are to SPI-5, revision 2.

De-skewed data valid window:

a) Rename this to be "Receiver de-skewed data valid window" in table 36 and 9.2.11 to make it clear that this is a receiver performance parameter and not a system number.

b) Change the equation in 9.2.11:

from: ± [(data transfer period) - (residual skew error) - (strobe offset tolerance) - (clock jitter) - (receiver amplitude skew) - (chip noise) - (system noise at receiver) - (receiver asymmetry)] / 2

to: ± [(data transfer period) - (residual skew error) - (strobe offset tolerance) - (receiver asymmetry) - (chip noise at receiver) - (system noise at receiver)] / 2

because: 1) Clock jitter is a transmitter error term and should not be in the receiver de-skewed data valid window budget; and, 2) receiver amplitude skew should not be included because the test signal for receiver de-skewed data valid window is a repeated 101010 pattern with no bit-to-bit amplitude variation

c) With the above definition, the value for receiver de-skewed data valid window for fast-320 in table 36 should be:

± [3.125 - 0.2 - 0.2 - 0 - 0.2 - 0.2] / 2 = ± 1,1625 ns
we recommend using ± 1,1 ns

Crosstalk:

a) Rename this to be “Crosstalk time shift” to be more clear about what it is.

b) Add a new definition as 9.2.x: “Crosstalk time shift: The peak-to-peak time shift error on DB(0-15), P_CRCA, or DB(P1) caused by transitions on all other DB(0-15), P_CRCA, and DB(P1) signals.”

Tables 39 and 40:

We propose combining the present tables 39 and 40 and separating the transmitter and receiver error budgets from the interconnect (cable / backplane) error budgets. This separation makes sense because the transmitter and receiver error budgets are fixed by the host, expander, and target designs, and most available (and reasonable) steps have already been taken in these designs to reduce and control these errors. The remaining error budget, [transfer period - total (transmitter + receiver) errors], is the system budget remaining for the interconnect.

In some fast-320 systems, e.g., with twisted-flat cable, crosstalk can be the dominant error. In others, e.g., with shielded round cable, ISI can dominate. By defining an “Interconnect timing error budget”, the standard could specify larger maximum crosstalk and ISI errors, and leave it to the system designers to ensure that individual system crosstalk plus residual ISI meets the interconnect timing error budget.

Table x – SCSI fast-160 and fast-320 timing budget template

Item	Location	Fast-160		Fast-320		Comments
Nominals:						
REQ(ACK) period		12,5 ns		6,25 ns		
Transfer period		6,25 ns		3,125 ns		
Transmitter and receiver errors:		**Total Errors**	**Post-Compensation**	**Total Errors**	**Post-Compensation**	**Worst case total of + and - time shift unless otherwise noted**
REQ(ACK) period tolerance / 2	A	0,06 ns	0,06 ns	0,06 ns	0,06 ns	
Transmit chip skew	A	0,75 ns		0,75 ns		
Receive chip skew	G	0,75 ns		0,75 ns		
Transmitter + Receiver trace skew	B,D	0,4 ns		0,4 ns		
Transmit time asymmetry	A	0,5 ns	0,5 ns	0,5 ns		
Receive time asymmetry	G	0,35 ns	0,35 ns	0,35 ns		
Residual skew error	F		0,3 ns		0,2 ns	
Strobe offset tolerance	F		0,5 ns		0,2 ns	
Clock jitter	A	0,25 ns	0,25 ns	0,25 ns	0,25 ns	
System noise at Transmitter	B	0,25 ns	0,25 ns	0,2 ns	0,2 ns	
System noise at Receiver	G	0,25 ns	0,25 ns	0,2 ns	0,2 ns	
Chip noise at Receiver	G	0,2 ns	0,2 ns	0,2 ns	0,2 ns	
Offset induced time asymmetry	G	N/A	N/A	0,8 ns	0,2 ns	Previously ignored for Fast-160
Receiver Amplitude time skew	G	0,2 ns	0,2 ns	0,2 ns	0,05 ns	
Total transmitter + receiver error budget		**3,96 ns**	**2,86 ns**	**4,66 ns**	**1,56 ns**	
Total timing error budget for interconnect and system margin		**2,29 ns**	**3,39 ns**	**-1,535 ns**	**1,565 ns**	Transfer period - (Total transmitter + receiver error budget)

Note to Table x:

The interconnect timing budget error terms are:

a) Cable skew (the value for this is 2,5 ns max, see 9.2.8): this error is fully corrected by receiver deskew circuitry, and the residual deskew error is already included in the receiver error budget;
b) Crosstalk time shift: this error is uncorrectable; and,
c) Intersymbol Interference (ISI): this error is 50% corrected for fast-160, and 75% corrected for fast-320.

The total timing error budget for interconnect and system margin minus the sum of crosstalk time shift and residual (post-compensation) ISI, gives the remaining system timing margin (e.g., for setup and hold at the receiver).

Example timing budget for fast-160 (post-compensation):

Total timing error budget for interconnect and system margin:	3,39 ns
- Crosstalk time shift	- 0,7 ns
(ISI before compensation)	(4 ns)
- ISI after compensation	- 2 ns
Remaining system timing margin	**0,69 ns**

Example timing budget for fast-320 (post-compensation):

Total timing error budget for interconnect and system margin:	1,565 ns
- Crosstalk time shift	- 0,5 ns
(ISI before compensation)	(4 ns)
- ISI after compensation	- 1 ns
Remaining system timing margin	**0,065 ns**