Test Pattern Comparison - FC, XAUI, SATA

The purpose of this document is to aid and promote the discussion of test patterns to be specified for SAS compliance testing. To that end, the tables below present a comparison of the test patterns specified for Fibre Channel, XAUI, and SATA.

A "non-compliant" pattern is a bit sequence that does not represent a valid protocol frame (but usually complies with the coding rules for running disparity). A "compliant pattern" is a valid protocol frame (SOF, payload, CRC, EOF) usually containing the actual test pattern as the payload. When a non-compliant pattern is encapsulated in a protocol frame for it to be used as a compliant pattern care must be taken in the pattern selection to ensure that the pattern structure remains the same in both running disparities.

High Level Comparison

FC (MJSQ Rev 6.0)	XAUI	SATA 1.0
Defines compliant patterns and non-compliant patterns. Does not explicitely say what pattern(s) to use for compliance test. Proposes RPAT/CRPAT for TX jitter measurements, and RPAT/CRPAT and JTPAT/CJTPAT for RX jitter tolerance measurements. "Composite patterns should be used for compliance testing." "For compliance testing of a particular device, the pattern(s) that produce(s) the worst case output or tolerance results shall be used."	Defines compliant patterns and non-compliant patterns. CJPAT (similar FC CJTPAT) is explicitely specified for RX jitter tolerance testing. However, it is also used for TX jitter measurements. Other patterns are explicitely specified as "not intended for jitter compliance testing".	Defines four different patterns which are essentially the same as the non-compliant FC patterns. All patterns are to be used individually as non-compliant patterns for jitter measurements and verifying electrical parameters, and both individually and as a composite pattern for frame error rate testing and in-system test. Also mentions random data patterns to be used for jitter output and BER measurements and as baseline patterns for comparative testing, but does not specify the pattern(s).

Comparison by Pattern

Pattern Type	Properties (per the specs)	TX / RX	FC (MJSQ Rev 6.0)	XAUI	SATA 1.0
Synchronous Switching Output (SSO) Pattern	Repeating D3132 Generates power supply noise through maximum simultaneous switching of the 10B parallel interface	RX	SPAT, CSPAT	n/a	Same pattern as FC SPAT
Low Transition Density Pattern	Repeating D30.3 Longest runs of 1s and 0s compliant with the 8B/10B code rules. Generates jitter due to ISI and tests PLL tracking.	TX, RX	Used in non-compliant form and as part of the CJTPAT.	n/a (XAUI low frequency pattern is a more extreme case of this pattern)	Essentially same pattern as FC
High Transition Density Pattern	Half-rate & quarter-rate clock. (D21.5, D24.3, D10.2, D25.6/6.1, D6.1/25.6) Generates high frequency jitter due to ISI and tests transition time asymmetries.	TX	Alternating half-rate and quarter-rate pattern Used in non-compliant form and as part of the CJTPAT.	High Frequency Test Pattern uses only half-rate clock (D21.5) Only used in non-compliant form (to test random jitter).	Essentially same pattern as FC
Low Frequency Spectral Contents Pattern	Repeating D11.5, D20.2 Contains low frequency spectral components. Tests input high-pass filter circuitry.	RX	Only used in non-compliant form.	n/a	Essentially same pattern as FC
Ten runs of 3	D7.7, D28.3, ... ?	TX	Only used in non-compliant form.	n/a	n/a
Composite pattern	Combines the above patterns in alternating sequences for maximum TX, RX stress.	TX, RX	Unspecified combinations of non-compliant FC patterns suggested for compliance testing.	n/a	SATA Composite Pattern consists of specified combinations of all of the individual SATA patterns. Only used in compliant form.
Random Pattern	Flat signal spectrum without peaks makes it possible to isolate spectral peaks in the TX jitter	TX, RX	RPAT, CRPAT Specifically developed for FC TX testing	CRPAT (Continuous Random Pattern) Essentially same as FC CRPAT.	n/a SATA also suggests to use random pattern for jitter output and tolerance testing, without specifying or strictly requiring it.
Jitter Tolerance Pattern	Alternating Low Transition Density Pattern and High Transition Density Pattern. Stresses receiver by exposing it to extreme phase jumps	RX	JTPAT, CJTPAT	CJPAT (Continuous Jitter Test Pattern) Modified from the FC CJTPAT to incorporate the low- and high density segments in both running disparities.	n/a (but the SATA Composite Pattern follows the same idea)

Low frequency Pattern	Repeating K28.7. (Continuous longest run square wave of five 1s, five 0s) Pattern does not contain DJ (ideally!) and therefore allows to measure RJ. MJSQ describes this approach as "flawed" because possible sub-harmonic deterministic processes in the TX might falsely be interpreted as RJ.	TX, RX	n/a in MJSQ (spec'd in FC-PH for RJ measurement)	To test low frequency RJ and PLL tracking	n/a
Mixed frequency Pattern	Repeating K28.5. Fast switching between low frequency and high frequency (contains both the longest (5) and shortest (1) runs of bits). A favorite pattern of some folks. MJSQ describes this pattern as inadequate because it can miss to expose jitter caused by subharmonic processes and possible mistiming on the edges not present in the long bit run segments.	TX	n/a in MJSQ (spec'd in FC-PH for DJ measurement)	To test RJ and DJ due to high frequency ISI.	n/a