The following is an edited version of section 5 from SAS-r00e. Changes included reflect the input to this section agreed upon by the SAS PHY Working group and are found in the following T10 documents: 02-183r0, 02-210r2, 02-229r0, 02-243r0, 02-265r0, 02-288r0

Changes are in red with yellow highlighting. The data agreed upon is in black with turquoise highlighting. The turquoise highlights are not to be included in the text update.

5 Physical layer

5.1 SATA cables and connectors

Figure 22 shows the cables and connectors defined by SATA (for reference). A “SATA host” is equivalent to a SAS initiator device; a “SATA device” is equivalent to a SAS target device.

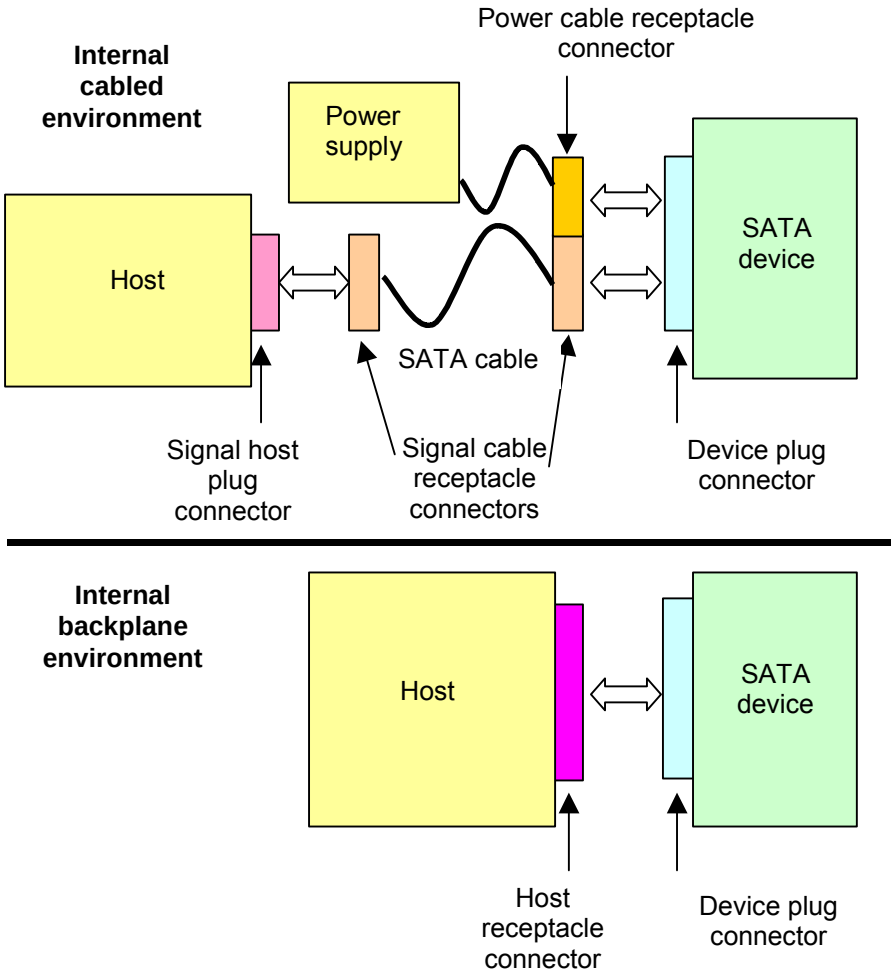

Figure 22. SATA cables and connectors (reference)

5.2 SAS cables and connectors

This standard supports internal cable and internal backplane environments.

Figure 23 shows the cables and connectors defined in this standard to support an external environment.

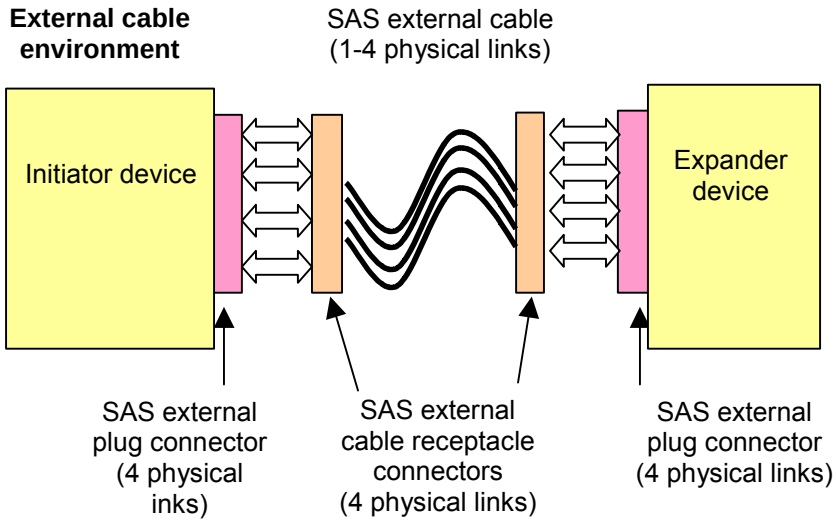

Figure 23. SAS cables and connectors - external environment

Figure shows the connectors defined by this standard for internal environments.

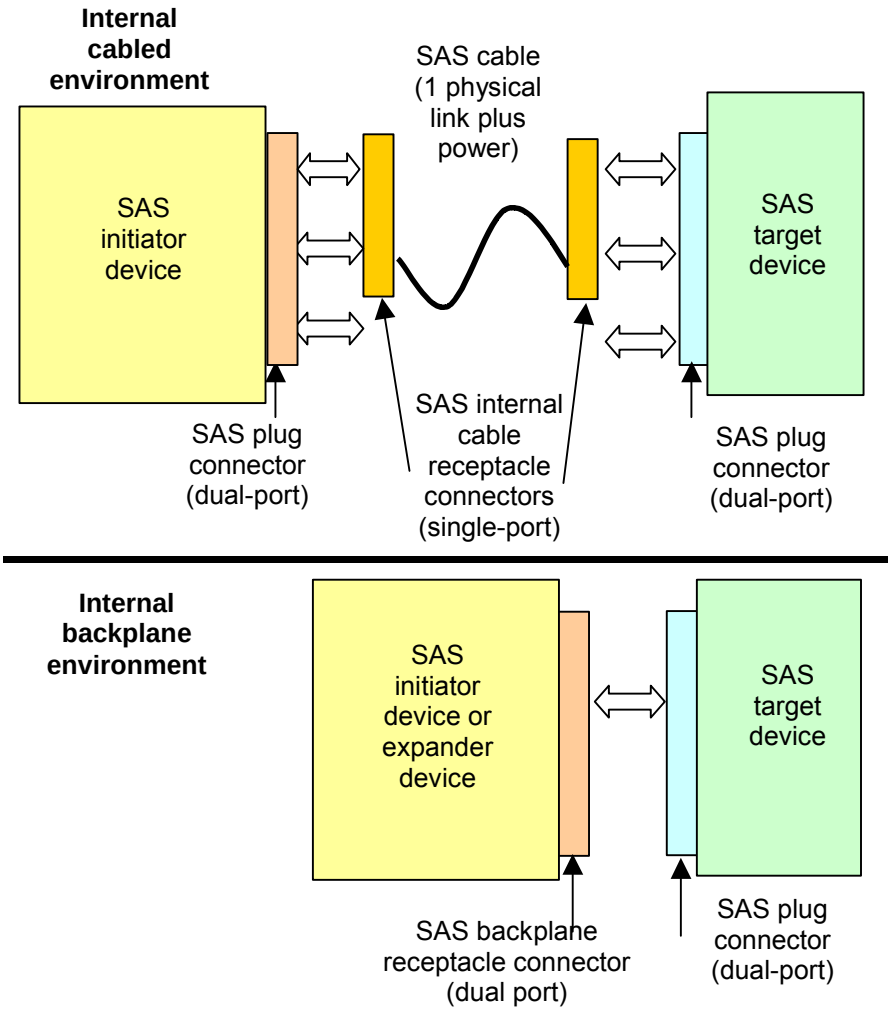

Figure 24. SAS connectors - internal environment

Table 7 summarizes the connectors defined by this standard.

Table 7. Connectors

Type of connector	Reference	Attaches to	Reference
SAS plug	5.3.2	SAS internal cable receptacle	5.3.3
		SAS backplane receptacle	5.3.4
SAS internal cable receptacle	5.3.3	SAS plug	5.3.2
		SATA device plug (single-port)	SATA
SAS backplane receptacle	5.3.4	SAS plug	5.3.2
		SATA device plug (single-port)	SATA
SAS external cable receptacle	5.3.5	SAS external plug	5.3.6
SAS external plug	5.3.6	SAS external cable receptacle	5.3.5

The SATA device plug connector (e.g., used by a disk drive) may be attached to a SAS backplane receptacle connector or a SAS internal cable receptacle connector, connecting the primary signal pairs and leaving the second signal pairs unconnected.

5.3 Connectors

5.3.1 Connectors overview

SAS connectors should be marked with the SAS logo (see Annex D).

5.3.2 SAS plug connector

5.3.2.1 SAS plug connector overview

SAS devices with internal ports shall use the SAS plug connector. The SAS plug connector is defined in SFF-8482. It attaches to SAS internal cable receptacle connectors (for SAS cables) and SAS backplane receptacle connectors (for SAS backplanes).

Table 8 shows the pins in the SAS plug connector.

Table 8. SAS plug connector pins

Segment	Pin	Name
Primary Signal	S1	GROUND
Primary Signal	S2	AR+
Primary Signal	S3	AR-
Primary Signal	S4	GROUND
Primary Signal	S5	AT-
Primary Signal	S6	AT+
Primary Signal	S7	GROUND
Secondary Signal	S8	GROUND
Secondary Signal	S9	BR+
Secondary Signal	S10	BR-
Secondary Signal	S11	GROUND
Secondary Signal	S12	BT-
Secondary Signal	S13	BT+
Secondary Signal	S14	GROUND
Power	P1	V_{33}
Power	P2	V_{33}
Power	P3	V_{33}, precharge
Power	P4	GROUND
Power	P5	GROUND
Power	P6	GROUND
Power	P7	V_5, precharge
Power	P8	V_5
Power	P9	V_5
Power	P10	GROUND
Power	P11	READY LED
Power	P12	GROUND
Power	P13	V_{12}, precharge
Power	P14	V_{12}
Power	P15	V_{12}

Notes:
Precharge and voltage pins shall be connected together.
S8 through S14 are no-connects on single port implementations.

~~Unlike SATA, the initiator device and target device share the same connector pin assignments. Therefore, the cable or backplane must swap the transmit and receive signal pairs.~~ Unlike SATA, the SAS initiator device and SAS target device share the same connector pin assignments. The SAS transmit and receive pin assignments are in the same locations as in SATA target devices. Therefore, the cable or backplane must swap the transmit and receive signal pairs. A SATA host pinout is different, not requiring the swap.

The AT+, AT-, AR+, and AR- signals are used by the primary physical link. The BT+, BT-, BR+, and BR- signals are used by the secondary physical link.

SAS plug connectors shall support at least 500 insertions and 500 removals.

5.3.3 SAS internal cable receptacle connector

SAS internal cables shall use the SAS internal cable receptacle connector. The SAS internal cable receptacle connector is defined in SFF-8482. It attaches to a SAS plug connector, providing contact for the power pins and the primary physical link.

Table 8 defines the signal assignment. The secondary signals, pins S8 through S14, are not used.

5.3.4 SAS backplane receptacle connector

SAS backplanes shall use the SAS backplane receptacle connector. The SAS backplane receptacle connector is defined in SFF-8482. It attaches to a SATA device plug connector, providing contact for only the power pins and the primary signal pins, or a SAS plug connector providing contact for the power pins and both primary and secondary signal pins.

Table 8 defines the signal assignments.

5.3.5 SAS external cable receptacle connector

SAS external cables shall use the SAS external cable receptacle connector. The SAS external cable receptacle connector is defined in SFF-8483. It includes special SAS keying. It attaches to a SAS external plug connector, providing contact for four physical links.

Table 9 shows how the connector signal pairs are used for applications using one, two, three, or four of the physical links.

Table 9. Physical link usage in wide connector

Physical link	Signal	Signal pin to use based on number of physical links supported by the cable			
		One	Two	Three	Four
1	T1+	S1	S1	S1	S1
	T1-	S2	S2	S2	S2
	R1+	S3	S3	S3	S3
	R1-	S4	S4	S4	S4
3	T3+	N/C	N/C	S5	S5
	T3-	N/C	N/C	S6	S6
	R3+	N/C	N/C	S7	S7
	R3-	N/C	N/C	S8	S8
4	T4+	N/C	N/C	N/C	S9
	T4-	N/C	N/C	N/C	S10
	R4+	N/C	N/C	N/C	S11
	R4-	N/C	N/C	N/C	S12
2	T2+	N/C	S13	S13	S13
	T2-	N/C	S14	S14	S14
	R2+	N/C	S15	S15	S15
	R2-	N/C	S16	S16	S16
Note: N/C: Not connected					

5.3.6 SAS external plug connector

SAS devices with external ports shall use the SAS external plug connector. The SAS external plug connector is defined in SFF-8483. It includes special SAS keying. It attaches to a SAS external cable receptacle connector, providing contact for the four physical links.

5.4 Cables

5.4.1 SAS internal cables

SAS internal cables shall use SAS internal cable receptacle connectors. The internal cable carries power signals (including READY LED).

SATA cables shall not be used for internal connections between SAS devices.

The SAS cable connector is only defined on the interface side. The back-end is left undefined to allow several options in implementation. Because of the many possible combinations, the configurations are beyond the scope of this specification. Some possible configurations include:

a) Device power, Ready LED signal, and the primary signal port connected directly to a motherboard or initiator device board;

b) Device power and the primary signal port connected directly to a motherboard or initiator device board, and the Ready LED signal connected to a unique destination; and

c) Device power directly connected to a power supply or power supply connector, Ready LED signal connected to a unique destination, and primary signal port connected to the initiator or expander device signal port.

5.4.2 SAS external cables

The SAS external cable is defined in SFF-8483. The external cable does not carry power signals (including READY LED).

Although the connector always supports ~~4~~ four physical links, the cable may support ~~1, 2, 3, or 4~~ one, two, three, or four physical links.

5.5 Backplanes

Backplanes designed with an expander device that supports SATA-only target ports shall support the SATA electrical specification for signals at the device connector. Since the expander device supports SAS electrical specifications, signals from the expander phy to the target phy may have better characteristics; signals driven by the target phy, however, only need to follow SATA rules.

SFF-8460 has the backplane recommendations

5.6 READY LED pin

The READY LED signal ~~and~~ may be driven by a target device to turn on an externally visible LED that indicates the state of readiness and activity of the target device.

All target devices shall support the READY LED signal. The system is not required to generate any visual output when the READY LED signal is raised, but if such a visual output is provided, it shall be white or green to indicate that normal activity is being performed. Additional optional flashing patterns may be used to signal vendor unique conditions, but these patterns are not part of the standard.

The READY LED signal is designed to pull down the cathode of an LED using an open collector or open drain driver circuit. The target device circuitry must be GROUND-tolerant, since this pin may be connected by a system directly to power supply GROUND. The LED anode shall be attached to an appropriate supply through a current limiting resistor. The LED and the current limiting resistor may be external to the target device.

Table 10 describes the output characteristics of the READY LED signal.

Table 10. Output characteristics of the READY LED signal

State	Output current	Output voltage
Drive LED off	-100 µA < I_{OH} < 100 µA	0 < V_{OH} < 5.5 V
Drive LED on	I_{OL} > 30 mA	0 < V_{OL} < 0.5V

The READY LED signal may optionally be driven by a backplane to turn on the external LED. This usage is vendor specific.

The READY LED signal shall driven by a target device using the following patterns:

a) If rotating media is spinning and the target device is processing a command, the target device shall not assert READY LED. The LED is off.

b) If the rotating media is not spinning, the target device shall assert READY LED with a 2 second cycle of 20% on, 80% off. The target device shall also assert READY LED while processing a command. The intent is that the light appears to be flashing with the 20%/80% cycle when the media is not spinning but that an indication is presented each time activity is in process. The target device may be removed with no danger of mechanical damage in this state.

c) If the target device is in the process of performing a spin-up or spin-down, it shall assert READY LED in such a manner that the light flashes on and off with a ~~1 second~~1 s cycle using a 50% duty cycle. The light is on for approximately 0,5 ~~seconds~~ s and off for approximately 0,5 ~~seconds~~s.

d) If the target device is ready, it shall assert READY LED continuously except when the target device is processing a command. When processing a command, the target device shall negate READY LED for a period long enough to be detected by an observer. The light is usually on, but flashes off when commands are processed.

e) If the target device is formatting, it shall toggle READY LED on and off with each cylinder change.

During the spin-down process, the target device transitions immediately from pattern d) to pattern c). When the target has reached a state stable enough for it to be removed without mechanical damage, it shall change from pattern c) to pattern b).

5.7 Driver and receiver electrical characteristics

5.7.1 Compliance and reference points

Compliance points are defined as the interoperability points at which the interoperability specifications shall be met. SAS compliance points are always at separable connectors, where SAS devices are interchangeable. Table 11 lists the compliance points.

Table 11. Compliance points

Compliance point	Type	Description
Dt	intra-enclosure	Drive connector; transmit serial port
Dr	intra-enclosure	Drive connector; receive serial port
Ct	inter-enclosure	External cabinet connector; transmit serial port
Cr	inter-enclosure	External cabinet connector; receive serial port

5.7.2 Optional interoperability points

Optional interoperability points are not points where any specifications are required to be met. In the normal case, these points are not accessible; however, devices at these points may be interchangeable, depending on the system design. These values are informative, listed to provide useful guidance values for aspects such as the allowable jitter output, jitter tolerance, and voltage levels at the inputs or outputs of an expander device or an initiator device that is consistent with the budgeting of the same attributes at compliance points. Table 12 lists the optional interoperability points.

Table 12. Optional interoperability points

Optional interoperability points	Description
Xt	Expander phy; transmit serial port
Xr	Expander phy; receive serial port
It	Initiator phy; transmit serial port
Ir	Initiator phy; receive serial port

5.7.3 General interface specification

A TxRx connection is the complete simplex signal path between the output reference point of one SAS phy or retimer to the input reference point of a second SAS phy or retimer, over which a BER of $<10^{-12}$ is achieved. It is one half of a duplex link.

A TxRx connection segment is that portion of a TxRx connection delimited by separable connectors or changes in media.

This section defines the interfaces of the serial electrical signal at the interoperability points Dt, Dr, Ct, and Cr in a TxRx connection. The existence of a Dt, Dr, Ct, and Cr point is determined by the existence of a connector at that point in a TxRx Connection.

Each conforming SAS phy shall be compatible with this serial electrical interface to allow interoperability within a SAS environment. All TxRx connections described in this clause shall operate within the BER objective (10^{-12}). The parameters specified in this section support meeting that requirement under all conditions including the minimum input and output amplitude levels. ~~**The system level BER requirements (e.g., BER < 10^{-12}) often require that the signal quality (eye amplitude and jitter) be better than 10^{-12} (usually a BER < 10^{-14}) in order to achieve the desired system BER with margin.**~~ **Note: Unanimous decision to remove, 5/2/02**

These specifications are based on ensuring interoperability across multiple vendors supplying the technologies (transceivers, expanders, initiators and cable plants) under the tolerance limits specified in the document. TxRx connections operating at these maximum distances may require some form of equalization (e.g., transmitter pre-emphasis, receiver adaptive equalization, or passive cable equalization) to enable the signal requirements to be met. Longer distances may be obtained by specifically engineering a TxRx connection based on knowledge of the technology characteristics and the conditions

under which the TxRx connection is installed and operated (e.g., a closed engineering environment); however, such distance extensions are outside the scope of this standard.

Table 13 defines the general interface characteristics.

Table 13. General interface characteristics

Characteristic	Units	1,5 Gbps	3,0 Gbps
Data rate	MBps	150	300
Nominal bit rate	Mbaud	1 500	3 000
Unit interval (UI)	ps	666,667	333,333
Data rate tolerance at Xr[b]	ppm	+350/-5 150	+350/-5 150
Data rate tolerance at Dr, Cr, Ir	ppm	+/-100	+/-100
Data rate tolerance at Dt, Ct, It, Xt	ppm	+/-100	+/-100
Media Impedance[a]	ohm	100	100
Notes: a) The media impedances are the differential, or odd mode, impedances. b) Supports a SATA 1.0 device with spread spectrum clocking.			

5.7.4 Eye masks

5.7.4.1 Eye masks overview

The eye masks shown in this clause shall be interpreted as graphical representations of the voltage and time limits. The time values between X1 and 1-X1 cover all but 10^{-12} of the jitter population. The random content of the total jitter population has a range of +/-7 sigma. Current oscilloscope technology only supports approximately +/-3 sigma, therefore the traditional method of using an oscilloscope to compare the signals against these masks to ascertain jitter compliance is invalid. The oscilloscope remains valid for determining rise/fall times, amplitude, and under and overshoots.

5.7.4.2 Transmitted eye masks at Dt, Ct, It, and Xt

Figure 25 describes the transmitted eye masks at the Dt, Ct, It, and Xt compliance points. These eye masks are directly applicable to compliance points, and are indirectly applicable to reference points.

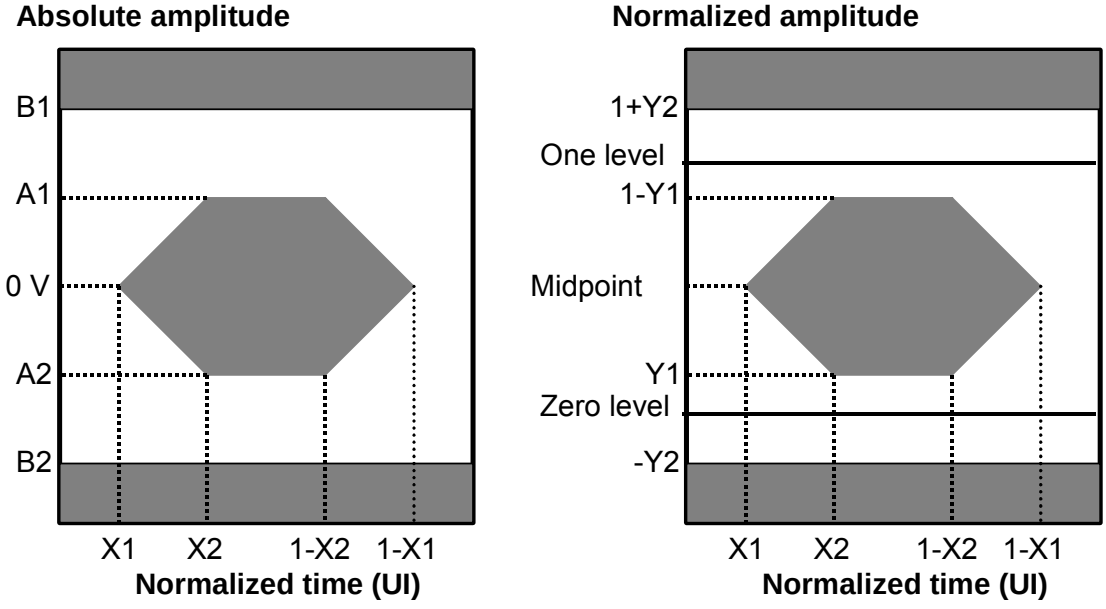

Figure 25. Absolute and normalized amplitude eye diagrams at Dt, Ct, It, and Xt

For unbalanced drivers the absolute amplitude values assume A.C. coupling between the test load and the driver. Drivers must meet the normalized and the absolute amplitude requirements. The Y1 and Y2

amplitudes allow signal undershoot and overshoot, respectively, relative to the levels determined to be one and zero.

To accurately determine the one and zero levels for use with the normalized mask, use an oscilloscope having an internal histogram capability. Use the voltage histogram capability and set the time limits of the histogram to extend from 0,4 UI to 0,6 UI. Set the voltage limits of the histogram to include only the data associated with the one level. The one level to be used with the normalized mask shall be the mean of the histogram. Repeat this procedure for the zero level.

The eye diagram mask applies to jitter after application of a single pole high-pass frequency-weighting function, which progressively attenuates jitter at 20 dB/decade below a frequency of bit rate/1 667.

5.7.4.3 Delivered (receive) eye mask at Dr, Cr, Ir, and Xr

Figure 26 describes the delivered (received) eye mask. This eye mask applies to jitter after the application of a single pole high-pass frequency-weighting function, which progressively attenuates jitter at 20 dB/decade below a frequency of the bit rate/1 667.

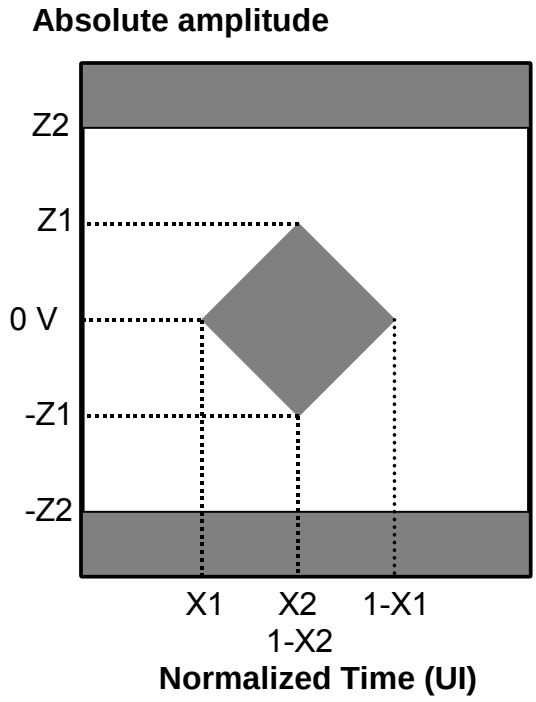

Figure 26. Eye mask at Dr, Cr, Ir, and Xr

Verifying compliance with the limits represented by the received eye mask should be done with reverse channel traffic present in order that the effects of cross talk are taken into account.

5.7.4.4 Jitter tolerance masks

Tolerance eye masks at Dt, Ct, It, and Xt shall be based on Figure 27 and shall be constructed using the X2, Z1 and Z2 values given in **Table** 17. X1 values shall be half the value for total jitter given in the tables for jitter value frequencies above bit rate/1 667.

~~Note that t~~The tolerance masks are identical to the output masks except that the X1 and X2 values are each increased by half the amount of the sinusoidal jitter values given in the jitter tolerance tables.

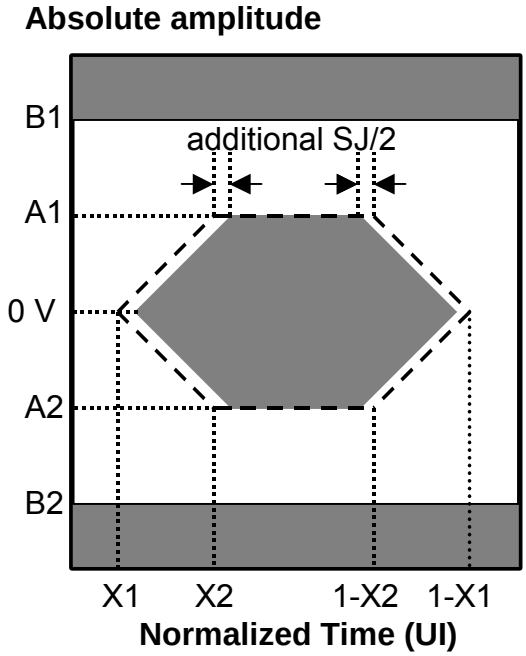

Figure 27. Deriving a tolerance mask at Dt, Ct, It, or Xt

Receiver Tolerance eye masks at Dr, Cr, Ir, and Xr shall be based on Figure 28 and shall be constructed using the X2 and Z2 values given in **Table** 17. X1 shall be half the value for total jitter given in these tables for jitter frequencies above bit rate/1 667.

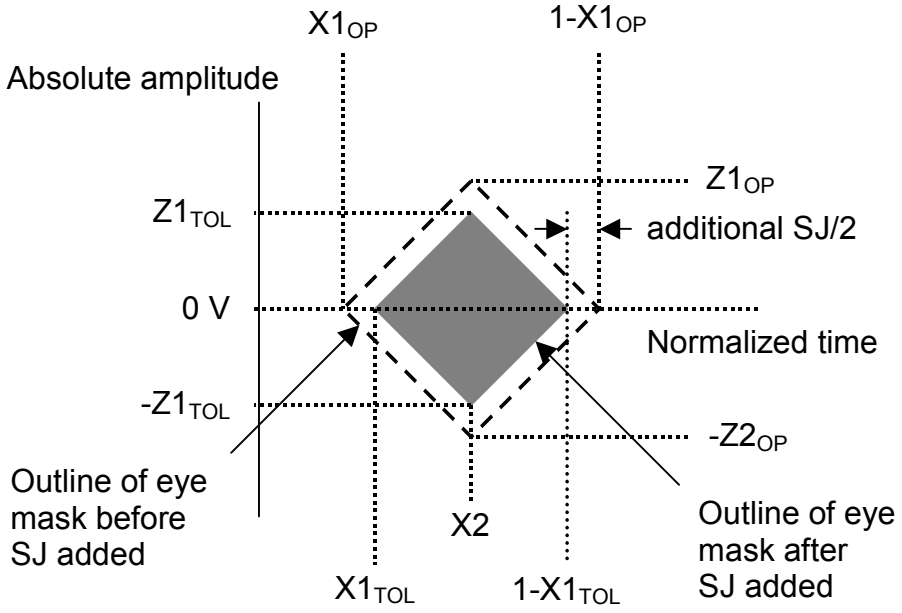

Figure 28. Deriving a tolerance mask at Dr, Cr, Ir, or Xr

However, the leading and trailing edge slopes of Figure 26 shall be preserved. As a result the amplitude value of Z1 is less than that given in Table 15 and must therefore be calculated from those slopes as follows:

$Z1_{Tol} = Z1_{OP} \times (X2_{OP} – (0{,}5 \times (\text{additional SJ UI})) - X1_{OP})/(X2_{OP} - X1_{OP})$

$Z1_{Tol}$ = value for Z1 to be used for the tolerance masks

$Z1_{OP}$, $X1_{OP}$, and $X2_{OP}$ are the values in **Table** 17 for Z1, X1, and X2

~~Note that t~~The X1 points in the receive tolerance masks are greater than the X1 points in the output masks, again due to the addition of sinusoidal jitter.

Figure 29 defines the sinusoidal jitter mask.

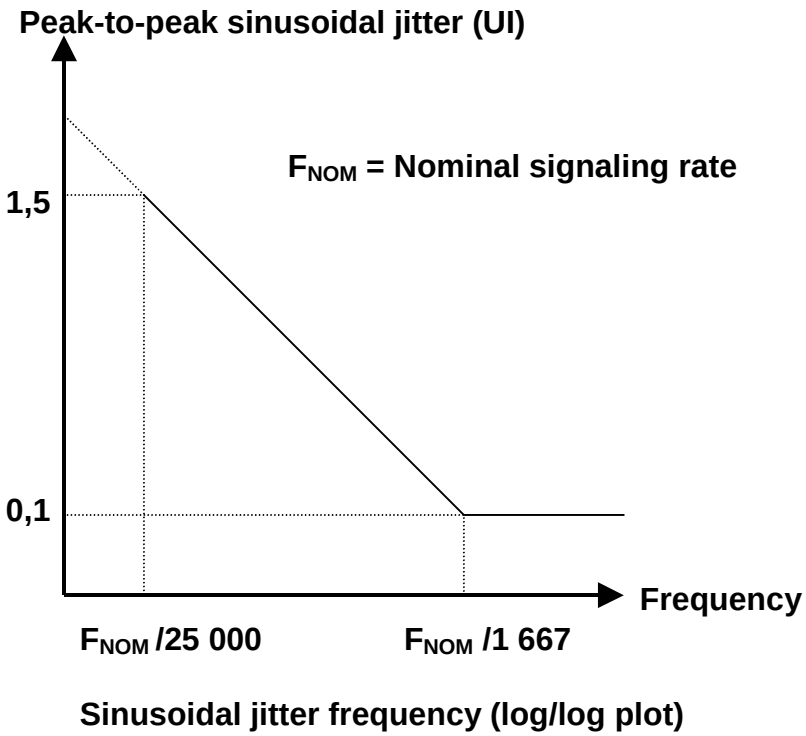

Figure 29. Sinusoidal jitter mask

5.7.5 Transmitted signal characteristics

This section defines the inter-operability requirements of the transmitted signal at the driver end of a TxRx connection as measured into the test load specified in Figure 30. All specifications are based on differential measurements.

The OOB sequence shall be performed at SATA 1.0 signal levels. As soon as COMSAS has been exchanged, the transmit levels shall increase to the SAS voltage levels specified in the following tables. Note: Change wording to support the OOB changes made 7/16/02 (SATA 1.0 signal level or the signal level of the lowest supported speed).

Table 14 specifies the transmitted signal characteristics at Tx compliance points and optional Tx compliance points.

Table 14. Transmitted signal characteristics at Tx compliance points

Compliance point	Signal characteristic	Units	SATA 1.0	1,5 Gbps	3,0 Gbps
Dt	Jitter Output Eye Mask (see Figure 25)[a]	N/A	N/A	See Table 16	See Table 16
	(B1-B2)[b]	mV(P-P)	N/A	1 200	1 600
	(A1-A2)[c]	mV(P-P)	N/A	600	800
	X1[d]	UI	N/A	0,125	0,175
	X2	UI	N/A	X1 + 0,21	X1 + 0,21
	Skew[g]	ps	N/A	20	10
	Tx Off Voltage[e]	mV(P-P)	N/A	< 50	< 50
	Y1	N/A	N/A	0,1	**[TBD]**
	Y2	N/A	N/A	0,2	**[TBD]**
	Maximum rise/fall time[f]	ps	N/A	273	137
	Minimum rise/fall time[f]	ps	N/A	133	67
Ct	Jitter Output Eye Mask (see Figure 25)[a]	N/A	N/A	See Table 16	See Table 16
	(B1-B2)[b]	mV(P-P)	N/A	1 600	1 600
	(A1-A2)[c]	mV(P-P)	N/A	800	800
	X1[d]	UI	N/A	0,125	0,175
	X2	UI	N/A	X1 + 0,21	X1 + 0,21
	Skew[g]	ps	N/A	20	10
	Tx off voltage[e]	mV(P-P)	N/A	< 50	< 50
	Y1	N/A	N/A	0,1	**[TBD]**
	Y2	N/A	N/A	0,2	**[TBD]**
	Maximum rise/fall time[f]	ps	N/A	273	137
	Minimum rise/fall time[f]	ps	N/A	133	67
Xt, It[g] optional compliance points	Jitter output eye mask (see Figure 25)[a]	N/A	See Table 16	See Table 16	See Table 16
	(B1-B2)[2]	mV(P-P)	900[h]	1 200	1 600
	(A1-A2)[3]	mV(P-P)	600[h]	600	800
	X1[d]	UI	0,125	0,125	0,175
	X2	UI	X1 + 0,21	X1 + 0,21	X1 + 0,21
	Skew[g]	ps	20	20	20
	Tx off voltage[e]	mV(P-P)	< 50	< 50	< 50
	Y1	N/A	0,1	0,1	**[TBD]**
	Y2	N/A	0,2	0,2	**[TBD]**
	Maximum rise/fall time[f]	ps	273	273	137
	Minimum rise/fall time[f]	ps	133	133	67

Notes:

a) Drivers shall meet both the absolute and normalized amplitude requirements.

b) The B amplitude specification identifies the maximum signal peak (including overshoots) that can be delivered into a resistive load matching those shown in Figure 30.

c) The minimum allowed peak-to-peak eye amplitude opening that shall be delivered into a resistive load matching those shown in Figure 30, is equal to the A1-A2 amplitude shown above.

d) The value of X1 shall be half the value for total jitter given in Table 16. The test or analysis shall include for the effects of a single pole high-pass frequency-weighting function, which progressively attenuates jitter at 20 dB/decade below a frequency of bit rate/1 667. The value for X1 applies at a total jitter probability of 10^{-12}. At this level of probability direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter output requirements.

e) The transmitter off voltage is the maximum voltage measured at point compliance points Ct and Dt and reference points It and Xt when the transmitter is logically turned off or is unpowered.

f) Rise/fall times are measured~~ments to be made using an oscilloscope with a bandwidth including probes of at least 1,8 times the baud rate~~ **from 20% to 80% of the "one" and "zero" amplitudes as derfined in section 5.7.4.2, using a test load as in figure 30. Note: Unanimous decision to change, 7/8/02**

g) ~~**Skew measurements shall be made using an oscilloscope with a bandwidth including probes of at least 1,8 times the baud rate.**~~ **SATA 1.0 column does not apply to It. Note: Unanimous decision to change, 5/2/02**

h) Minimum and maximum recommended launch levels. Implementation should consider possible loss to achieve SATA 1.0 compliance at the drive connector. At the drive connector, SATA 1.0 allows 600 mV peak-to-peak maximum, 325 mV peak-to-peak minimum.

[Editor's note: The preemphasis specs for Y1 and Y2 appropriate for 3,0 Gbps are still under investigation and are listed as TBD. More than 20% seems likely.]

5.7.6 Received signal characteristics

Table 15 defines the inter-operability requirements of the delivered signal at the receiver end of a TxRx connection as measured into the test load specified in Figure 30. It also defines optional Rx compliance points. All specifications are based on differential measurements.

Table 15. Delivered signal characteristic at Rx compliance points

Compliance point	Signal characteristic	Units	SATA 1.0	1,5 Gbps	3,0 Gbps
Dr	Jitter output eye mask[b] (see Figure 26)	N/A	N/A	See Table 16	See Table 16
	2 x Z2	mV(P-P)	N/A	1 200	1 600
	2 x Z1	mV(P-P)	N/A	325	275
	X1[a]	UI	N/A	0,25	0,25
	X2	UI	N/A	0,50	0,50
	Skew[c]	ps	N/A	50	25
	Max voltage (non-op)	mV(P-P)	N/A	2 000	2 000
	OOB detect ~~threshold min~~ guaranteed on (eye opening)[d]	mV(P-P)	N/A	**~~150~~ 240**	**~~150~~ 240**
	OOB detect guaranteed off signal level[d]	mV(P-P)	**N/A**	**120**	**120**
	Max near-end crosstalk	mV(P-P)	N/A	100	100
Cr	Jitter output eye mask[b] (see Figure 26)		N/A	See Table 16	See Table 16
	2 x Z2	mV(P-P)	N/A	1 600	1 600
	2 x Z1	mV(P-P)	N/A	275	275
	X1[a]	UI	N/A	0,275	0,275
	X2	UI	N/A	0,50	0,50
	Skew[c]	ps	N/A	50	25
	Max voltage (non-op)	mV(P-P)	N/A	2 000	2 000
	OOB detect ~~threshold min~~ guaranteed on (eye opening)[d]	mV(P-P)	N/A	**~~150~~ 240**	**~~150~~ 240**
	OOB detect guaranteed off signal level[d]	mV(P-P)	**N/A**	**120**	**120**
	Max near-end crosstalk	mV(P-P)	N/A	100	100
Xr, Ir[c] optional compliance points	Jitter output eye mask[b] (see Figure 26)		See Table 16	See Table 16	See Table 16
	2 x Z2	mV(P-P)	600	1 200	1 600
	2 x Z1	mV(P-P)	225	325	275
	X1[a]	UI	0,275	0,275	0,275
	X2	UI	0,50	0.50	0,50
	Skew[c]	ps	50	50	25
	Max voltage (non-op)	mV(P-P)	2 000	2 000	2 000
	OOB detect ~~threshold min~~ guaranteed on (eye opening)[d]	mV(P-P)	**~~100~~ 240**	**~~150~~ 240**	**~~150~~ 240**
	OOB detect guaranteed off signal level[d]	mV(P-P)	**120**	**120**	**120**
	Max near-end crosstalk	mV(P-P)	< 50	100	100

Notes:

a) The value for X1 shall be half the value given for total jitter in Table 16. The test or analysis shall include the effects of a single pole high-pass frequency-weighting function, which progressively attenuates jitter at 20 dB/decade below a frequency of bit rate/1 667.

b) The value for X1 applies at a total jitter probability of 10^{-12}. At this level of probability direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter output requirements.

c) ~~**Skew measurements shall be made using an oscilloscope with a bandwidth including probes of at least 1,8 times the baud rate. Maximum transmitter and maximum interconnect skew is assumed.**~~ **SATA 1.0 column does not apply to Ir. Note: Unanimous decision to change, 5/2/02**

d) **Worst case signals are trapezoidal. Guaranteed on level based on 2x ratio to guaranteed off level. Note: Unanimous decision to change OOB levels and add this note, 6/24/02**

5.7.7 Jitter output

Table 16 defines the allowable output jitter at the compliance points. Entries for inter-enclosure TxRx connections and for intra-enclosure TxRx connections are covered.

Table 16. Jitter output compliance points

Compliance point	1,5 Gbps		3 Gbps	
	Deterministic jitter	Total jitter	Deterministic jitter	Total jitter
Dt	0,15	0,25	0,20	~~0,30~~ 0,35
Dr	~~0,30~~ 0,35	~~0,50~~ 0,55	0,35	~~0,50~~ 0,55
Ct	0,15	0,25	0,20	0,35
Cr	0,35	0,55	0,35	0,55
It	0,15	0,25	0,20	0,35
Ir	0,35	0,55	0,35	0,55
Xt	0,15	0,25	0,20	0,35
Xr	0,35	0,55	0,35	0,55

Note: Unanuimous decision to change Table values, 7/16/02

Notes:

a) It, Ir, Xt, and Xr are optional compliance points.

b) Units are in UI.

c) The values for jitter in this section are measured at the average amplitude point.

d) Total jitter (TJ) is the sum of deterministic jitter (DJ) and random jitter (RJ). If the actual deterministic jitter is less than the maximum specified, then the random jitter may increase as long as the total jitter does not exceed the specified maximum total jitter.

e) Total jitter is specified at a probability of 10^{-12}.

f) The deterministic and total values in this table apply to jitter after application of a single pole high-pass frequency-weighting function, which progressively attenuates jitter at 20 dB/decade below a frequency of bit rate/1 667.

g) Values at the various points are determined by the application.

h) If total jitter delivered at any point is less than the maximum allowed, then the jitter distribution of the signals is allowed to be asymmetric. The total jitter plus the magnitude of the asymmetry must not exceed the allowed maximum total jitter. The numerical difference between the average of the peaks (at 10^{-12}) and the average of the individual events is the measure of the asymmetry. Jitter peak-to-peak measured < (TJ max - |Asymmetry|).

~~i)~~ ~~**SERDES voltage sensitivity to switching power supply noise: Jitter values specified above shall be achieved even in an environment of switching noise pulses with peak-to-peak amplitude of 50 mV, rise/fall times from 10 ns to 500 ps, and multiple pulse duration of up to 2,0 µs maximum. A real-time sampling scope is required to make this measurement.**~~ **Note: Unanimous decision to delete, 5/2/02**

5.7.8 Jitter tolerance

Table 17 defines the minimum allowable jitter tolerance at the required and optional compliance points. Entries for inter-enclosure TxRx connections and for intra-enclosure TxRx connections are covered. ~~**SERDES voltage sensitivity to switching power supply noise: Jitter values specified above shall be achieved even in an environment of switching noise pulses with peak-to-peak amplitude of 50 mV, rise/fall times from 10 ns to 500 ps, and multiple pulse duration of up to 2,0 µs maximum. A real-time sampling scope is required to make this measurement.**~~ **Note: Unanimous decision to delete, 5/2/02**

Table 17. Jitter tolerance compliance points

Compliance point	1,5 Gbps			3,0 Gbps		
	Sinusoidal jitter[b]	Deterministic jitter[c,f]	Total jitter[f]	Sinusoidal jitter[d]	Deterministic jitter[e,f]	Total jitter[f]
Ct	0,10	0,15	0,35	0,10	0,20	0,45
Cr	0,10	~~**0,10**~~ **0,35**	0,65	0,10	0,35	0,65
Dt	0,10	0,15	0,35	0,10	0,20	0,45
Dr	0,10	~~**0,30**~~ **0,35**	0,65	0,10	~~**0,30**~~ **0,35**	0,65
It, Xt[g]	0,10	0,15	0,35	0,10	0,20	0,45
Ir, Xr[g]	0,10	0,35	0,65	0,10	0,35	0,65

Note: Unanuimous decision to change table values, 7/16/02

Notes:

a) Units are in UI.

b) Sinusoidal swept frequency: 900 kHz to > 5 MHz. The jitter values given are normative for a combination of DJ, RJ, and SJ (sinusoidal jitter) which receivers shall be able to tolerate without exceeding a BER of 10^{-12}.

c) Deterministic jitter: 900 kHz to 750 MHz. No value is given for random jitter. For compliance with this standard, the actual random jitter amplitude shall be the value that brings total jitter to the stated value at a probability of 10^{-12}.

d) Sinusoidal swept frequency: 1 800 kHz to > 5 MHz. Receivers shall tolerate sinusoidal jitter of progressively greater amplitude at lower frequencies, according to the mask in Figure with the same DJ and RJ levels as were used in the high frequency sweep.

e) Deterministic jitter: 1 800 kHz to 1 500 MHz. The additional 0,1 UI of sinusoidal jitter is added to ensure the receiver has sufficient operating margin in the presence of external interference.

f) The deterministic and total values in this table apply to jitter after application of a single pole high-pass frequency-weighting function, which progressively attenuates jitter at 20 dB/decade below a frequency of bit rate/1 667.

g) Optional compliance point.

5.7.9 Impedance specifications

Table 18 defines impedance requirements.

Table 18. Impedance requirements

Requirement	Units	1,5 Gbps	3,0 Gbps
~~Time domain reflectometer rise time~~ TDR risetime 20% - 80%[a,b]	ps	~~85~~ 100	~~85~~ 50
~~Common mode impedance~~[b,c,d]	~~ohm~~	~~32,5 +/- 7,5~~	~~32,5 +/- 7,5~~
~~Cable pair matching~~[b,c,d]	~~ohm~~	~~+/- 5~~	~~+/- 5~~
Media (PCB or cable) [b,c,d]	~~ohm~~	~~100 +/- 10~~	~~100 +/- 10~~
Differential impedance [b,c,d]	ohms	100 +/- 10	100 +/- 10
Single-ended impedance match [b,c,d]	ohms	+/- 5	+/- 5
Common mode impedance [b,c,d]	ohms	32,5 +/-7,5	32,5 +/-7,5
~~Through~~ Mated connectionors[b]	~~ohms~~	~~100 +/- 15~~	~~100 +/- 15~~
Differential impedance [b,c,d]	ohms	100 +/- 15	100 +/- 15
Single-ended impedance match [b,c,d]	ohms	+/- 5	+/- 5
Common mode impedance [b,c,d]	ohms	32,5 +/-7,5	32,5 +/-7,5
Receiver termination [b,e,f]	~~ohm~~	~~100 +/- 15~~	~~100 +/- 15~~
Differential impedance [b,e,f]	ohms	100 +/- 15	100 +/- 15
Single-ended impedance match [b,e,f]	ohms	+/- 5	+/- 5
Area of impedance dip [b,e,f]	ps	150 max	100 max
Common mode impedance [b,e]	ohms	20 min / 40 max	20 min / 40 max
Transmitter source termination [b,e,f]	~~ohm~~	~~100 +/- 15~~	~~100 +/- 15~~
Differential impedance [b]	ohms	60 min / 115 max	60 min / 115 max
Single-ended impedance match [b]	ohms	+/- 5	+/- 5
Common mode impedance [b]	ohms	15 min / 40 max	15 min / 40 max

Notes:

a) All times indicated for time domain reflectometer measurements are recorded times. Recorded times are twice the transit time of the time domain reflectometer signal.

b) All measurements are made through mated connector pairs.

c) The media impedance measurement identifies the impedance mismatches present in the media when terminated in its characteristic impedance. This measurement includes mated connectors at both ends of the media, where they exist, and any intermediate connectors or splices.

d) Where the media has an electrical length of > 4 ns the procedure detailed in SFF-8410, or an equivalent procedure, shall be used to determine the impedance.

e) The receiver termination impedance specification applies to each and every receiver in a TxRx connection and covers all time points between the connector nearest the receiver, the receiver, and the transmission line terminator. This measurement shall be made from that connector.

f) At the time point corresponding to the connection of the receiver to the transmission line the input capacitance of the receiver and its connection to the transmission line may cause the measured impedance to fall below the minimum impedances specified in this table. The area of the dip **(amplitude in units of the reflection coefficient rho, and duration in time)** caused by this capacitance is directly proportional to the capacitance. An approximate value for the area is given by the product of the amplitude of the dip (in units of ~~rho~~Γ, the reflection coefficient) and its width[a] (in picoseconds) measured at the half amplitude point. The ~~**product**~~ **area** calculated by this method shall not be greater than ~~**150 ps**~~ **the values shown in the above table**. The amplitude is defined as being the difference in ~~rho~~ the reflection coefficient between the ~~rho~~ reflection coefficient at the nominal impedance and the ~~rho~~ reflection coefficient at the minimum impedance point.

5.7.10 Electrical TxRx connections

TxRx connections may be divided into TxRx connection segments. In a single TxRx connection individual TxRx connection segments may be formed from differing media and materials, including traces on printed wiring boards and optical fibers. This clause applies only to TxRx connection segments that are formed from an electrically conductive media.

Each electrical TxRx connection segment shall comply with the impedance requirements of Table 18 for the media from which they are formed. An optional equalizer network, when present in a TxRx connection, shall exist and operate as part of the cable plant.

TxRx connections that are composed entirely of electrically conducting media shall be applied only to homogenous ground applications, such as between devices within an enclosure or rack, or between enclosures interconnected by a common ground return or ground plane. This restriction minimizes safety and interference concerns caused by any voltage differences that could otherwise exist between equipment grounds.

5.7.11 Driver characteristics

For all inter-enclosure TxRx connections, the output shall be A.C. coupled to the cable through a transmission network.

For intra-enclosure TxRx connections the expander shall be A.C. coupled to the media. Other drivers may be A.C. or D.C. coupled.

The driver shall have the output voltages and timing listed in Table 14 and Table 16 measured at the designated interoperability points. The default point is Ct for inter-cabinet TxRx connections and Dt for intra-cabinet TxRx connections. The measurements shall be made across a load equivalent to that shown in Figure 30.

The relevant eye diagrams are given in 5.7.4. The normalized amplitudes, Y1 and Y2, allow signal undershoots. The driver shall meet both the normalized and absolute values.

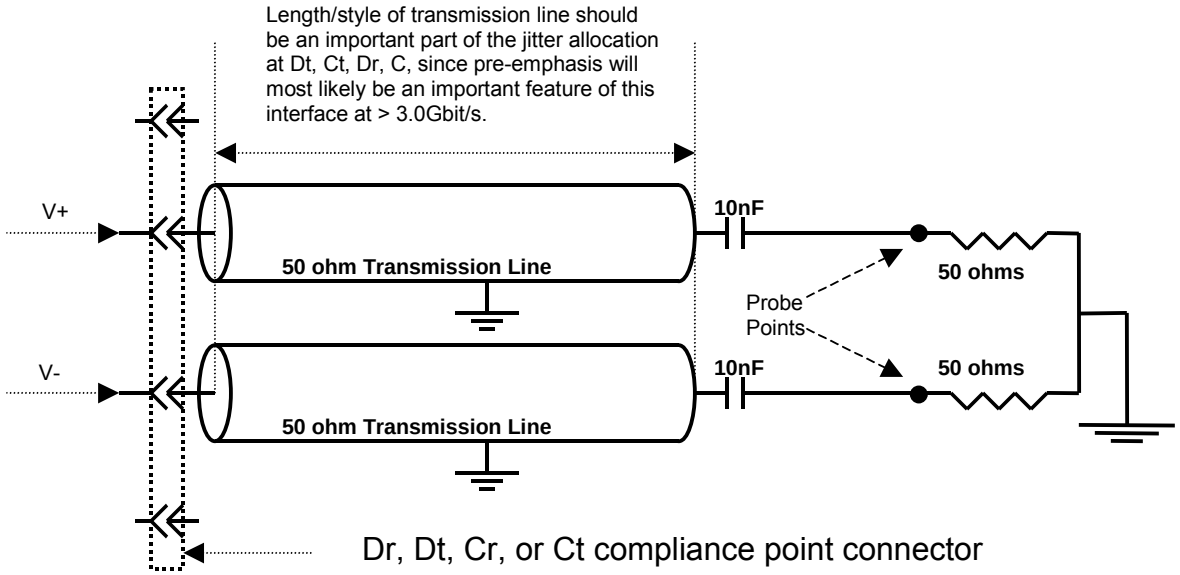

Figure 30. Test loads

5.7.12 Receiver characteristics

The receiver shall be A.C.-coupled to the media through a receive network. The receive network shall terminate the TxRx connection by a 100 ohm equivalent impedance as specified in Table 18.

The receiver shall operate within the BER objective (10^{-12}) when a SAS signal with valid voltage and timing characteristics is delivered to the interoperability point from a 100 ohm source. The delivered SAS signal shall be considered valid if it meets the voltage and timing limits specified in Table 16 when measured across a load equivalent to those of Figure 30.

Additionally the receiver shall also operate within the BER objective when the signal at a receiving phy has the additional sinusoidal jitter present that is specified in the Table 17. Jitter tolerance figures are given in 5.7.4.4 for all interoperability points in a TxRx connection. The figures given assume that any external interference occurs prior to the point at which the test is applied. When testing the jitter tolerance capability of a receiver the additional 0,1 UI of sinusoidal jitter may be reduced by an amount proportional to the actual externally induced interference between the application point of the test and the input to the receiving phy. The addition of additional jitter reduces the eye opening in both voltage and time; see the Jitter tolerance masks in 5.7.8.

5.7.13 Spread spectrum clocking

Phys shall not transmit with spread spectrum clocking. Expander phys that support being attached to SATA target phys shall support receiving with spread spectrum clocking. The expander device shall retime data from a SATA target phy with an internal clock before forwarding to the rest of the domain.

5.8 Non-tracking clock architecture

Phys shall be designed with a non-tracking clock architecture, where the receive clock has no relationship to the transmit clock. Expander phys that support being attached to SATA target phys shall tolerate clock tracking by the SATA target phy.