

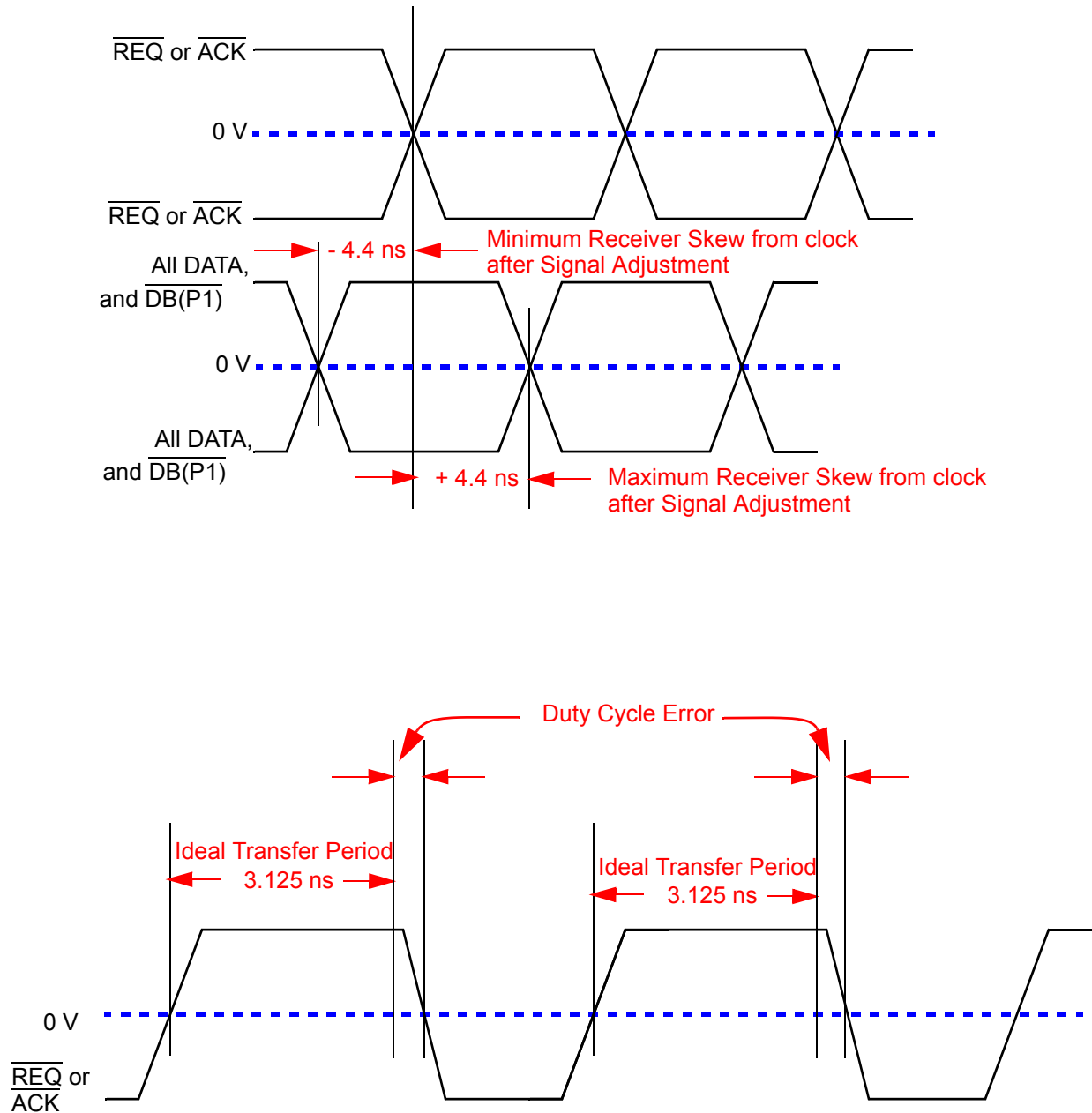
Date: July 10, 2002

To: T10 Committee (SCSI)

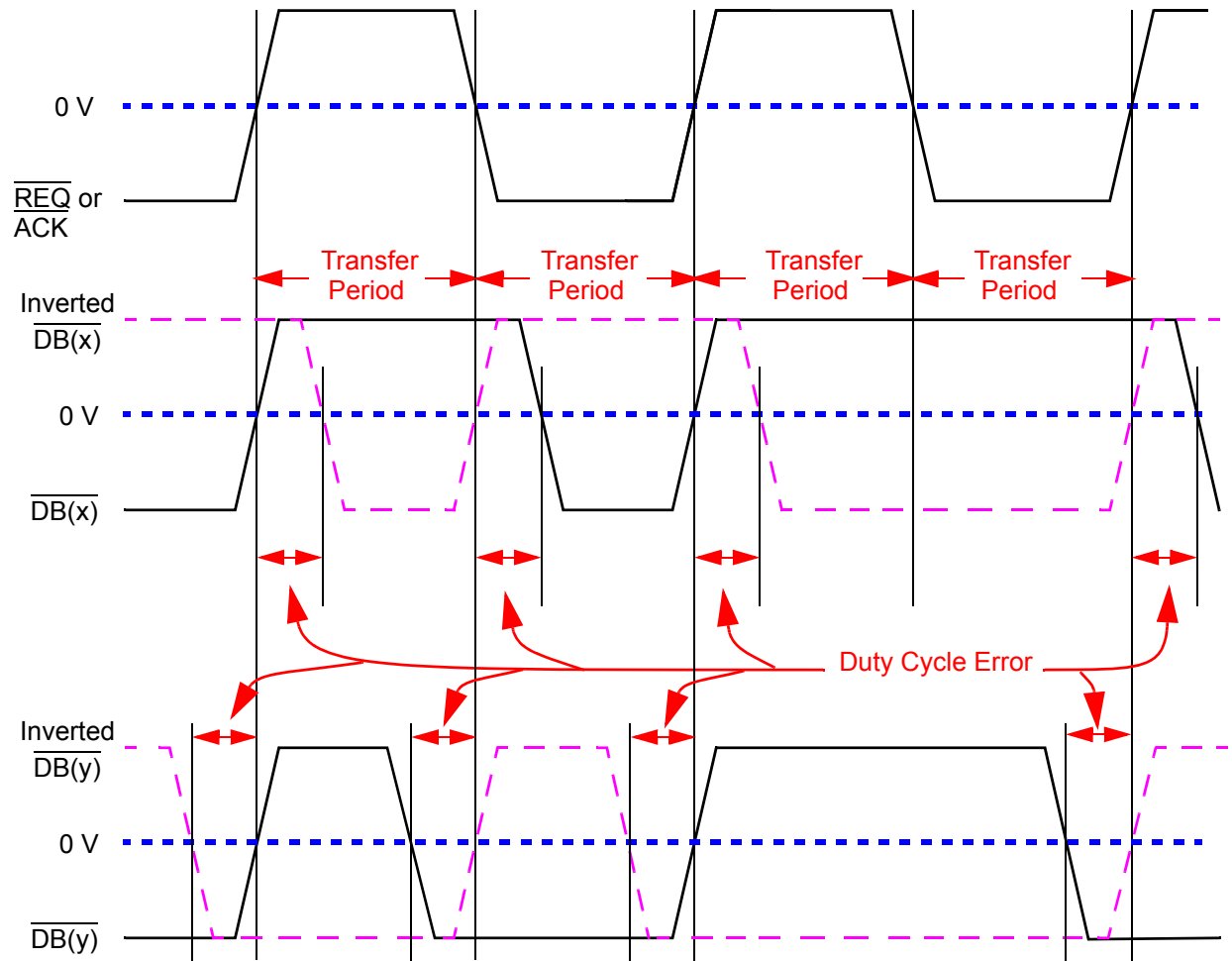
From: George Penokie (IBM/Tivoli)

Subject: Clock-to-Data and Duty Cycle Timings

1 Overview



Note: The duty cycle error may be plus or minus from the idle transfer period



The drive time asymmetry plus receiver time asymmetry equals the duty cycle error.

The maximum receiver skew from clock after the signal adjustment circuit shall consist of the following times:

- the transmitter chip skew;
- the receiver chip skew;
- the cable skew; and
- two times the trace skew.

The worst case skew from either the rising edge or the falling edge referenced to the clock including the duty cycle error shall not exceed the maximum receiver skew from clock (+/- 4.4 ns).