



Maxtor Corporation
500 McCarthy Boulevard
Milpitas, CA 95035 USA

To: T10 Parallel SCSI Working Group
From: Russ Brown
Email: russ_brown@maxtor.com
Contact: Mark Evans
Email: mark_evans@maxtor.com
408-894-5310
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Subject: Proposal for SPI-5 for Ultra640 AAF receiver masks

Introduction

The following is a proposal to modify SPI-5 clause 9.4.5 Paced transfers with precompensation disabled to include the requirements for Ultra640. All references in the following are to the draft standard SCSI Parallel Interface – 5 (SPI-5) revision 1. The changes required by this proposal are in **RED** font.

9.4.5 Paced transfers with pre-compensation disabled on fast-160 and fast-320

During paced transfers with a negotiated transfer rate of fast-160 or fast-320 and with precompensation disabled, receiving SCSI devices shall operate with signals that meet all of the following requirements at the receiver:

- a) A change in amplitude for all transitions shall be greater than 100 mV (see figure 73).
- b) The differential low frequency signal amplitude shall not exceed the following limits:

$$600 \text{ mV} < (|V_A| + |V_N|) < 1,7 \text{ V peak-to-peak}$$

Where:

- a) V_A and V_N shall be measured after 100 ns continuous assertion or negation of the signal;
and
- b) the low frequency is 2,5 MHz or less

NOTE 31 – The section A of the training pattern meets the low frequency requirements (see 10.7.4.2).

- c) The differential offset component of the signal shall not exceed the following limits:

Fast-160	$-50 \text{ mV} < [(V_A - V_N) / 2] < 50 \text{ mV}$
Fast-320	$-75 \text{ mV} < [(V_A - V_N) / 2] < 75 \text{ mV}$

Where:

- a) V_A and V_N shall be measured after 100 ns continuous assertion or negation of the signal; and
- b) the low frequency is 2,5 MHz or less

NOTE 32 – The section A of the training pattern meets the low frequency requirements (see 10.7.4.2).

- d) The amplitude of any signal transitioning at the negotiated transfer period (e.g., clocking signals, any data signal with a 1010 bit pattern) shall be at least 240 mV derived as follows:

$$240 \text{ mV} < (|V_A| \text{ min} + |V_N| \text{ min})$$

Where:

- a) V_A and V_N shall not be measured until at least 20 transitions have occurred on the signal being measured; and
- b) for fast-160, V_A and V_N shall be measured within a 2 ns interval centered on the assertion or negation pulse (see figure 72); and
- c) for fast-320, V_A and V_N shall be measured within a 1 ns interval centered on the assertion or negation pulse (see figure 72).

NOTE 33 – The section A of the training pattern meets the requirements described in this subclause (see 10.7.4.2).

- e) All non-clocking signals shall meet the requirements defined for the isolated negation pulse receiver mask (see figure 75) and the isolated assertion pulse receiver mask (see figure 74).

The receiver input masks only measure the A.C. components of the input waveforms. Any D.C. ~~term~~ differential offset component shall be removed before applying the mask.

Receiver input eye masks in figures 72, 73, 74, 75 and 76 illustrate the requirements described in this subclause using the parameters in table x:

Parameter	Fast-160	Fast-320
Tcell	6,25 ns	3,125 ns
W1	2,0 ns	1,0 ns
W2	1,50 ns	0,75 ns
W3	2,125 ns	1,063 ns
W4	2,375 ns	1,188 ns

Table x – Receiver eye mask values

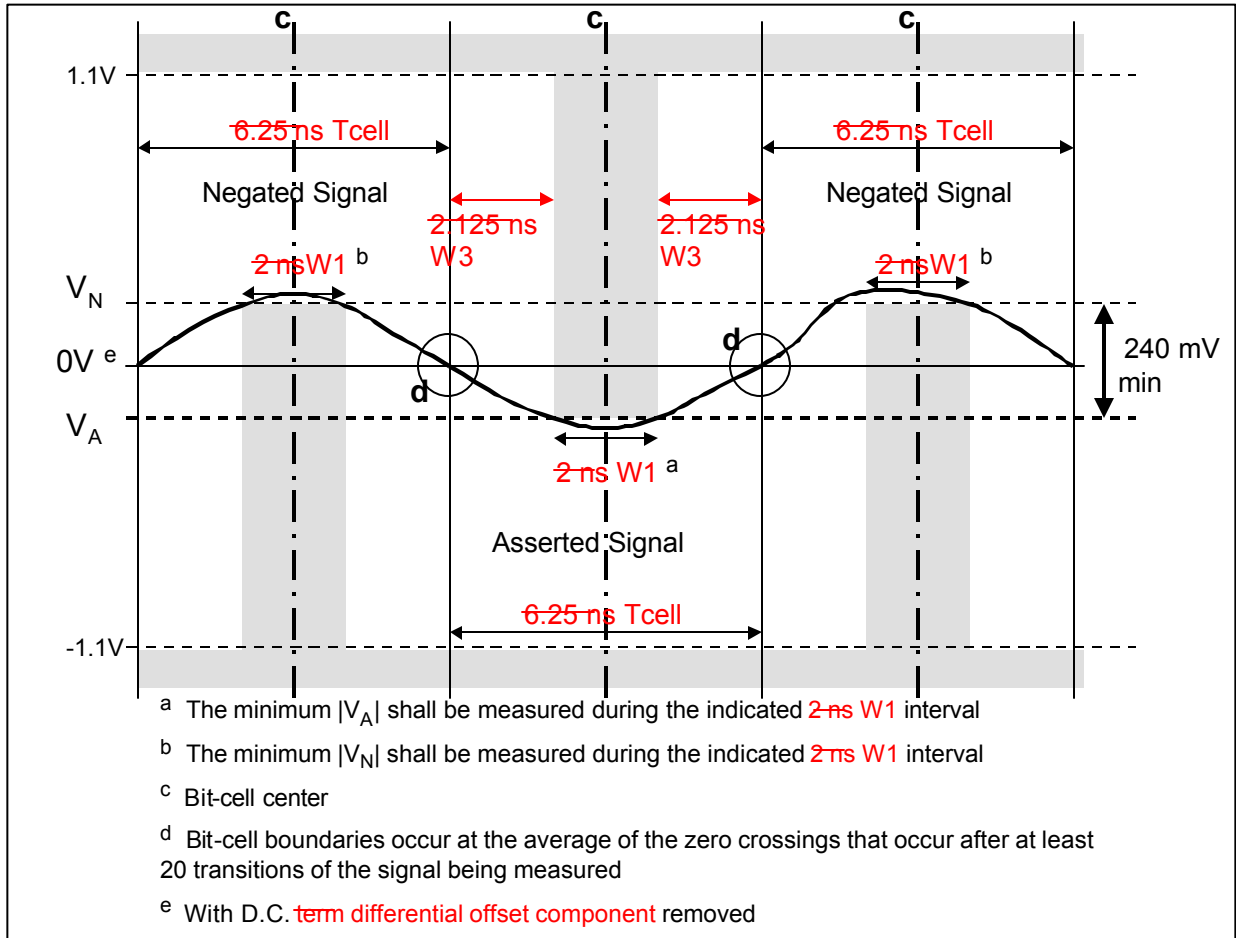


Figure 72 – **Fast-160** LVD paced transfer receiver mask for non-precompensated signals transitioning at the negotiated transfer period

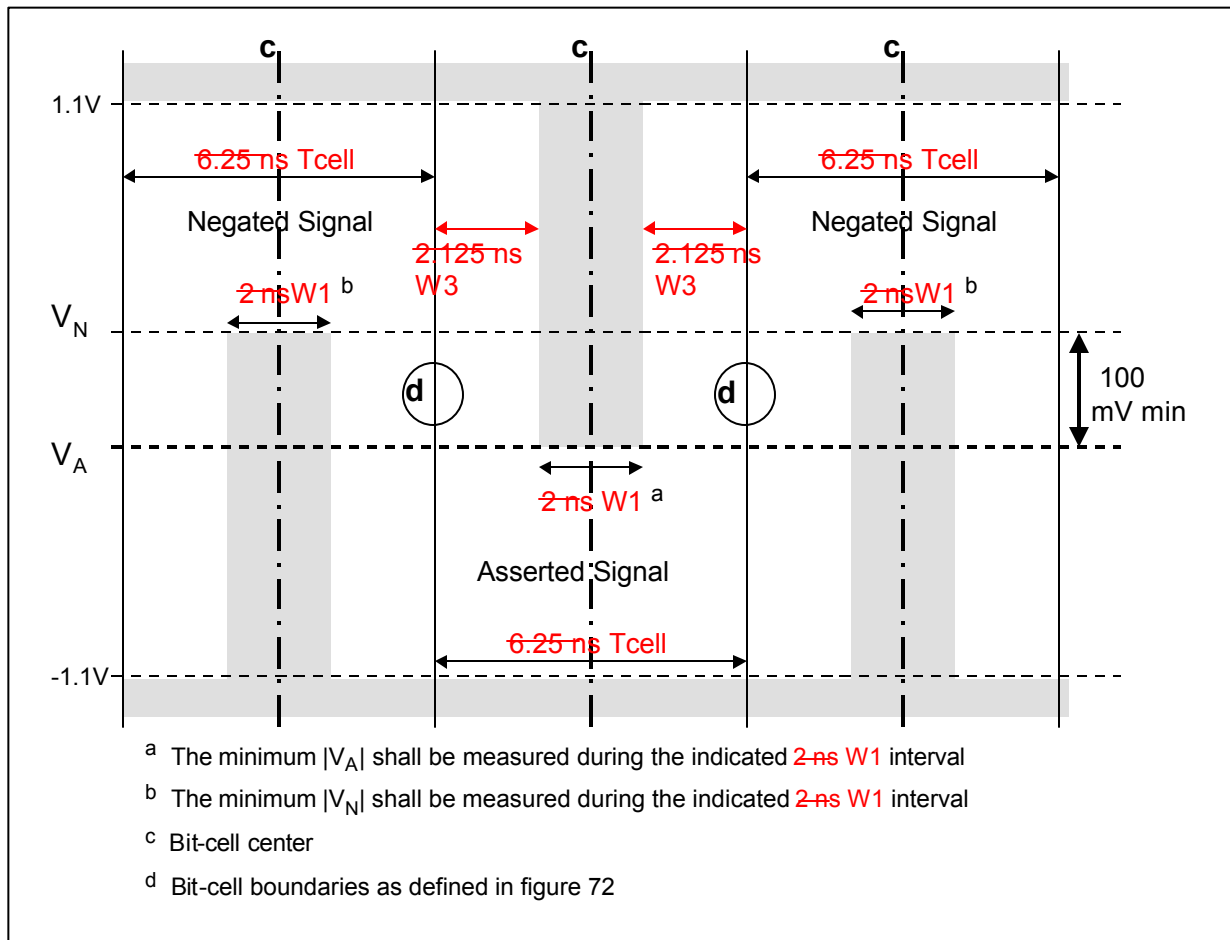


Figure 73 – ~~Fast-160~~ LVD paced transfer receiver mask non-precompensated minimum amplitude change

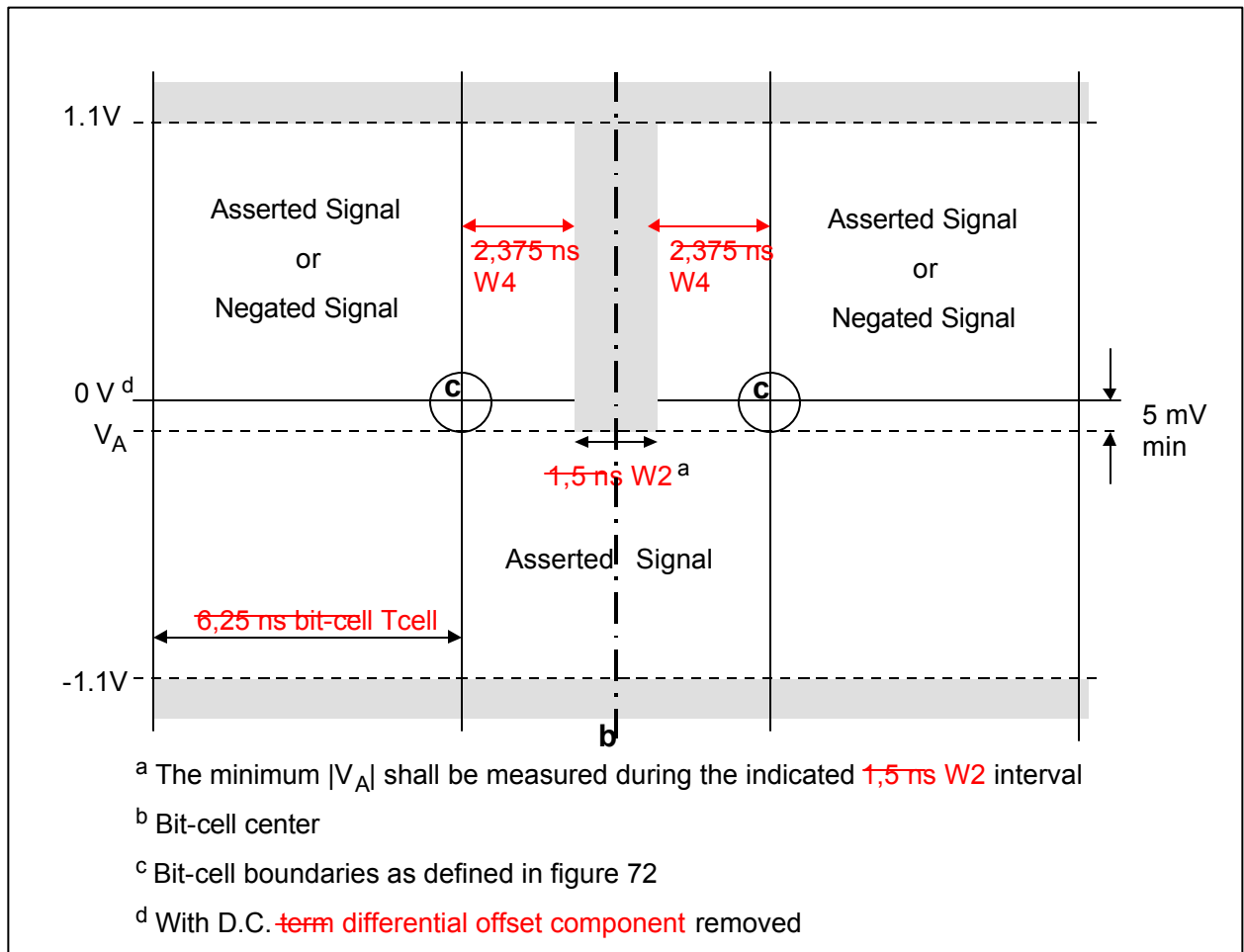


Figure 74 – ~~Fast-160~~ LVD paced transfer receiver mask non-precompensated non-clocking isolated assertion pulse

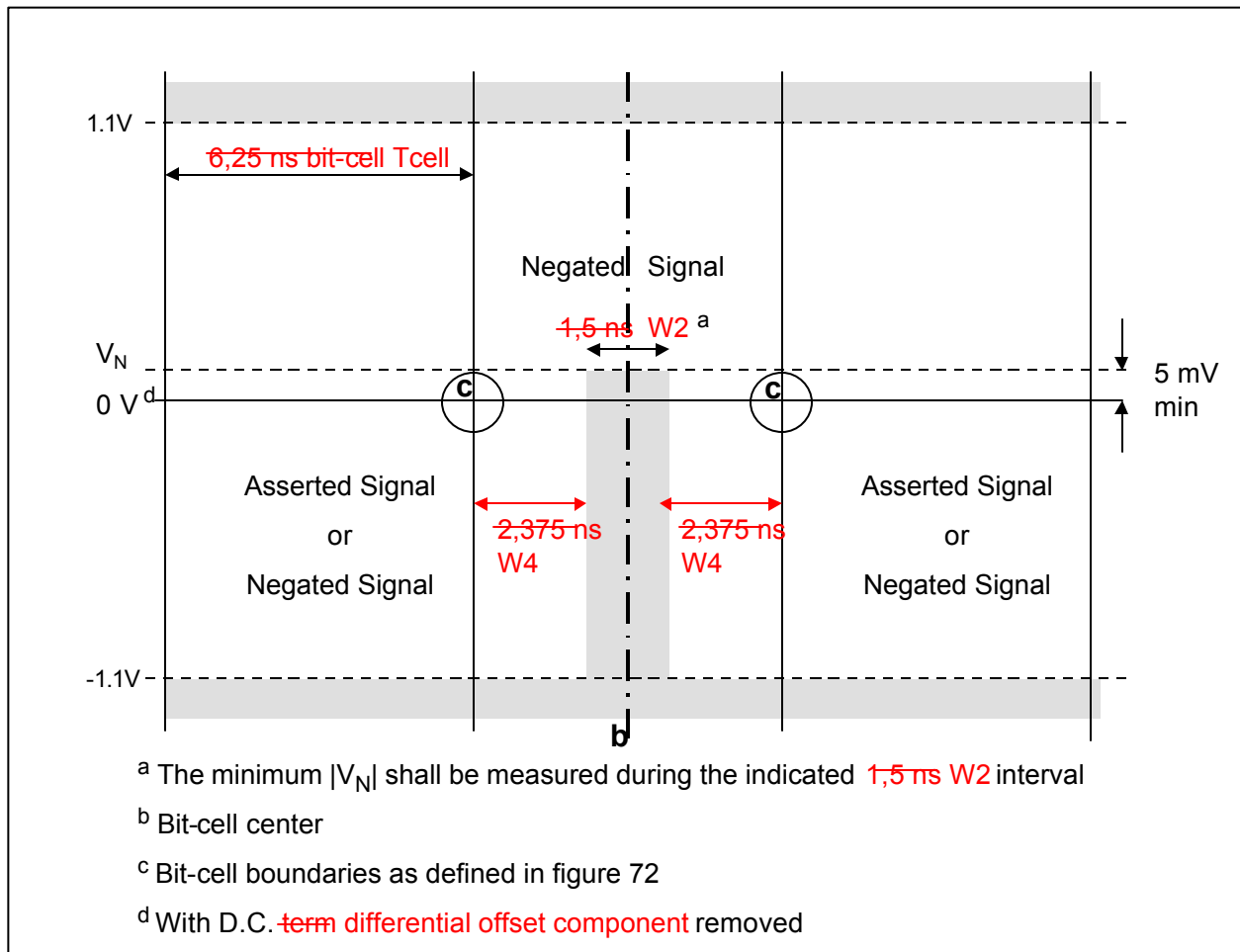


Figure 75 – Fast-160 LVD paced transfer receiver mask non-precompensated non-clocking isolated negation pulse

The eye diagram is formed by superimposing the waveforms of all bit cells of the input data pattern. **The For Fast-160**, the input data pattern shall be open for 1,5 ns centered on the bit-cell center, **and for Fast-320**, the input data pattern shall be open for 0,75 ns centered on the bit-cell center (see figure 76).

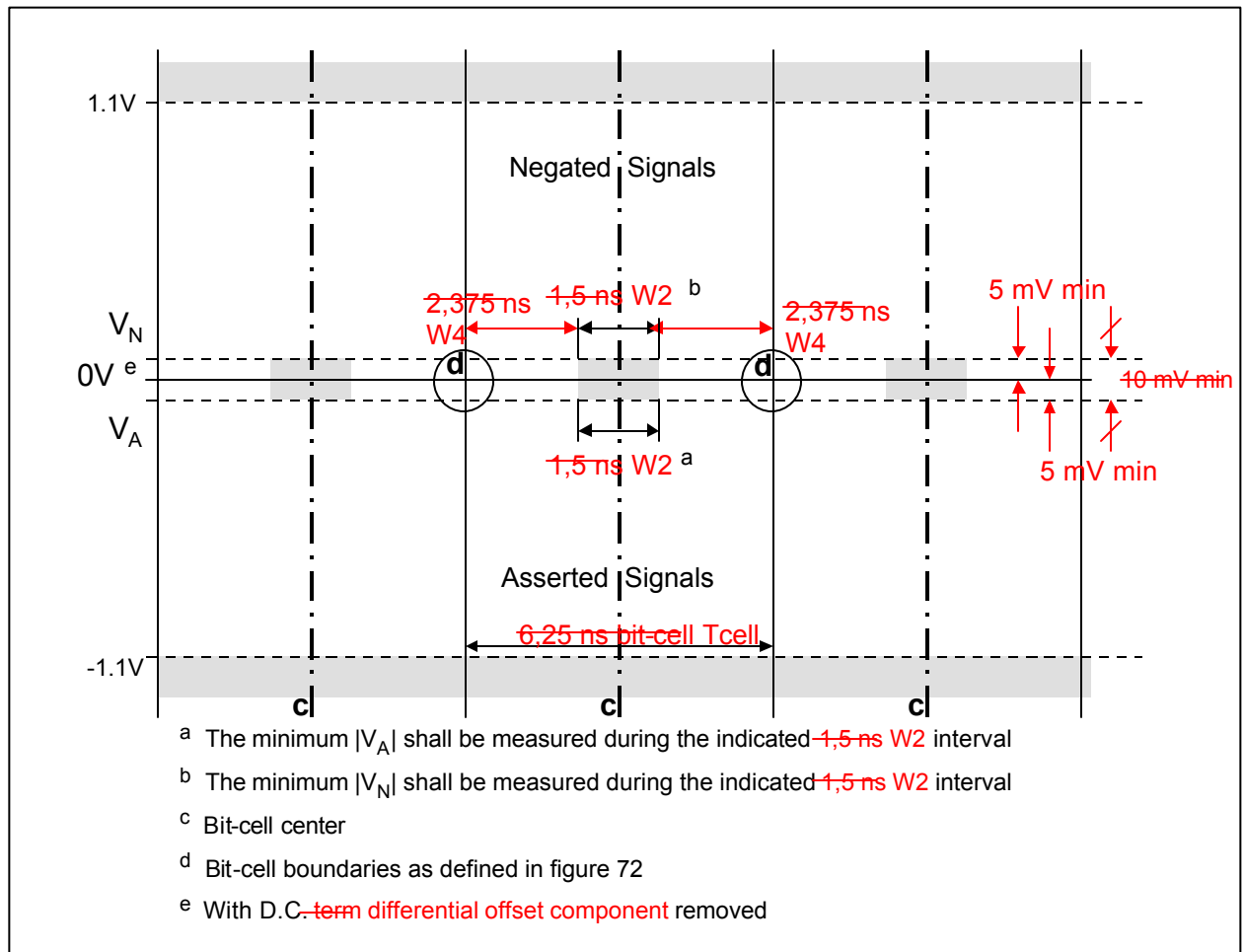


Figure 76 – **Fast-160** LVD paced transfer eye mask non-precompensated non-clocking pulse