Common Mode Shift Oxide Stress

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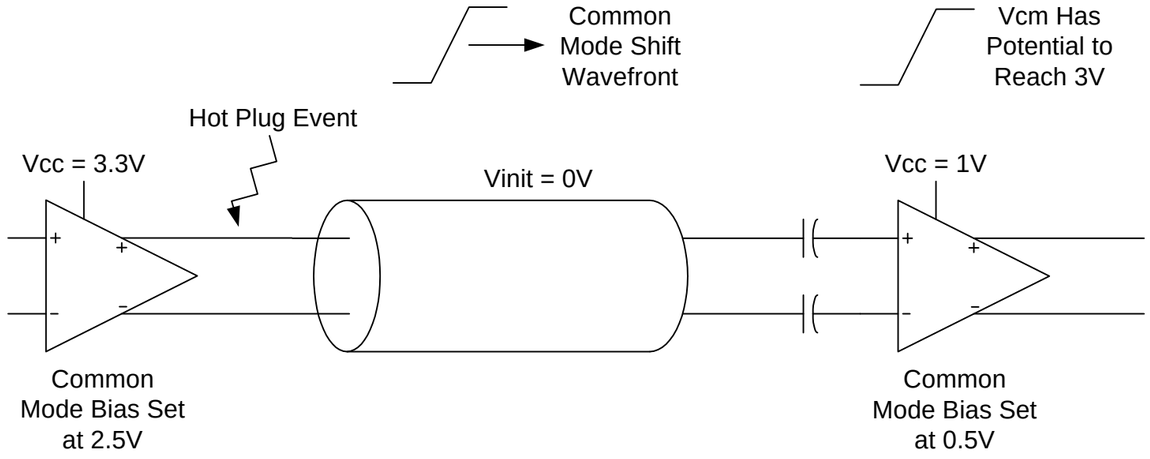
Problem Definition

- Sudden common mode shifts can occur during a hot plug event or during power-on
  - Both Tx/Rx will send a common mode shift across the physical link
  - Far-side PHY experiences the summation of common modes at its terminals
- Problem is magnified when two wildly different common modes are used at each end

Example Drawing

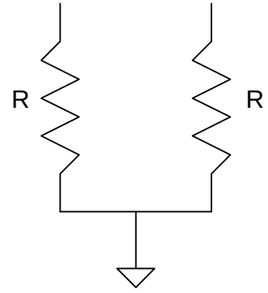


Common Mode Impedance Electrical Specification

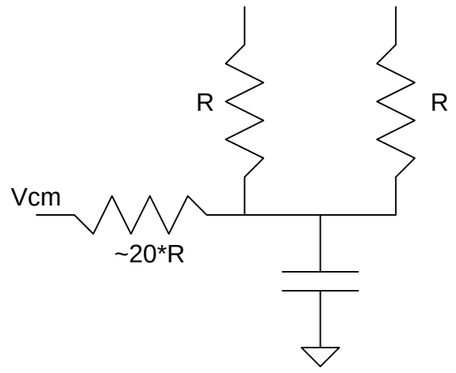
- In document number 02-210r1.pdf
  - CM Impedance is 15min/40max at 1.5Gb/s
  - CM Impedance is 15min/40max at 3.0Gb/s
  - CM Impedance value at DC is not specified
    - Allows for several different impedance implementations
      - Ex: series local common mode bias capacitor

Termination Examples

Example 1

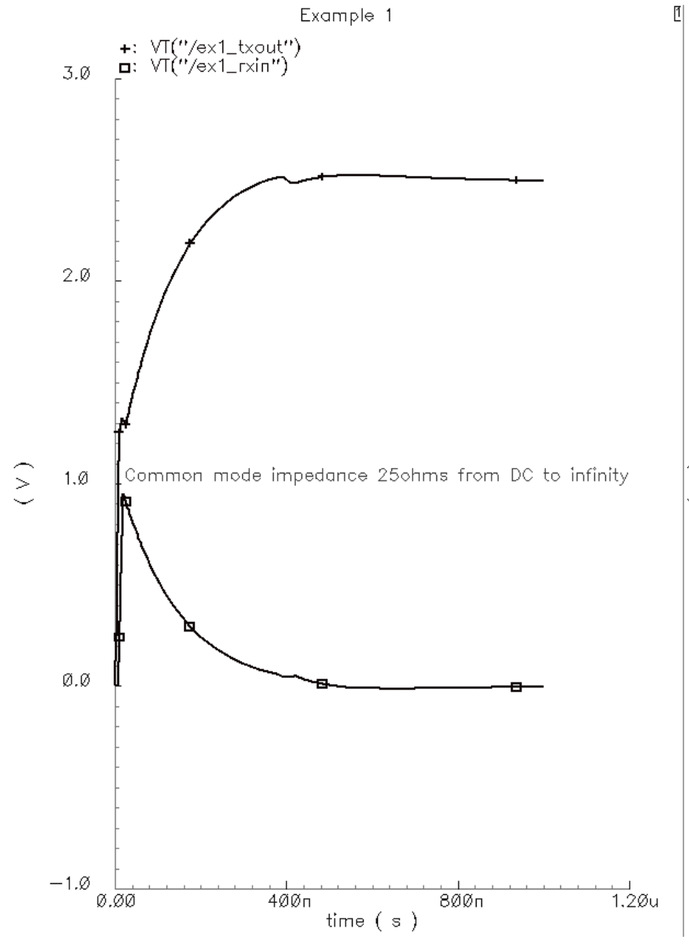


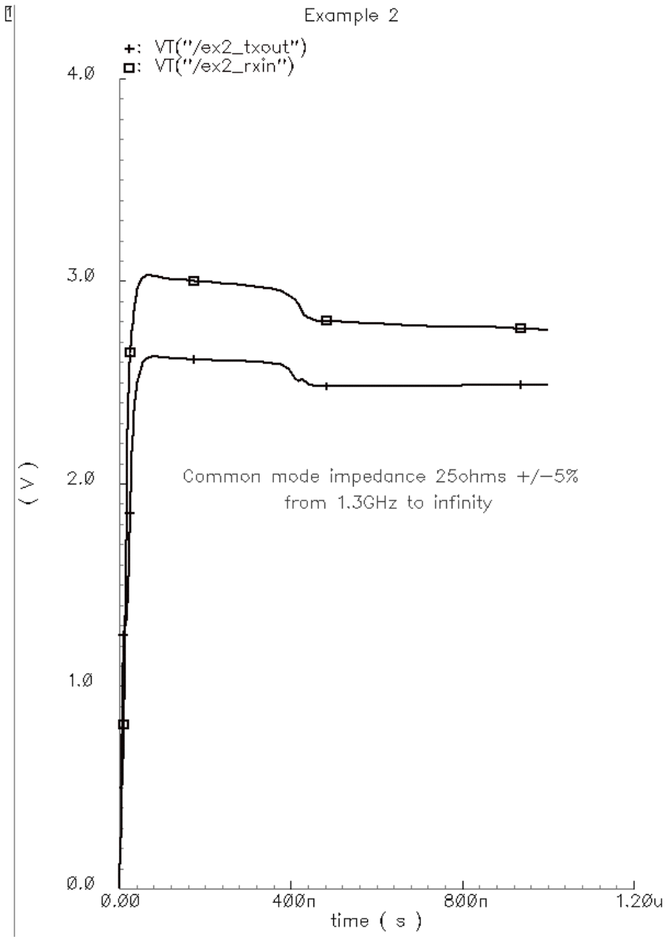
Example 2



Waveforms

Common Mode Shift Due to Transmit Hot Plug





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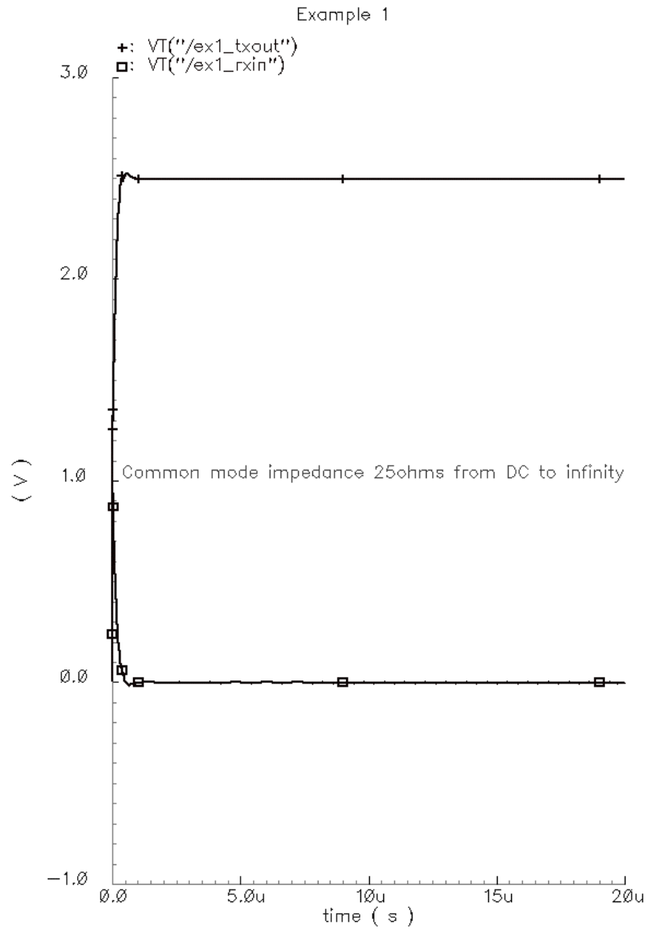

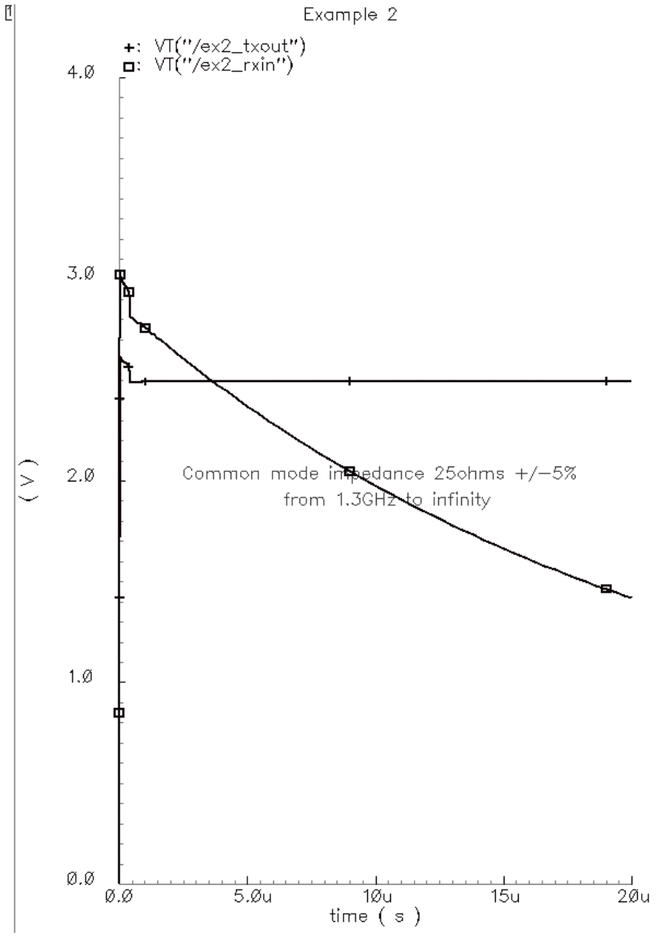

Generalized Solution Space

- External components may be able to clamp common mode shifts
  - Adds cost to the system
- Specify a maximum voltage on a physical link
  - Maybe restrictive in terms of design
- Put an IC solution into the standard
- Others?

Next Steps

- Schedule and open dialogue regarding common mode shift oxide stress
- Decide whether information regarding CM shift stress should be placed within the standard