Date: June 25, 02
To: T10 Technical Committee
From: Jim Coomes (jim.comes@seagate.com)
Subject: Bit and byte order for scrambling, CRC and transmission

This proposal is updated to show byte order input to scrambling, CRC, transmit order and receive order.

Both SAS and SATA data are organized into 32 bit chucks called dwords. A 10,000 foot view on the data flow in a port would appear as in figure 1.

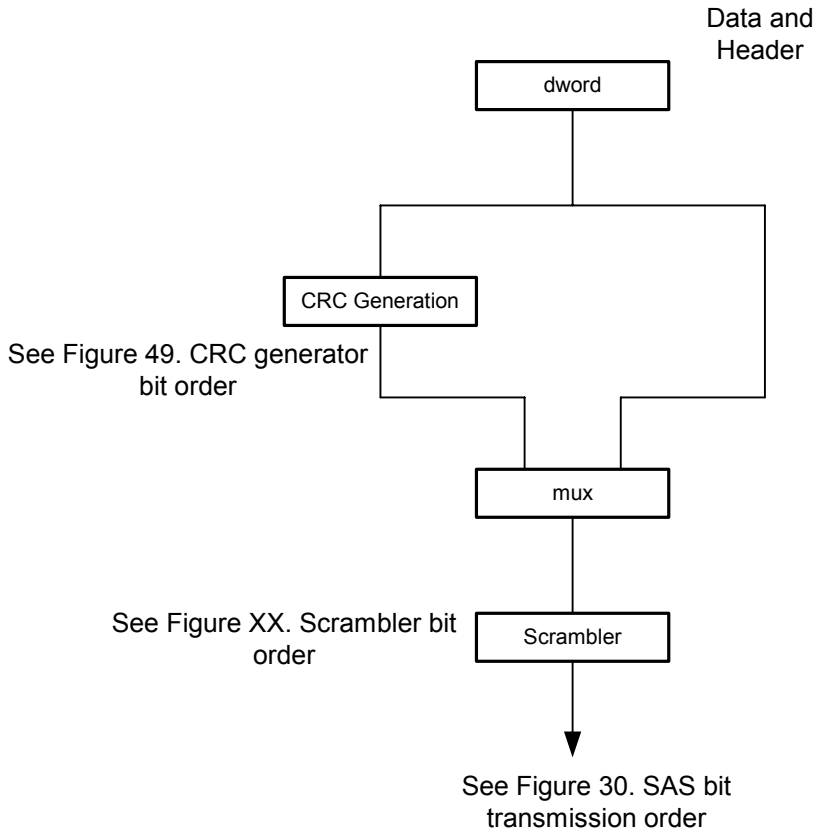

Figure 1 – Port data path

CRC bit order

The order of the bits presented to the CRC generation logic has to match the order the bits will be transmitted on the physical serial link to optimize data protection. If CRC is generated on a bit wide bases, data would be serially shifted into the generator in the order it is transmitted. However, CRC generation is typically based on dword input to allow the logic to run at reasonable clock rates. The input to the CRC generation logic still has to be in the order the bits will be transmitted. For the SAS big endian transmission order, the data has to be ordered as in figure 2.

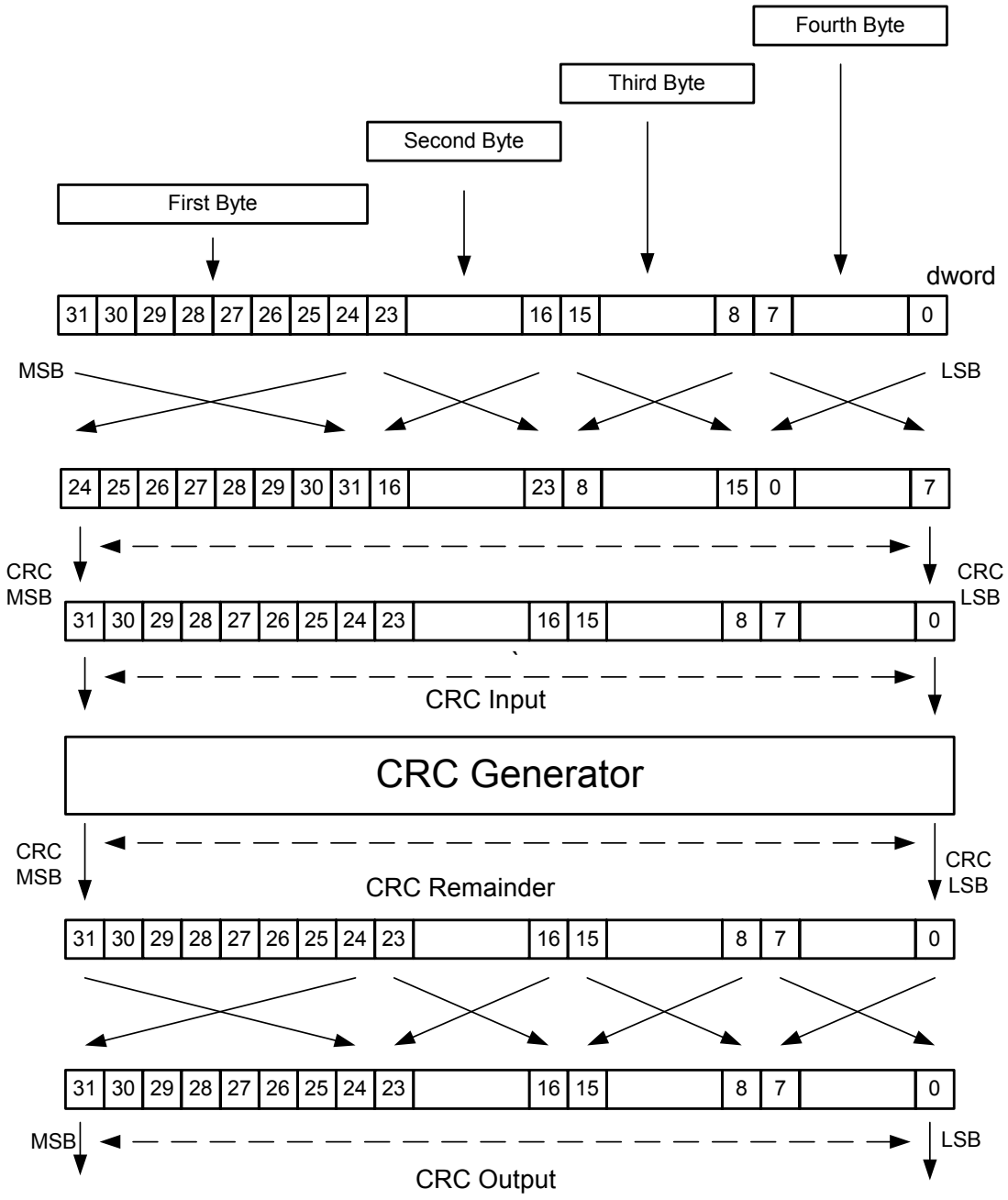

Figure 2 – CRC Generator

The output of the CRC block in this example has to restore the bit order to be compatible with the dword data path to the scrambler.

Scrambling bit order

The scrambling function is intended to randomize the image of the data to prevent repetitive patterns from being present on the physical link. This randomization prevents repeating 10 bit

characters from appearing on the physical link. This function may be performed on the straight dword path as the randomization is not depended on the transmission bit order. Figure 3 is the bit order for the data/CRC flowing through the scrambler block.

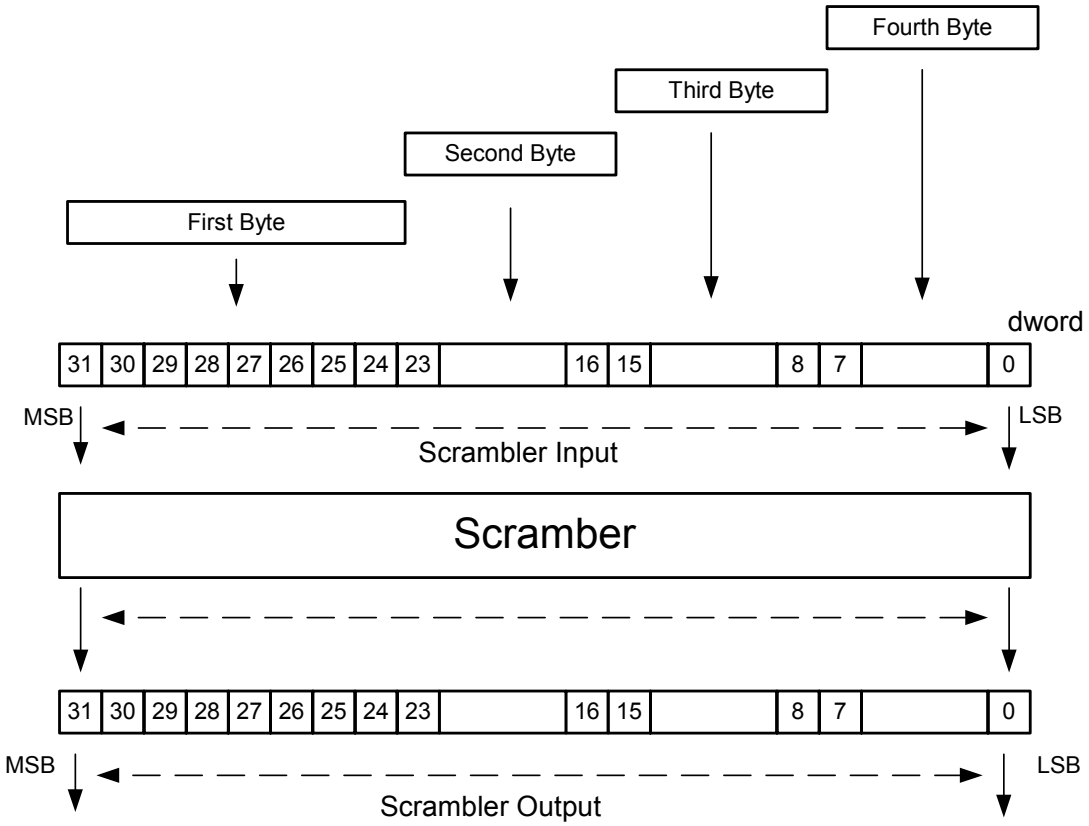

Figure 3 – Scrambler

Bit transmission order

To support big endian byte order and follow the 8b/10b for running disparity, the transmission order for data and the CRC field is as shown in figure 4.

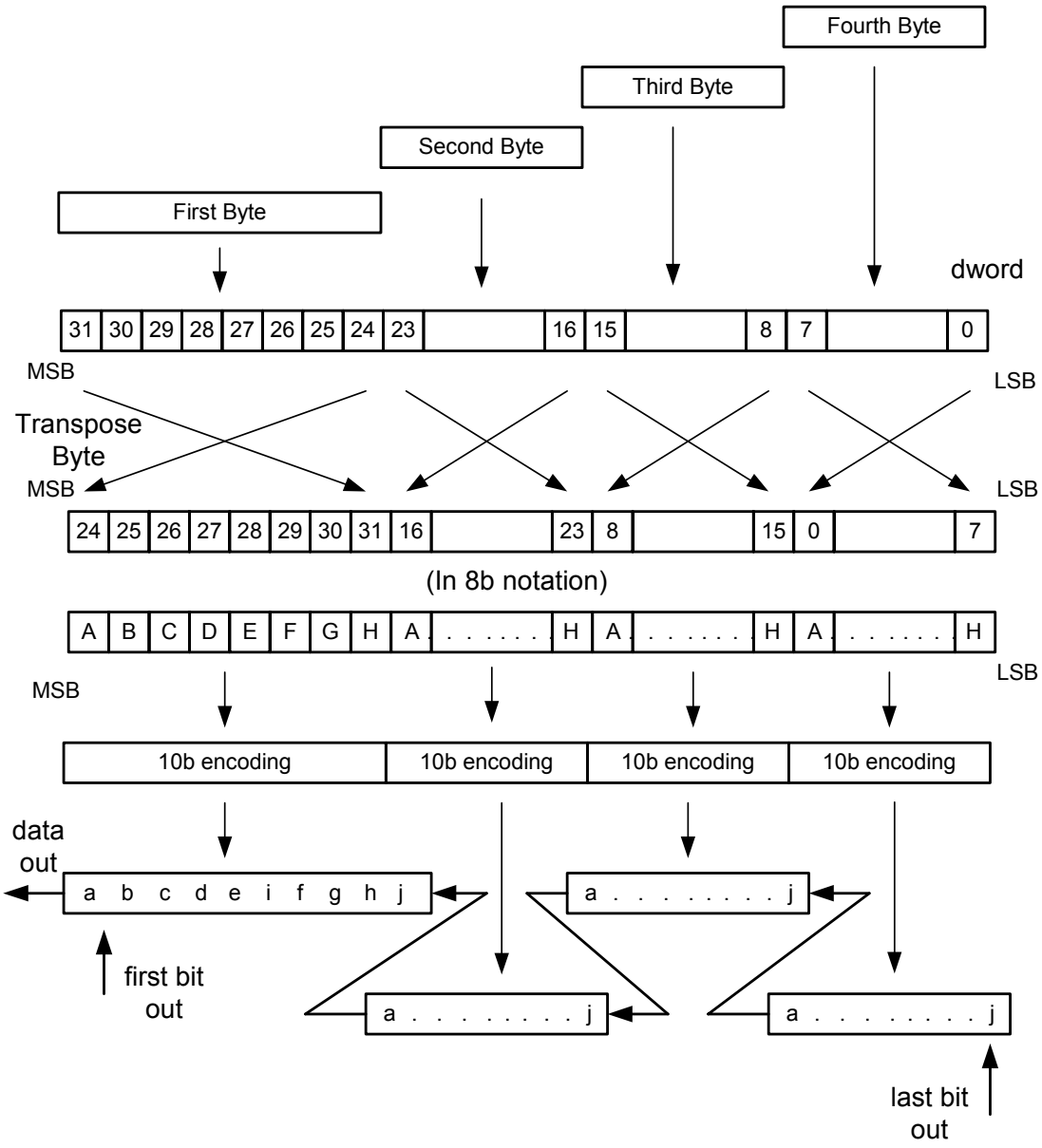

Figure 4 – Bit transmission order

Bit receive order

The receive order of SSP information shown in figure 5.

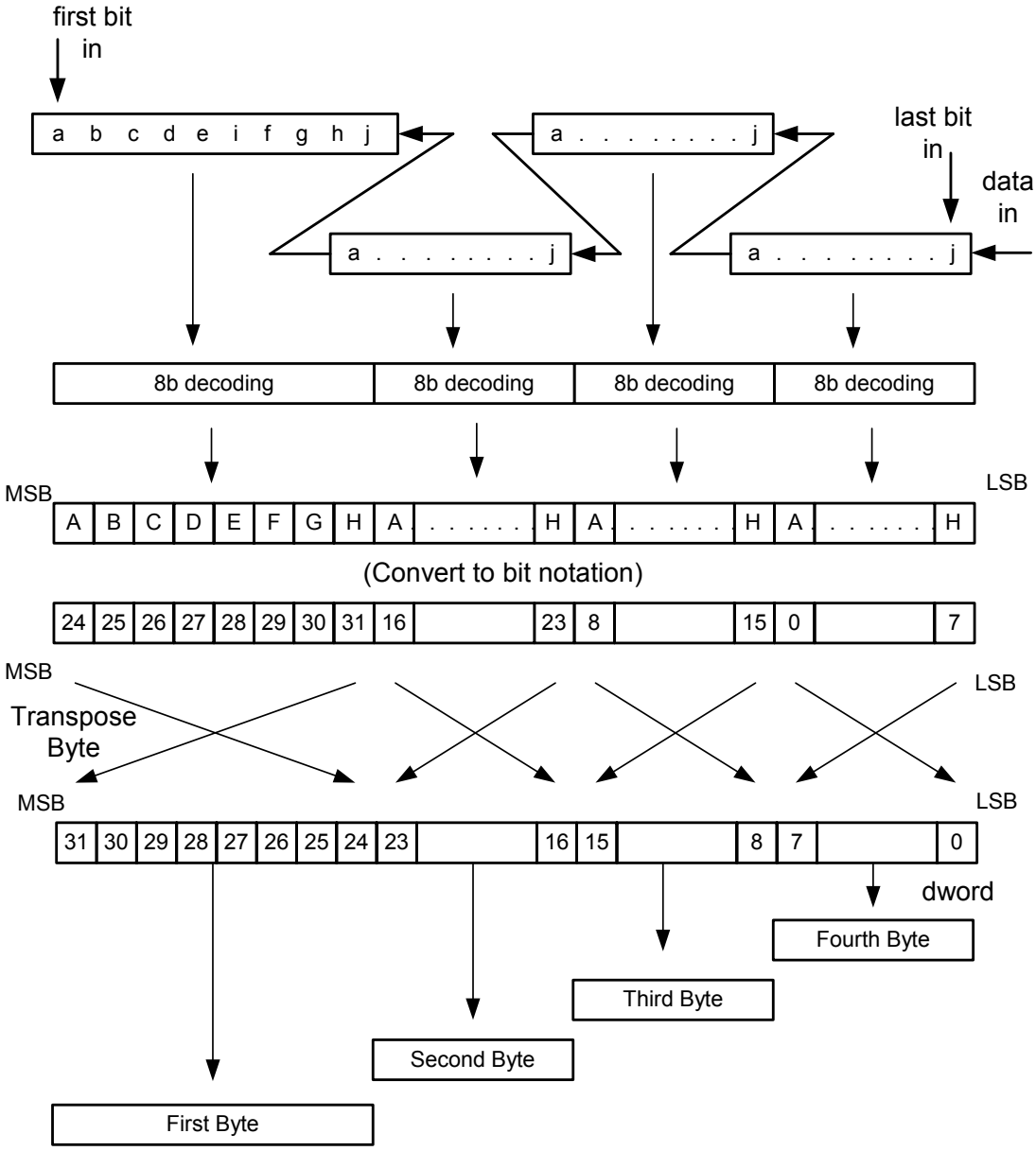

Figure 5 – Bit receive order