To: T10 Technical Committee
From: Rob Elliott, Compaq Computer Corporation (Robert.Elliott@compaq.com)
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Subject: T10/02-145r0 SPC-3 AERC clarification

Revision History
Revision 0 (16 April 2002) first revision

Related Documents
spc3r06 - SCSI Primary Commands - 3 revision 6

Overview
An email by Kenneth Craig on the T10 list (28 March 2002) indicated the AERC bit description is confusing.

The intention is to identify which processor devices can receive AERs (with SEND commands), not which target devices can generate AERs (by whatever method the protocol supports). The latter can be determined by checking if any of the three Control mode page AER bits are changeable.

A processor device type cannot itself generate AERs, because it does not define support for the Control mode page.

Suggested Changes
7.4.2 Standard INQUIRY data

~~The asynchronous event reporting capability (AERC) bit indicates that the target supports the asynchronous event reporting capability as defined in SAM-2. The AERC bit is qualified by the PERIPHERAL DEVICE TYPE field as follows:~~
~~a) Processor device-type definition: An AERC bit of one indicates that the processor device is capable of accepting asynchronous event reports. An AERC bit of zero indicates that the processor device does not support asynchronous event reports; or~~
~~b) All other device-types: This bit is reserved.~~

~~Details of the asynchronous event reporting support are protocol specific.~~

An asynchronous event reporting capability (AERC) bit of one indicates the logical unit is a processor device (see table 59) and supports receiving asynchronous event reports with the SEND command (see 10.3). An AERC bit of zero indicates the logical unit is either not a processor device or it does not support receiving asynchronous event reports with the SEND command.