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SSC-2 Proposal

Explicit Address Write Sequence Ordering

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Introduction

Background

SSC-2 includes explicit addressing commands. From HP's point of view, these commands justify their existence by providing a greater level of data integrity assurance to backup applications and users. The transition of streaming serial devices from direct connect to SAN and long-haul configurations expands the set of possible order and timing combinations for the delivery of commands and data.

HP believes that the existing model for the explicit write commands (i.e., Erase(16), Write(16), and Write Filemarks(16)) does not guarantee data integrity under a number of conditions.

Objectives

With this proposal, HP seeks to modify the operation of explicit Erase, Write, and Write Filemarks commands, such that the explicit address and other CDB fields (including FCS and LCS) guarantee data integrity in the presence of duplicate, missing, and out of order delivery of tagged write commands by packetized transport layers.

Problems with Current Draft Technical Standard

The draft standard does not address ordering implications for target devices supporting the basic task management model (SAM-2, 7.2):

> b) The device server may reorder the actual processing sequence of tasks in any manner. Any data integrity exposures related to task sequence order shall be explicitly handled by the application client using the appropriate commands.

This omission severely reduces the utility of the explicit command set.

Note: the draft standard also does not address ordering implications for target devices configured for unrestricted reordering (SPC-3, 8.4.6). However, since the Queue Algorithm Modifier field defaults to restricted reordering, this data integrity exposure will only occur after specific intervention by an application client that modifies the Queue Algorithm Modifier value. Since an application client must specifically ask the device to allow the data integrity exposure, it appears reasonable to expect the application clients to manage the exposure through their selection and timing of commands.

Change Concept

Connect tagged write sequences and task management such that, for a target device supporting tagged queuing, a simple tagged write command task for LBA *n* shall not transition from dormant to enabled state until a tagged write command task for LBA *n-1* has transitioned from enabled state to ended state. Hence, the LBA becomes a task management ordering mechanism. It should act in this way only as an inferior ordering criteria for simple tagged write command tasks under the basic task management model or the more general tagged management model with restricted reordering.

Detailed Changes to Draft Technical Standard

4.2.12 Explicit address mode tagged write sequences

For explicit address mode tagged write sequences (see 3.1.64) the following rules shall apply:

a) For a tagged write sequence consisting of more than one command, the FCS bit (see 5.6 or 5.7) shall be set to one in the first command of the tagged write sequence. For all other commands within the tagged write sequence, the FCS bit shall be set to zero;

b) for a tagged write sequence consisting of more than one command, the LCS (see 5.6 or 5.7) shall be set to one in the last command of the tagged write sequence. For all other commands within the tagged write sequence, the LCS bit shall be set to zero;

c) for a tagged write sequence consisting of only one command, the FCS bit and LCS bit shall be set to one;

d) the application client shall not issue a tagged write sequence prior to receiving status for all outstanding read type commands; ~~and~~

e) the application client shall not issue linked commands as part of the tagged write sequence;

f) a WRITE(16) command with the TRANSFER LENGTH field set to zero or a WRITE FILEMARKS(16) command with the IMMED bit set to zero and the transfer length field set to zero shall be issued following an error condition to transition from write capable state to neutral state~~.~~; and

g) if the device server supports the basic task management model (see SAM-2, 7.2 and SPC-3, 7.4.2) or if it has been configured for unrestricted reordering (see SPC-8.4.6), the device server shall not transition a simple tagged task for a WRITE(16) command with LBA *n* from dormant to enabled state until the tagged task for the WRITE(16) command with LBA *n-1* has transitioned from enabled state to ended state (see SAM-2, 7.4).