9 SCSI parallel bus timing

9.1 SCSI parallel bus timing values

See table 28, table 29, table 30, table 31, and table 32 for the SCSI bus timing values. Unless otherwise indicated, the timing measurements for each SCSI device, shown in table 28, shall be calculated from signal conditions existing at that SCSI device's port. The timing characteristics of each signal are described in the following paragraphs. Timing requirements relating to LVD release glitches are defined in 7.3.4.1.

Table 28 - SCSI bus control timing values

Subclause	Timing description	Type	Timing values
9.2.1	Arbitration delay	minimum	2,4 µs
9.2.4	Bus clear delay	maximum	800 ns
9.2.5	Bus free delay	minimum	800 ns
9.2.6	Bus set delay	maximum	1,6 µs
9.2.7	Bus settle delay	minimum	400 ns
9.2.8	Cable skew (note 1)	maximum	4 ns
9.2.21	Data release delay	maximum	400 ns
9.2.22	DIFFSENS voltage filter time	minimum	100 ms
9.2.23	Physical disconnection delay	minimum	200 us
9.2.24	Power on to selection (note 2)	maximum	10 s
9.2.25	QAS arbitration delay	minimum	1000 ns
9.2.26	QAS assertion delay	maximum	200 ns
9.2.27	QAS release delay	maximum	200 ns
9.2.28	QAS non-DATA phase REQ (ACK) period	minimum	50 ns
9.2.41	Reset delay	minimum	200 ns
9.2.42	Reset hold time	minimum	25 µs
9.2.43	Reset to selection (note 2)	maximum	250 ms
9.2.45	Selection abort time	maximum	200 µs
9.2.46	Selection time-out delay (note 2)	minimum	250 ms
9.2.50	System deskew delay	minimum	45 ns

Notes:
1 Cable Skew is measured at each SCSI device connection with the transmitted skew subtracted from the received skew.
2 This is a recommended time. It is not mandatory.

Table 29 - SCSI bus data & information phase ST timing values

Subclause	Timing description	Type	Timing values (note 4)				
			Asynch	Fast-5	Fast-10	Fast-20	Fast-40
9.2.2	ATN transmit setup time	min	90 ns	33 ns	33 ns	21,5 ns	19,25 ns
9.2.3	ATN receive setup time	min	45 ns	17 ns	17 ns	8,5 ns	6,75 ns
9.2.8	Cable skew (note 1)	max	4 ns	4 ns	4 ns	3 ns	2,5 ns
9.2.29	Receive assertion period (note 2)	min	N/A	70 ns	22 ns	11 ns	6,5 ns
9.2.30	Receive hold time (note 2 and note 3)	min	N/A	25 ns	25 ns	11,5 ns	4,75 ns
9.2.33	Receive negation period (note 2)	min	N/A	70 ns	22 ns	11 ns	6,5 ns
9.2.34	Receive setup time (note 2 and note 3)	min	N/A	15 ns	15 ns	6,5 ns	4,75 ns
9.2.29	Receive REQ (ACK) period tolerance	min	N/A	1,1 ns	1,1 ns	1,1 ns	1,1 ns
9.2.47	Signal timing skew	max	8 ns	8 ns	8 ns	5 ns	4,5 ns
9.2.40	REQ (ACK) period	nominal	N/A	200 ns	100 ns	50 ns	25 ns
9.2.54	Transmit assertion period (note 2)	min	N/A	80 ns	30 ns	15 ns	8 ns
9.2.55	Transmit hold time (note 2 and note 3)	min	N/A	53 ns	33 ns	16,5 ns	9,25 ns
9.2.57	Transmit negation period (note 2)	min	N/A	80 ns	30 ns	15 ns	8 ns
9.2.58	Transmit setup time (note 2 and note 3)	min	N/A	23 ns	23 ns	11,5 ns	9,25 ns
9.2.59	Transmit REQ (ACK) period tolerance	max	N/A	1 ns	1 ns	1 ns	1 ns

Notes:
1 Cable skew is measured at each SCSI device connection with the transmitted skew subtracted from the received skew.
2 See 9.3 for measurement points for the timing specifications.
3 See 9.6 for examples of how to calculate setup and hold timing.
4 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.

Table 30 - Miscellaneous SCSI bus data & information phase DT timing values

Subclause	Timing description	Type	Timing Values (note 2)				
			Fast-10	Fast-20	Fast-40	Fast-80	Fast-320
9.2.8	Cable skew (note 1)	max	4 ns	3 ns	2,5 ns	2,5 ns	2,5 ns
9.2.40	REQ (ACK) period	nominal	200 ns	100 ns	50 ns	25 ns	6,25 ns
9.2.44	Residual Skew Error (note 3)	max	N/A	N/A	N/A	N/A	±0,20 ns
9.2.11	De-skewed data valid window (note 4)	min	N/A	N/A	N/A	N/A	±0.032 ns
9.2.48	Skew correction range (note 4)	min	N/A	N/A	N/A	N/A	±3,65 ns (note 5)
9.2.47	Signal timing skew	max	26,8 ns	13,4 ns	6,7 ns	3,35 ns	4,85 ns
9.2.49	Strobe Offset Tolerance	max	N/A	N/A	N/A	N/A	±0,20 ns

Notes:
1 Cable skew is measured at each SCSI device connection with the transmitted skew subtracted from the received skew.
2 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.
3 Calculated assuming timing budget shown in table 33.
4 Measured at the receiver terminal using clean input signals with 500 mV peak amplitude and 1 ns rise and fall time between 20 % and 80 % of the signal.
5 Relative to the REQ (ACK) clocking signal.
6 Fast 160 SCSI devices shall not change timing parameters between training or reset events.

Table 31 - Transmit SCSI bus data & information phase DT timing values

Subclause	Timing description	Type	Timing Values (note 3)				
			Fast-10	Fast-20	Fast-40	Fast-80	Fast-320
9.2.2	ATN transmit setup time	min	48,4 ns	29,2 ns	19,6 ns	14,8 ns	14 ns
9.2.14	Flow control transmit hold time	min	38,4 ns	19,2 ns	9,6 ns	4,8 ns	TBD
9.2.15	Flow control transmit setup time	min	48,4 ns	29,2 ns	19,6 ns	14,8 ns	14 ns
9.2.19	pCRC transmit hold time	min	38,4 ns	19,2 ns	9,6 ns	4,8 ns	N/A
9.2.20	pCRC transmit setup time	min	48,4 ns	29,2 ns	19,6 ns	14,8 ns	N/A
9.2.54	Transmit assertion period (note 1)	min	92 ns	46 ns	23 ns	11,5 ns	2,56 ns
9.2.55	Transmit hold time (note 1 and note 2)	min	38,4 ns	19,2 ns	9,6 ns	4,8 ns	2,47 ns
9.2.56	Transmit ISI Compensation	max	note 4	note 4	note 4	note 4	1,0 ns
9.2.57	Transmit negation period (note 1)	min	92 ns	46 ns	23 ns	11,5 ns	2,47 ns
9.2.59	Transmit REQ (ACK) period tolerance	max	0,6 ns	0,6 ns	0,6 ns	0,6 ns	0,06 ns
9.2.60	Transmit REQ assertion period with P_CRCA transitioning	min	97,5 ns	54 ns	35,5 ns	24 ns	N/A
9.2.61	Transmit REQ negation period with P_CRCA transitioning	min	97,5 ns	54 ns	35,5 ns	24 ns	N/A
9.2.58	Transmit setup time (note 1 and note 2)	min	38,4 ns	19,2 ns	9,6 ns	4,8 ns	(1,28) ns
	Transmitter skew	max	N/A	N/A	N/A	N/A	±0,75 ns
9.2.63	Transmitter time asymmetry	max	N/A	N/A	N/A	N/A	±0,25 ns

Notes:
1 See 9.3 for measurement points for the timing specifications.
2 See 9.6 for examples of how to calculate setup and hold timing.
3 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.
4 Calculated without any ISI compensation.
5 Fast 160 SCSI devices shall not change timing parameters between training or reset events.

Table 32 - Receive SCSI bus data & information phase DT timing values

Subclause	Timing description	Type	Timing Values (note 3)				
			Fast-10	Fast-20	Fast-40	Fast-80	Fast-320
9.2.3	ATN receive setup time	min	13,6 ns	7,8 ns	4,9 ns	3,45 ns	3 ns
9.2.12	Flow control receive hold time	min	11,6 ns	5,8 ns	2,9 ns	1,45 ns	3 ns
9.2.13	Flow control receive setup time	min	18,6 ns	12,8 ns	9,9 ns	8,45 ns	3 ns
9.2.17	pCRC receive hold time	min	11,6 ns	5,8 ns	2,9 ns	1,45 ns	N/A
9.2.18	pCRC receive setup time	min	18,6 ns	12,8 ns	9,9 ns	8,45 ns	N/A
9.2.29	Receive assertion period (note 1)	min	80 ns	40 ns	20 ns	8,5 ns	TBD
9.2.30	Receive hold time (note 1 and note 2)	min	11,6 ns	5,8 ns	2,9 ns	1,45 ns	TBD
9.2.33	Receive negation period (note 1)	min	80 ns	40 ns	20 ns	8,5 ns	TBD
9.2.34	Receive setup time (note 1 and note 2)	min	11,6 ns	5,8 ns	2,9 ns	1,45 ns	TBD
9.2.35	Receive REQ (ACK) period tolerance	min	0,7 ns	0,7 ns	0,7 ns	0,7 ns	0,06 ns
9.2.36	Receive REQ assertion period with P_CRCA transitioning	min	85,5 ns	48 ns	32,5 ns	21 ns	N/A
9.2.37	Receive REQ negation period with P_CRCA transitioning	min	85,5 ns	48 ns	32,5 ns	21 ns	N/A
9.2.38	Receive Skew Compensation	max	N/A	N/A	N/A	N/A	4,4 ns
9.2.31	Receive Internal Hold Time (note 4)	min	N/A	N/A	N/A	N/A	0,032 ns
9.2.32	Receive Internal Setup Time (note 4)	min	N/A	N/A	N/A	N/A	0,032 ns

Notes:
1 See 9.3 for measurement points for the timing specifications.
2 See 9.6 for examples of how to calculate setup and hold timing.
3 SCSI bus timing values specified by the maximum transfer rate for the given range shall apply even if a slower transfer rate within the given range is negotiated.
4 Calculated assuming timing budget shown in table 33.
5 Fast 160 SCSI devices shall not change timing parameters between training or reset events.

Table 33 - SCSI Fast-160 / Fast-320 timing budget template

Item	Fast-160	Fast-320	Comments
Nominals:			
REQ(ACK) Period	12,5 ns	6,25 ns	from table 30
Transfer period	6,25 ns	3,125 ns	REQ/ACK period / 2
Ideal Setup/Hold	3,125 ns	1,526 ns	REQ/ACK period / 4
Non-Compensatable (Early to Late):			**Worse case total of + and - time shift unless otherwise noted**
REQ(ACK) period tolerance / 2	0,06 ns	0,06 ns	Tolerance of transmitter plus measurement error (note 1)
Driver time asymmetry	0,50 ns	0,00 ns	Compensatable in Fast-320
Receiver time asymmetry	0,35 ns	0,00 ns	Compensatable in Fast-320
System noise at launch	0,25 ns	0,20 ns	Time impact (Requires tighter system performance)
System noise at receiver	0,25 ns	0,20 ns	Time impact (Requires tighter system performance)
Near end Crosstalk	0,7 ns	0,5 ns	Time impact (Requires PIP cable concessions)
Chip noise in receiver	0,2 ns	0,2 ns	
Receiver amplitude time skew	0,2 ns	0,0 ns	With minimum signals (Compensatable in Fast-320)
Clock jitter	0,25 ns	0,25 ns	
Strobe offset tolerance	0,5 ns	0,20 ns	Accuracy of centering strobe
Residual Skew error	0,3 ns	0,20 ns	After skew compensation
Non-Compensatable total:	**3,56 ns**	**1,81 ns**	
Compensatable:			**Worst Case**
Offset induced time asymmetry	0,0 ns	0,80 ns	Timing impact from cumulative DC offsets at receiver
Driver time asymmetry	0,0 ns	0,50 ns	
Receiver time asymmetry	0,0 ns	0,35 ns	
Receiver amplitude time skew	0,0 ns	0,2 ns	
Transmitter chip skew	0,75 ns	0,75 ns	
Receiver chip skew	0,75 ns	0,75 ns	
Cable skew	2,5 ns	2,5 ns	
Two times trace skew	0,4 ns	0,4 ns	Total for SCSI device pair
ISI of data	4,0 ns	4,0 ns	Worse case pattern
ISI of REQ(ACK)	0,0 ns	0,0 ns	Post preamble
May detect to shall detect ambiguity	0,0 ns	0,0 ns	Assumed to be negligible in given chip
Compensatable total:	**8,4 ns**	**10,25 ns**	
Assumed Compensation			
ISI Compensation	2,0 ns	3,0 ns	Assumes 50%(Fast-160), 75% (Fast-320) corrected
Skew compensation	4,4 ns	4,4 ns	Internal alignment of data signals to REQ or ACK
Symmetry correction	0,0 ns	0,85 ns	Deskew of both asserting and negating edges

Table 33 - SCSI Fast-160 / Fast-320 timing budget template

Item	Fast-160	Fast-320	Comments
Amplitude normalization	0,0 ns	0,15 ns	Assumes 75% of receiver amplitude time skew error
Offset correction	0,0 ns	0,60 ns	75% of worst case offset corrected
Compensation total:	**6,4 ns**	**9,00 ns**	
Total Error Inputs:	**11,96 ns**	**12,06 ns**	**Sum of compensatable and non-compensatable timings**
Post compensation error:	**5,56 ns**	**3,06 ns**	**Total error inputs - compensation total**
Minimum compensated internal setup (int) data valid window	**0,345 ns**	**0,032 ns**	**(transfer period - post compensation error) / 2 note 2**
Minimum compensated internal hold (int) data valid window	**0,345 ns**	**0,032 ns**	**(transfer period - post compensation error) / 2 note 2**

Notes:
1 Tolerance adjusted for half cycle (transfer period)
2 Timing budgets in previous standards neglected asymmetry & detection ambiguity and lumps chip noise, clock jitter, cross-talk, noise, ISI and receiver amplitude skew into other terms (e.g., signal distortion skew) and/or ignores the effects.

9.2 Timing description

9.2.1 Arbitration delay

The minimum time a SCSI device shall wait from asserting the BSY signal for arbitration until the DATA BUS is examined to see if arbitration has been won (see 10.5). There is no maximum time.

9.2.2 ATN transmit setup time

When data group transfers are being used with asynchronous transfers or synchronous transfers, the ATN transmit setup time is the minimum time provided by the transmitter between the assertion of the ATN signal and the last negation of the ACK signal in any phase.

When information unit transfers are being used with asynchronous transfers or synchronous transfers, the ATN transmit setup time is the minimum time provided by the transmitter between the assertion of the ATN signal and the negation of the ACK signal corresponding to the last iuCRC transfer of an information unit.

When information unit transfers are being used with paced transfers, the ATN transmit setup time is the minimum time provided by the transmitter between the assertion of the ATN signal and the assertion of the ACK signal corresponding to the last iuCRC transfer of an information unit.

Specified to provide the increased ATN receive setup time, subject to intersymbol interference, cable skew, and other distortions.

9.2.3 ATN receive setup time

When data group transfers are being used with asynchronous transfers or synchronous transfers, the ATN receive setup time is the minimum time required at the receiver between the assertion of the ATN signal and the last negation of the ACK signal in any phase to recognize the assertion of an attention condition.

When information unit transfers are being used with asynchronous transfers or synchronous transfers, the ATN receive setup time is the minimum time required at the receiver between the assertion of the ATN signal and the negation of the ACK signal corresponding to the last iuCRC transfer of an information unit to

recognize the assertion of an attention condition.

When information unit transfers are being used with paced transfers, the ATN receive setup time is the minimum time required at the receiver between the assertion of the ATN signal and the assertion of the ACK signal corresponding to the last iuCRC transfer of an information unit to recognize the assertion of an attention condition.

9.2.4 Bus clear delay

The maximum time for a SCSI device to release all SCSI bus signals after:

a) the BUS FREE phase is detected (the BSY and SEL signals are both false for a bus settle delay);
b) the SEL signal is received from another SCSI device during the ARBITRATION phase;
c) the transition of the RST signal to true.

For item a) above, the maximum time for a SCSI device to release all SCSI bus signals is 1200 ns from the BSY and SEL signals first becoming both false. If a SCSI device requires more than a bus settle delay to detect BUS FREE phase, it shall release all SCSI bus signals within a bus clear delay minus the excess time.

9.2.5 Bus free delay

The minimum time that a SCSI device shall wait from its detection of the BUS FREE phase (BSY and SEL both false for a bus settle delay) until its assertion of the BSY signal in preparation for entering the ARBITRATION phase.

9.2.6 Bus set delay

The maximum time for a SCSI device to assert the BSY signal and its SCSI ID after it detects a BUS FREE phase for the purpose of entering the ARBITRATION phase.

9.2.7 Bus settle delay

The minimum time to wait for the bus to settle after changing certain control signals as called out in the protocol definitions.

Provides time for a signal transition to propagate from the driver to the terminator and back to the driver.

9.2.8 Cable skew

The maximum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices excluding any signal distortion skew delays.

9.2.9 Chip noise in receiver

The maximum transition to transition time shift due to the internal physics of the receiving SCSI device circuitry.

9.2.10 Clock jitter

The maximum transition to transition time shift of SCSI bus signals caused by short term variations in the transmitting SCSI device’s clock.

9.2.11 De-skewed data valid window

The minimum difference in time allowed between the rising or falling edge of a “1010…” pattern on the DATA BUS or DB(P1) and its clocking signal on the ACK or REQ signal as measured at their zero-crossing

points after skew compensation is applied by the receiver without allowing any error in the received data (see figure 46). The de-skewed data valid window shall be equal to:

± [(data transfer period) - (residual skew error) - (strobe offset tolerance) - (clock jitter) - (receiver amplitude skew) - (chip noise) - (system noise at receiver) - (receiver asymmetry)] / 2.

~~**Editors Note 2 - GOP: Should P_CRCA be added into this description?**~~

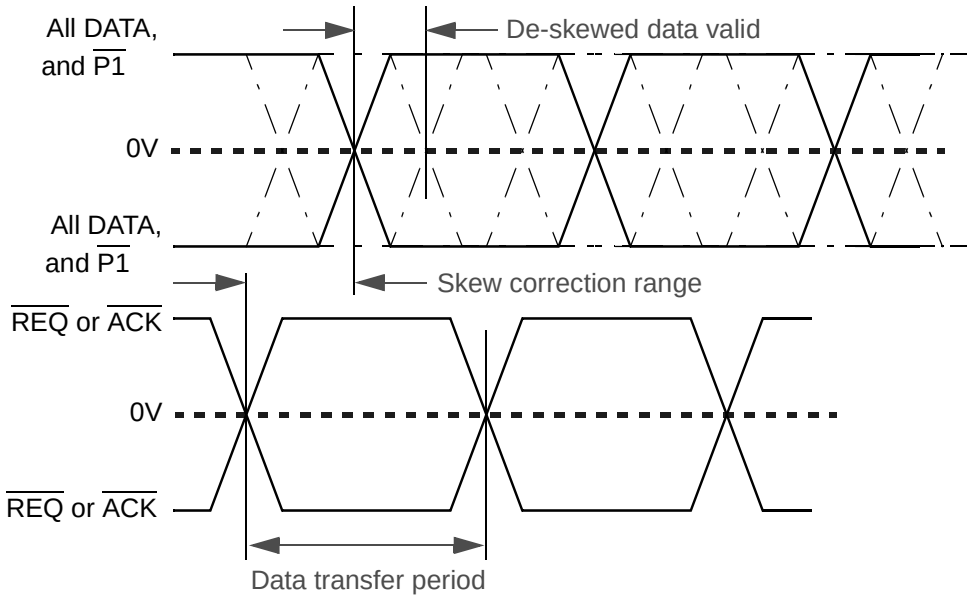

Figure 46 - Receiver de-skew parameters

9.2.12 Flow control receive hold time

The maximum time required by the initiator between the assertion of the REQ signal corresponding to the last iuCRC transfer of a SPI data streaming information unit and the changing of the P_CRCA signal.

Specified to ease receiver timing requirements.

9.2.13 Flow control receive setup time

The maximum time required by the initiator between the assertion of the P_CRCA signal and the assertion of the REQ signal corresponding to the last iuCRC transfer of a SPI data streaming information unit. Also, the maximum time required by the initiator between the negation of the P_CRCA signal and the assertion of the REQ signal corresponding to any valid data transfer of a SPI L_Q information unit.

Specified to ease receiver timing requirements.

9.2.14 Flow control transmit hold time

The minimum time provided by the target between the assertion of the REQ signal corresponding to the last iuCRC transfer of a SPI data streaming information unit and the changing of the P_CRCA signal.

Specified to provide the increased P_CRCA receive setup time, subject to intersymbol interference, cable

skew, and other distortions.

9.2.15 Flow control transmit setup time

The minimum time provided by the target between the assertion of the P_CRCA signal and the assertion of the REQ signal corresponding to the last iuCRC transfer of a SPI data streaming information unit. Also, the minimum time provided by the target between the negation of the P_CRCA signal and the assertion of the REQ signal corresponding to any valid data transfer of a SPI L_Q information unit.

Specified to provide the increased P_CRCA receive setup time, subject to intersymbol interference, cable skew, and other distortions.

9.2.16 Offset induced time asymmetry

Time symmetry error created by the cumulative sum of all offset errors seen by the receiver. This includes non-symmetrical transmitter drive plus terminator current mismatch, receiver offset, and IR drop within the cable or backplane.

9.2.17 pCRC receive hold time

The minimum time required at the receiver between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled (see 16.3.12).

9.2.18 pCRC receive setup time

The minimum time required at the receiver between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled (see 16.3.12).

Specified to ease receiver timing requirements and ensure that this signal, which is outside CRC protection, is received correctly.

9.2.19 pCRC transmit hold time

The minimum time provided by the transmitter between the transition of the REQ signal and the transition of the P_CRCA signal while pCRC protection is enabled (see 16.3.12).

9.2.20 pCRC transmit setup time

The minimum time provided by the transmitter between the transition of the P_CRCA signal and the transition of the REQ signal while pCRC protection is enabled (see 16.3.12).

Specified to provide the increased receive setup time, subject to intersymbol interference, cable skew, and other distortions.

9.2.21 Data release delay

The maximum time for an initiator to release the DATA BUS, DB(P_CRCA), and/or DB(P1) signals, following the transition of the I/O signal from false to true.

9.2.22 DIFFSENS voltage filter time

The minimum time DIFFSENS voltage shall be sensed continuously within the voltage range of a valid SCSI bus mode.

9.2.23 Physical disconnection delay

The minimum time that a target shall wait after releasing BSY before participating in an ARBITRATION

phase when honoring a DISCONNECT message from the initiator.

9.2.24 Power on to selection

The recommended maximum time from power application until a SCSI target is able to respond with appropriate status and sense data to the TEST UNIT READY, INQUIRY, and REQUEST SENSE commands (See SCSI Primary Commands-2 standard).

9.2.25 QAS arbitration delay

The minimum time a SCSI device with QAS enabled (see 16.3.12) shall wait from the detection of the MSG, C/D, and I/O signals being false to start QAS until the DATA BUS is examined to see if QAS has been won (see 10.5).

9.2.26 QAS assertion delay

The maximum time allowed for a SCSI device to assert certain signals during QAS.

9.2.27 QAS release delay

The maximum time allowed for a SCSI device to release certain signals during QAS.

9.2.28 QAS non-DATA phase REQ (ACK) period

The minimum time a QAS-capable initiator shall ensure the REQ and ACK signals are asserted and that data is valid during COMMAND, MESSAGE, and STATUS phases.

9.2.29 Receive assertion period

The minimum time provided at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous transfers, provided P_CRCA is not transitioning with pCRC protection enabled (see 16.3.12). Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 0,8 V level. For SE fast-20 operation the period is measured at the 1,0 V level. For LVD see figure 51 and figure 52 for signal measurement points.

9.2.30 Receive hold time

For ST data transfers the minimum time provided at the receiving SCSI device between the assertion of the REQ signal or the ACK signals and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous transfers, provided P_CRCA is not transitioning with pCRC protection enabled (see 16.3.12). For DT data transfers the minimum time required at the receiving SCSI device between the transition (i.e. assertion or negation) of the REQ signal or the ACK signals and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous transfers.

9.2.31 Receive internal hold time

The minimum time provided for hold time in the receive data detector after allowance for timing errors and timing compensation from all sources measured from the worse case bit (i.e., data or parity) to the compensated offset strobe.

NOTE 21 - This time may not be observable to other than the SCSI device designer.

9.2.32 Receive internal setup time

The minimum time provided for setup time in the receive data detector after allowance for timing errors and timing compensation from all sources measured from the worse case bit (i.e., data or parity) to the

compensated offset strobe.

NOTE 22 - This time may not be observable to other than the SCSI device designer.

9.2.33 Receive negation period

The minimum time required at a SCSI device receiving a REQ signal for the signal to be negated while using synchronous transfers. Also, the minimum time required at a SCSI device receiving an ACK signal for the signal to be asserted while using synchronous transfers. For SE fast-5 and fast-10 operation, the time period is measured at the 2,0 V level. For SE fast-20 operation the period is measured at the 1,9 V level. For LVD see figure 51 and figure 52 for signal measurement points.

9.2.34 Receive setup time

For ST data transfers the minimum time provided at the receiving SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the assertion of the REQ signal or the ACK signal while using synchronous transfers. For DT data transfers the minimum time required at the receiving SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the transition of the REQ signal or the ACK signal while using synchronous transfers.

9.2.35 Receive REQ (ACK) period tolerance

The minimum tolerance that a SCSI device shall allow to be subtracted from the REQ (ACK) period. The tolerance comprises the transmit REQ (ACK) tolerance plus a measurement error due to noise.

9.2.36 Receive REQ assertion period with P_CRCA transitioning

The minimum time required at a SCSI device receiving a REQ signal for the signal to be asserted while using synchronous transfers with P_CRCA transitioning with pCRC protection enabled (see 16.3.12).

Specified to ensure that the assertion period is longer than the receive hold time plus the receive setup time.

9.2.37 Receive REQ negation period with P_CRCA transitioning

The minimum time required at a SCSI device receiving a REQ signal for the signal to be negated while using synchronous transfers with P_CRCA transitioning with pCRC protection enabled (see 16.3.12).

Specified to ensure that the negation period is longer than the receive hold time plus the receive setup time.

9.2.38 Receive Skew Compensation

The effective reduction in worse case timing skew of data, parity, and strobe signals provided by the receiving SCSI device but not directly observable at the receiving SCSI device connector.

9.2.39 Receiver amplitude time skew

The maximum time shift of SCSI bus signals caused by the difference in receiver switching delay of a minimum amplitude signal versus a maximum amplitude signal.

9.2.40 REQ (ACK) period

The REQ (ACK) period during synchronous transfers, specified in table 29 for ST DATA phases and in table 30 for DT DATA phases, is the nominal time between adjacent assertion edges of the REQ or ACK signal for the fastest negotiated data transfer rate. For the purpose of calculating the actual REQ (ACK) period tolerance the REQ (ACK) period should be measured without interruptions (e.g., offsets pauses). To

minimize the impact of cross-talk and ISI the measurements should be made by averaging the time between edges during long (i.e., greater than 512 bytes) all zero or all ones data transfers and by ignoring the first and last 10 transitions.

In DT DATA phases the negotiated transfer period for data is half of the REQ (ACK) period since data is qualified on both the assertion and negation edges of the REQ or ACK signal. In ST DATA phases the negotiated transfer period for data is equal to the REQ (ACK) period during synchronous transfers since data is only qualified on the assertion edge of the REQ or ACK signal.

9.2.41 Reset delay

The minimum time that the RST signal shall be continuously true before the SCSI device shall initiate a reset.

9.2.42 Reset hold time

The minimum time that the RST signal is asserted. There is no maximum time.

9.2.43 Reset to selection

The recommended maximum time from after a reset condition until a SCSI target is able to respond with appropriate status and sense data to the TEST UNIT READY, INQUIRY, and REQUEST SENSE commands (See SCSI Primary Commands-2 standard).

9.2.44 Residual skew error

The maximum timing error between the deskewed data and REQ or ACK internal to the receiving SCSI device after skew compensation.

9.2.45 Selection abort time

The maximum time that a SCSI device shall take from its most recent detection of being selected or reselected until asserting the BSY signal in response. This time-out is required to ensure that a target or initiator does not assert the BSY signal after a SELECTION or RESELECTION phase has been aborted.

9.2.46 Selection time-out delay

The minimum time that an initiator or target should wait for the assertion of the BSY signal during the SELECTION or RESELECTION phase before starting the time-out procedure. Note that this is only a recommended time period.

9.2.47 Signal timing skew

The maximum signal timing skew occurs when transferring random data and in combination with interruptions of the REQ or ACK signal transitions (e.g., pauses caused by offsets). The signal timing skew includes cable skew (measured with 0101... patterns) and signal distortion skew caused by random data patterns and transmission line reflections as shown in figure 49, figure 50, figure 51, and figure 52.

The receiver detection range is the part of the signal between the "may detect" level and the "shall detect" level on either edge. (see 9.3)

NOTE 23 - For timing budget purposes the value stated in table 30 is calculated without the benefit of skew compensation.

9.2.48 Skew correction range

The minimum skew correction capability of the receiver of a signal on the DATA BUS or DB(P1) relative to

the ACK or REQ signal as measured at the receiver's connector. The skew correction range shall be equal to ± [(transmitter chip skew) + (cable skew) + (two times trace skew)] relative to the corresponding ACK or REQ clock signal for that transition. Receiver chip skew is not included, as it is internal to the receiver.

9.2.49 Strobe offset tolerance

The time tolerance of centering the compensated REQ or ACK strobe in the transfer period during the training pattern.

9.2.50 System deskew delay

The minimum time that a SCSI device should wait after receiving a SCSI signal to ensure that any signals transmitted at the same time are valid. The system deskew delay shall not be applied to the synchronous transfers.

9.2.51 System noise at launch

The maximum time shift of SCSI bus signals caused by system noise at the transmitter (e.g., noise caused by current changes in the voice coil) measured at the transmitting SCSI device connector.

9.2.52 System noise at receiver

The maximum time shift of SCSI bus signals caused by system noise at the receiver (e.g., noise caused by current changes in the voice coil) measured at the receiving SCSI device connector not including the time shift from the system noise at launch.

9.2.53 Time asymmetry

The maximum time difference between the asserted and negated signal for data, REQ, or ACK transitions that are intended to be equidistant.

9.2.54 Transmit assertion period

The minimum time that a target shall assert the REQ signal while using synchronous transfers, provided it is not transitioning P_CRCA with pCRC protection enabled (see 16.3.12). Also, the minimum time that an initiator shall assert the ACK signal while using synchronous transfers.

9.2.55 Transmit hold time

For ST data transfers the minimum time provided by the transmitting SCSI device between the assertion of the REQ signal or the ACK signal and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous transfers. For DT data transfers the minimum time provided by the transmitting SCSI device between the transition of the REQ signal or the ACK signal and the changing of the DATA BUS, DB(P_CRCA), and/or DB(P1) signals while using synchronous transfers.

9.2.56 Transmit ISI Compensation

The effective reduction in worse case ISI timing shift provided by the transmitting SCSI device as seen at the receiving SCSI device connector.

9.2.57 Transmit negation period

The minimum time that a target shall negate the REQ signal while using synchronous transfers, provided it is not transitioning P_CRCA with pCRC protection enabled (see 16.3.12). Also, the minimum time that an initiator shall negate the ACK signal while using synchronous transfers.

9.2.58 Transmit setup time

For ST data transfers the minimum time provided by the transmitting SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the assertion of the REQ signal or the ACK signal while using synchronous transfers. For DT data transfers the minimum time provided by the transmitting SCSI device between the changing of DATA BUS, DB(P_CRCA), and/or DB(P1) signals and the transition of the REQ signal or the ACK signal while using synchronous transfers.

9.2.59 Transmit REQ (ACK) period tolerance

The maximum tolerance that a SCSI device may subtract from the REQ (ACK) period.

9.2.60 Transmit REQ assertion period with P_CRCA transitioning

The minimum time that a target shall assert the REQ signal during a synchronous transfer DT DATA phase while transitioning P_CRCA with pCRC protection enabled (see 16.3.12).

Specified to provide the increased receive REQ assertion period, subject to loss on the interconnect.

9.2.61 Transmit REQ negation period with P_CRCA transitioning

The minimum time that a target shall negate the REQ signal during a synchronous transfer DT DATA phase while transitioning P_CRCA with pCRC protection enabled (see 16.3.12).

Specified to provide the increased receive REQ negation period, subject to loss on the interconnect.