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To: **T10 Parallel SCSI Working Group**
From: **Russ Brown**
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Date: ~~**22 February**~~**12 March 2002**

Subject: Proposal for Offset Correction for Ultra640 SCSI for SPI-5

Introduction

As described in T10/02-038r0, applying DC offset correction at the receiver provides significant improvement in timing margin. Because of this improvement, we propose that this feature be mandatory for Ultra640 SCSI. The following identifies where changes need to be made in SPI-5 to implement this proposal. The changes in revision 1 are identified by revision marks.

In A.3.2 Receiver steady state input voltage requirements:

Make the text in the existing clause into subclause A.3.2.1 Steady state input voltage requirements for Fast160 and slower LVD receivers, and, add subclause A.3.2.2 Steady state input voltage requirements for Fast320 LVD receivers. The content for this new subclause is as follows:

A.3.2.2 Steady state input voltage requirements for Fast320 LVD receivers

Table A.x and Figure A.y define the voltages for the requirements in this subclause. This subclause places requirements on receivers only and does not change input signal requirements.

The differential offset component of the receiver input voltage is defined as:

$V_{RXOFFSET} = (|V_N| - |V_A|) / 2$

where $|V_A|$ and $|V_N|$ are the steady state differential Asserted and Negated signal levels applied to the receiver, measured after 100 ns assertion (negation) of the signal.

Within the common-mode input voltage range (V_{CM}), of 0,845 V < V_{CM} < 1,655 V (see table A.7) and after calibration on a training pattern containing a differential offset voltage component, $V_{RXOFFSET}$, a Fast320 receiver shall detect assertion and negation with V_{IN} in the ranges shown in Table A.x, and over an input signal offset range of –75 mV < $V_{RXOFFSET}$ < +75 mV (see figure A.11 for the test circuit for V_{IN}).

Table A.x - Fast320 receiver steady state input voltage ranges

	Minimum	Maximum
Correctable input signal offset ($V_{RXOFFSET}$) range		+/- 75 mV
V_{IN} to detect Assertion (after training)	-3.6 V	$V_{RXOFFSET}$ – 20 mV
V_{IN} to detect Negation (after training)	$V_{RXOFFSET}$ + 20 mV	3.6 V

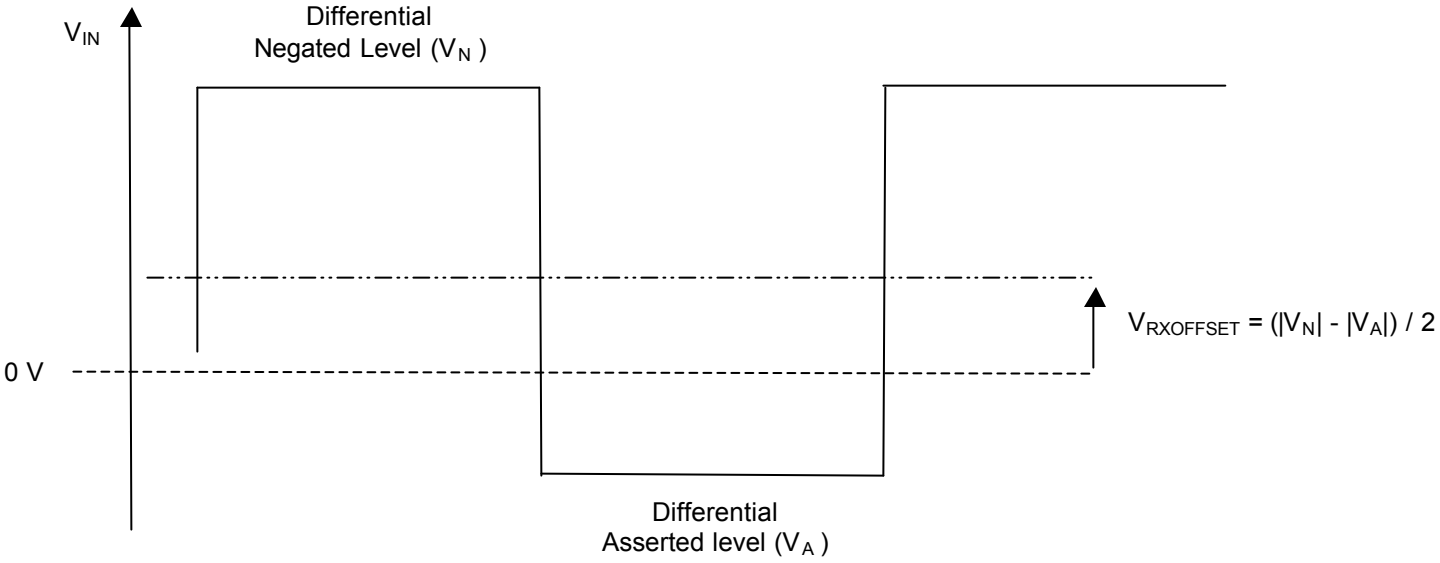

Figure A.y - Input Signal Offset Component $V_{RXOFFSET}$