SCSI Signal Path Tr/Tf Asymmetries

Typical Signal Path Block Diagram:

- LVD Transmitter
- LVD Receiver
- Cable Backplane
- Deskew Circuits
- Buffers, Level Translators, etc.
- Receiver, comparator
- 320MHz Clk
- Data
- Ack (Req)
T10/02-045r0

Method to Reduce Driver/Receiver Asymmetry Induced Timing Errors

CASE 1: Uncorrected duty cycle errors. Align rising Data to rising Clk

ACK (REQ)
Strobes placed T/2 after Clk edges
Data after aligning data rising to Clk rising

CASE 2: Corrected duty cycle errors. Align rising and falling Data to Clk

Duty-Cycle Corrected ACK (REQ)
Strobes placed T/2 after Clk edges
Data after aligning both rising and falling Data edges to Clk

Ideal Cell Boundaries referenced to ACK (REQ) Rising Edge

T = 3.125ns

Reduced Setup / Hold Margins due to Clk and Data asymmetries

Clk Duty Cycle Error

Data Duty Cycle Error

Data Falling Edge Correction

Strobes centred in Data window after double de-skew corrects asymmetries. No loss of Setup / Hold time
Method to Reduce Driver/Receiver Asymmetry Induced Timing Errors

Perform the following steps:

- Deskew asserting data edges to asserting clock edge.
- Deskew negating data edges to asserting clock edge.
- Combine both deskewed signals to generate corrected data.
- Correct clock asymmetries.
- Use Corrected clock and set strobes to 1/2 of the bit period.

Possible budget improvement of 1000pS+
From SPI-4 Table 44

- TX Asymmetry ± 250pS
- Receiver chip skew 750pS (Asymmetry portion only)