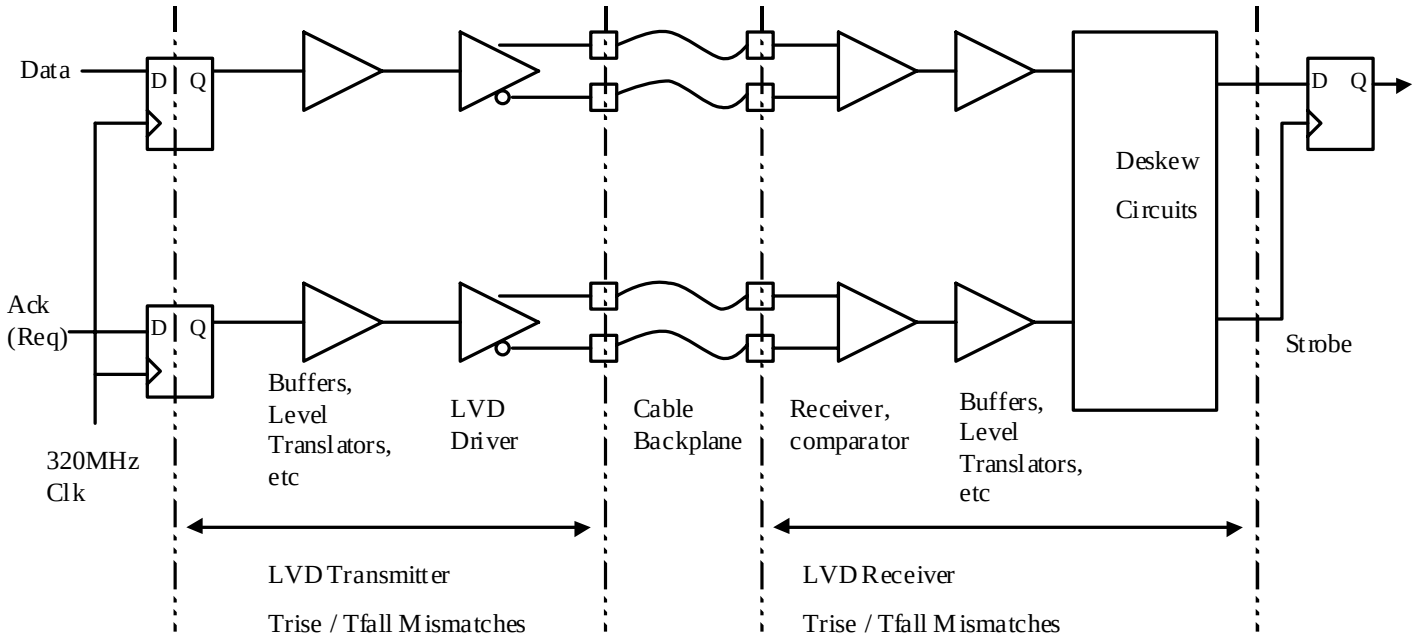
Method to Reduce Driver/Receiver Asymmetry Induced Timing Errors

SCSI Signal Path Tr/Tf Asymmetries

Typical Signal Path Block Diagram:



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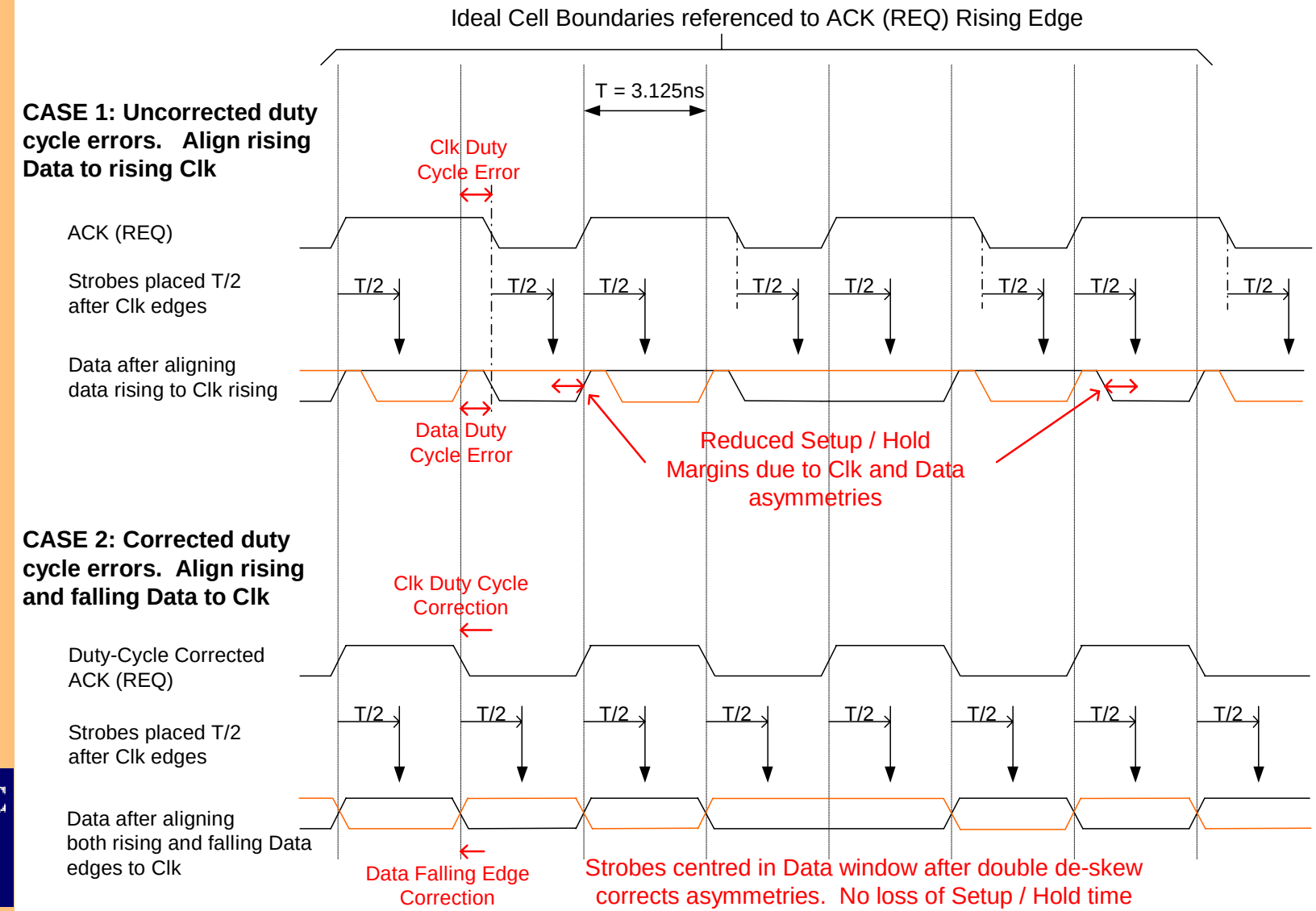
Method to Reduce Driver/Receiver Asymmetry Induced Timing Errors

CASE 1: Uncorrected duty cycle errors. Align rising Data to rising Clk

CASE 2: Corrected duty cycle errors. Align rising and falling Data to Clk



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Method to Reduce Driver/Receiver Asymmetry Induced Timing Errors

Perform the following steps:

- Deskew asserting data edges to asserting clock edge.
- Deskew negating data edges to asserting clock edge.
- Combine both deskewed signals to generate corrected data.
- Correct clock asymmetries.
- Use Corrected clock and set strobes to 1/2 of of bit period.

Possible budget improvement of 1000pS+

From SPI-4 Table 44

- TX Asymmetry ± 250pS
- Receiver chip skew 750pS (Asymmetry portion only)

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