

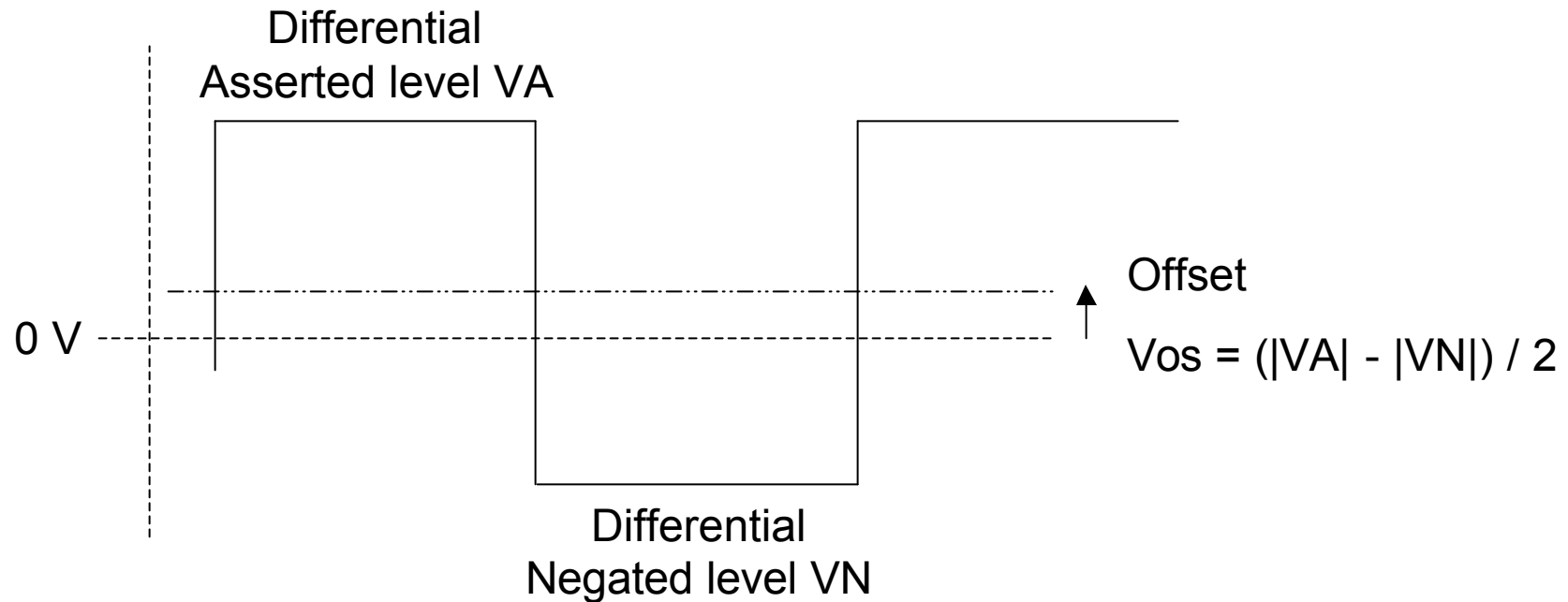
T10/02-038r0



# Ultra640 SCSI Receiver Offset Issues

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## Differential Offset at the LVD Receiver Input



- Differential offset is the difference between the absolute value of an asserted signal measured from zero volts and the absolute value of a negated signal measured from zero volts divided by two.
- For optimum vertical eye margin, the detection threshold should be set midway between the asserted and negated signal levels at the receiver.
- Several system errors add to offset this mid-point away from zero volts differential at the receiver.

## DC Offset Issues with LVD SCSI

- The total DC Offset Error at a SCSI LVD receiver input is the sum of several system errors, the major terms being:
  - Driver unbalance
  - Terminator tolerances
  - Receiver internal offset errors
  - Bias cancellation errors due to interconnect IR drops
- Offset causes signal asymmetry at the receiver
  - The resulting timing margin degradation is very significant for U640
  - This timing loss is not completely covered in the present timing budget
  - Offset amplitude loss was included in the Ultra320 eye masks
- Total offset can be detected and corrected at the receiver using the existing training pattern to avoid this loss of timing margin
  - This is worth doing for Ultra640 because timing budget is very tight

## Major DC Offset Error Terms: (reference SPI-4)

### 1) Driver unbalance: ref SPI-4 Table A3 and test circuit Fig A1

- $0.9 * |V_n| - 23 \text{ mV} < |V_a| < 1.1 * |V_n| + 26 \text{ mV}$

@  $|V_a| = 370 \text{ mV}$ ,  $|V_n| < 436.7 \text{ mV}$   $\Rightarrow V_{os} = +/- 33.5 \text{ mV}$

@  $|V_a| = 500 \text{ mV}$ ,  $431 < |V_n| < 581 \text{ mV}$   $\Rightarrow V_{os} = +/- 40.5 \text{ mV}$

@  $|V_a| = 800 \text{ mV}$ ,  $|V_n| > 697 \text{ mV}$   $\Rightarrow V_{os} = +/- 51.5 \text{ mV}$

### 2) Terminator tolerance: ref SPI-4, Table 20

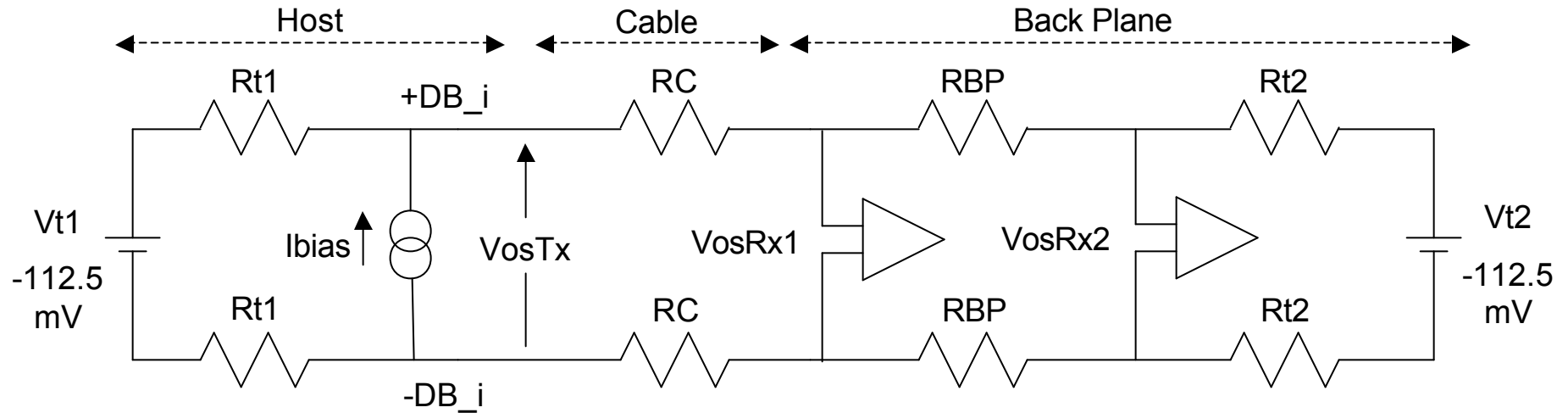
- negation bias  $100 - 125 \text{ mV}$   $\Rightarrow V_{os} = +/- 12.5 \text{ mV}$

### 3) Receiver offset budget: ref SPI-4, Table A3

- receiver offset  $\Rightarrow V_{os} = +/- 30 \text{ mV}$

## Major DC Offset Error Terms (continued)

### 4) Bias cancellation errors due to cable and back-plane resistance. Example:



- ⌘ Nominal terminators & driver:  $V_{t1} = V_{t2} = -112.5$  mV,  $R_{t1} = R_{t2} = 52.5$  ohms,  $I_{bias} = 2.108$  mA
- ⌘ R cable: 12m 32 AWG 50 deg C  $R_C = 8$  ohms
- ⌘ R back-plane at 1.5 ohms per slot x 10 slots:  $R_{BP} = 15$  ohms
- ⌘ Receiver offset  $V_{osRx2}$  due to IR drop adjacent to the back-plane terminator:  

$$V_{osRx2} = -112.5 + 2 * 2.108 * [R_{t1} \parallel (R_{t2} + R_C + R_{BP})] * R_{t2} / (R_{t2} + R_C + R_{BP}) = -21.7$$
 mV
- ⌘ Receiver offset  $V_{osRx1}$  due to IR drop adjacent to the back-plane connector:  

$$V_{osRx1} = -112.5 + 2 * 2.108 * [R_{t1} \parallel (R_{t2} + R_C + R_{BP})] * (R_{t2} + R_{BP}) / (R_{t2} + R_C + R_{BP}) = +4.2$$
 mV

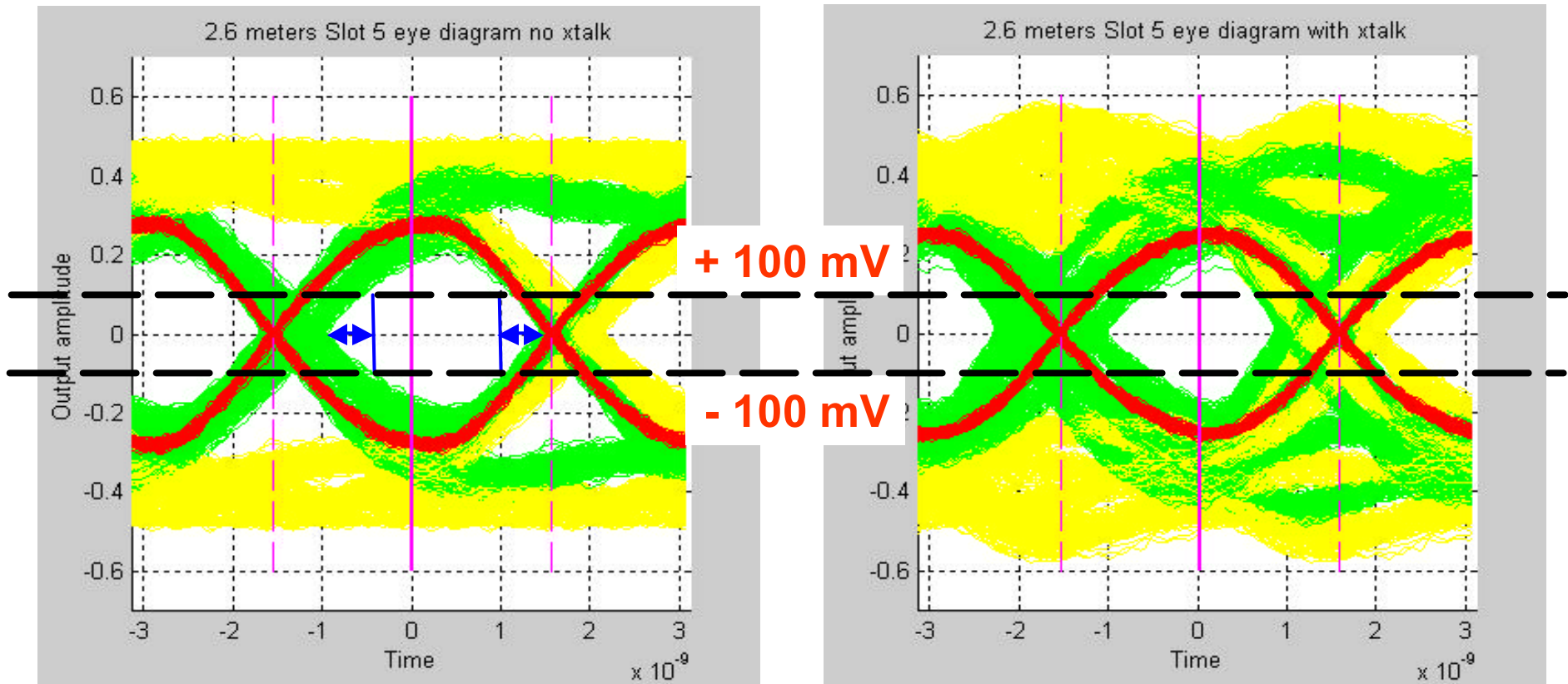
## Summary of Major DC Offset Errors:

Nominal Driver Amplitude	Driver offset	Terminator tolerance	Receiver Offset	Interconnect Resistance (this example)	Worst-case Total Offset Error	“RSS” Offset terms and ADD + IR
370 mV	+/- 33.5 mV	+/- 12.5 mV	+/- 30 mV	+ 4.2 / - 21.7 mV	+ 80.2 / - 97.7 mV	+ 51.2 / - 68.7 mV
500 mV	+/- 40.5 mV	+/- 12.5 mV	+/- 30 mV	+ 4.2 / - 21.7 mV	+ 87.2 / - 104.7 mV	+ 56.2 / - 73.7 mV
800 mV	+/- 51.5 mV	+/- 12.5 mV	+/- 30 mV	+ 4.2 / - 21.7 mV	+ 98.2 / - 115.7 mV	+ 65.2 / - 82.7 mV

### Notes:

- The IR offset term is derived for an 8 ohm cable and 15 ohm backplane. This may not be worst-case.
- The “RSS” column treats the driver, terminator and receiver offsets as random. This may be optimistic, depending on the actual distribution of these errors. Actual maximum offset values lie somewhere between the “Worst-case” and “RSS” values.

# Ultra640 Eye Diagrams .. from T10/01-224r0: 5-slot Backplane, 5 loads, 2.6 m Twisted-Flat Cable Eye Diagrams at Slot 5, without and with Crosstalk

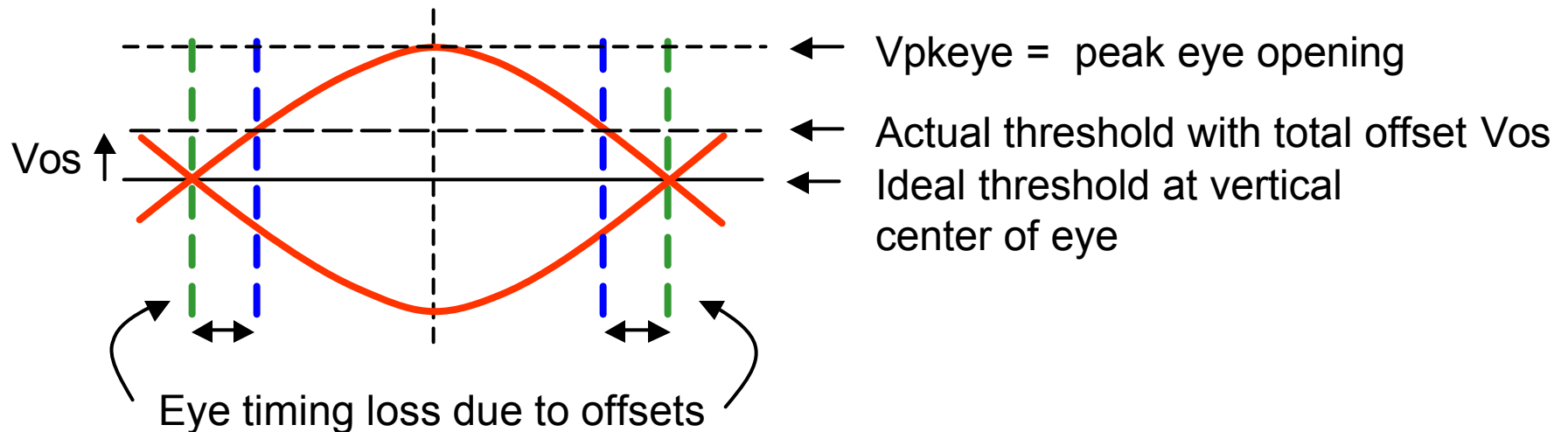


- Drive Signal: 500 mV peak differential on DB0
- Crosstalk: 0 mV

- Drive Signal: 500 mV peak differential on DB0
- Crosstalk: 500 mV peak 1010 on DB1 and DBP1

The blue arrows show that a +/- 100 mV total DC offset error gives a timing margin loss of approximately 500 ps at each end of the bit-cell

## Timing Loss due to DC Offset Errors



- With 500 mV peak drive, T10/01-224r0 shows a 200 mV peak approximately sinusoidal eye opening with a 2.6 m cable into a loaded backplane at the Ultra640 data rate. For this case:
  - A 100 mV offset error wastes 50% of the available 200 mV peak vertical eye opening
  - Eye timing loss due to offset per half-bit cell =  $0.5 * T * [\sin^{-1}(V_{os} / V_{pkeye})] / 90$
  - Timing loss due to 100 mV offset in a 200 mV eye = **520 ps at each end of the bit cell** or **33%** of the total 3.125 ns Ultra640 bit cell
  - Offset corrected to < 10 mV reduces timing loss to **< 50 ps at each end of the bit cell** or **< 3.2%** of the total 3.125 ns Ultra640 bit cell



## DC Offset Error Correction in LVD SCSI

- Total SCSI Bus DC Offset errors can be detected at the receiver using the existing SPI-4 training pattern structure.
  - The training pattern as defined in SPI-4 begins with a low-frequency asserted-negated reference pattern for AAF adaption. This pattern is also suitable for detection of total DC offset.
  - The 200 ns durations of VA and VN in this pattern allow reflections, crosstalk and ISI to settle so that the actual DC error can be detected.
  - The DC asserted VA and negated VN receive levels can be captured during this low frequency portion of the training pattern.
  - The offset component of the input signal is then  $( |VA| - |VN| ) / 2$ .
- Standard circuit techniques can be used to correct total bus offset plus internal receiver offset.
  - Offset correction can be done during the existing training interval, e.g., after AAF adaption and before de-skew.
  - Correction to a residual error of less than 20 mV is reasonable.

## DC Offset Errors in LVD SCSI: Conclusions

- Eye opening loss due to DC Offset errors for Ultra640 SCSI is significant, and comparable to losses due to ISI, reflections and cross-talk.
- DC Offset correction can be readily implemented within the existing training pattern structure.
- DC Offset correction allows improved timing margin and / or operation at lower transmitted signal amplitudes.
- Correction of DC offset errors will also reduce receiver time asymmetry errors.
- Suggested Receiver DC Offset correction specifications for Ultra640 SCSI:
  - Range of external offset correction: +/- 75 mV minimum  
(excludes the 30 mV internal offset budget)
  - Residual offset error after training +/- 20 mV maximum  
(reduces the 1 ns error on slide 8 to 200 ps max)