Isochronous & SBP3

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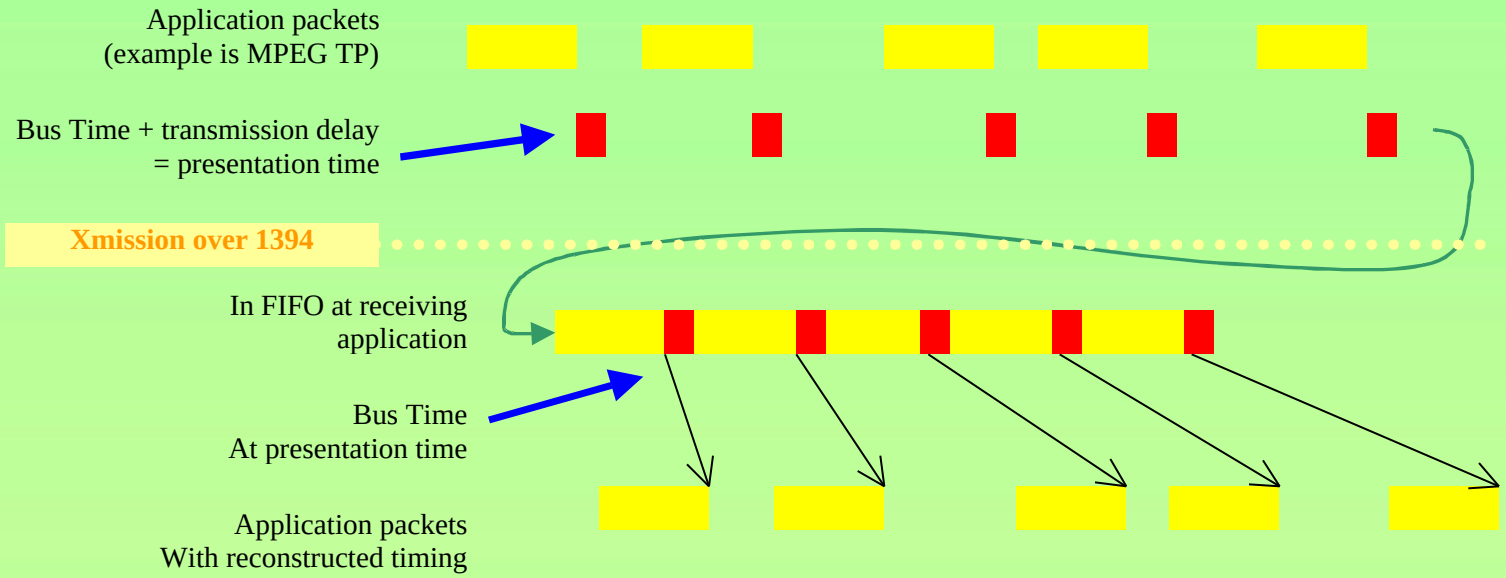
Topics

- Streaming Applications, 61883 and 1394
- Clock Distribution on 1394
- Why it works anyway
- The effect of non-format cognizant storage
- Isochronous recording format overview
- Demonstration

Timing & Re-timing Application Packets

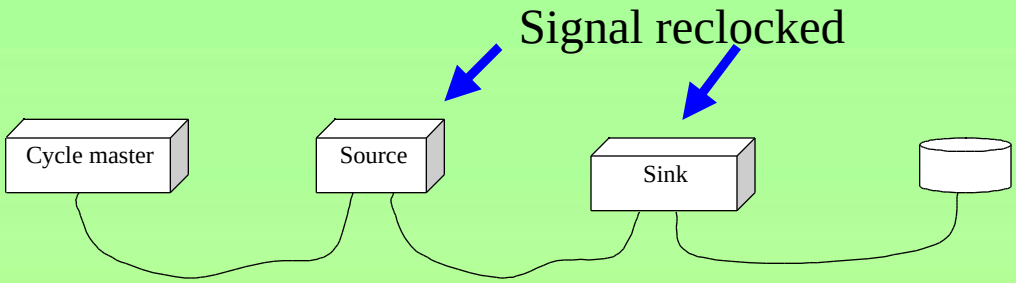


- At transmitter: Capture bus time of “interesting events” and add transmission delay
  - Interesting events - MPEG2 TP, DV video synch or audio synch
  - create embedded timestamp (SPH - MPEG2 TP or SYT in FDF of CIP for video or audio synch)
- At receiver: Wait for bus time contained in time stamp, then regenerate the “interesting event”
  - In example, announce the delivery of an MPEG2 TP

Problems (the easy part)

- All nodes have a common concept of time for creating and consuming time stamps
  - OK because all nodes have the cycle time register which is updated 8000 times per second by cycle start packet
    - Therefore, SPH and SYT time stamps are all in terms of absolute bus time at time of transmission
  - Not OK for intermediate storage devices because bus time of recording will almost always be different from bus time at playback
    - Intermediate, non-format cognizant devices will need to either:
      - Remember bus time at recording time and translate embedded time stamps upon playback by calculating record/playback delta time
      - Convert time stamps at recording to a time relative to bus time at time of transmission, then convert back to absolute time when playing back
    - Both of these are real time calculations done on the fly by recording device

Problems (the hard part): Distributing time on 1394



- Bus time is defined as counts of a 24.576MHz PHY clock (~40ns per cycle)
- Every 1394 node has a PHY clock, and virtually all existing 1394 nodes implement a PHY clock that is free running relative to the PHY clocks of all other nodes on the bus
- In the process of repeating packets, at each hop the packet bits are received, then reclocked using the local PHY clock
  - According to 1394 standard: PHY delay is <= 3.5 PHY clocks, exactly (<= ~144ns)
  - The repeat delay of each cycle start packet through each node can vary by +/- 0.5 counts of the PHY clock
  - When it arrives at a node, the cycle start packet may be up to 1 PHY clock out of phase with local bus time
- Therefore, in normal operation:
  - The bus time register of a non-cycle master node may experience a count discontinuity on a given isochronous cycle of up to plus or minus int((1 + <number of hops to root>)/2) counts in the cycle offset field (= ~326ns for 16 hops)
  - This is the worst case discontinuity; actuality is random discontinuities that are non-cumulative and that center on the PHY clock of the cycle master

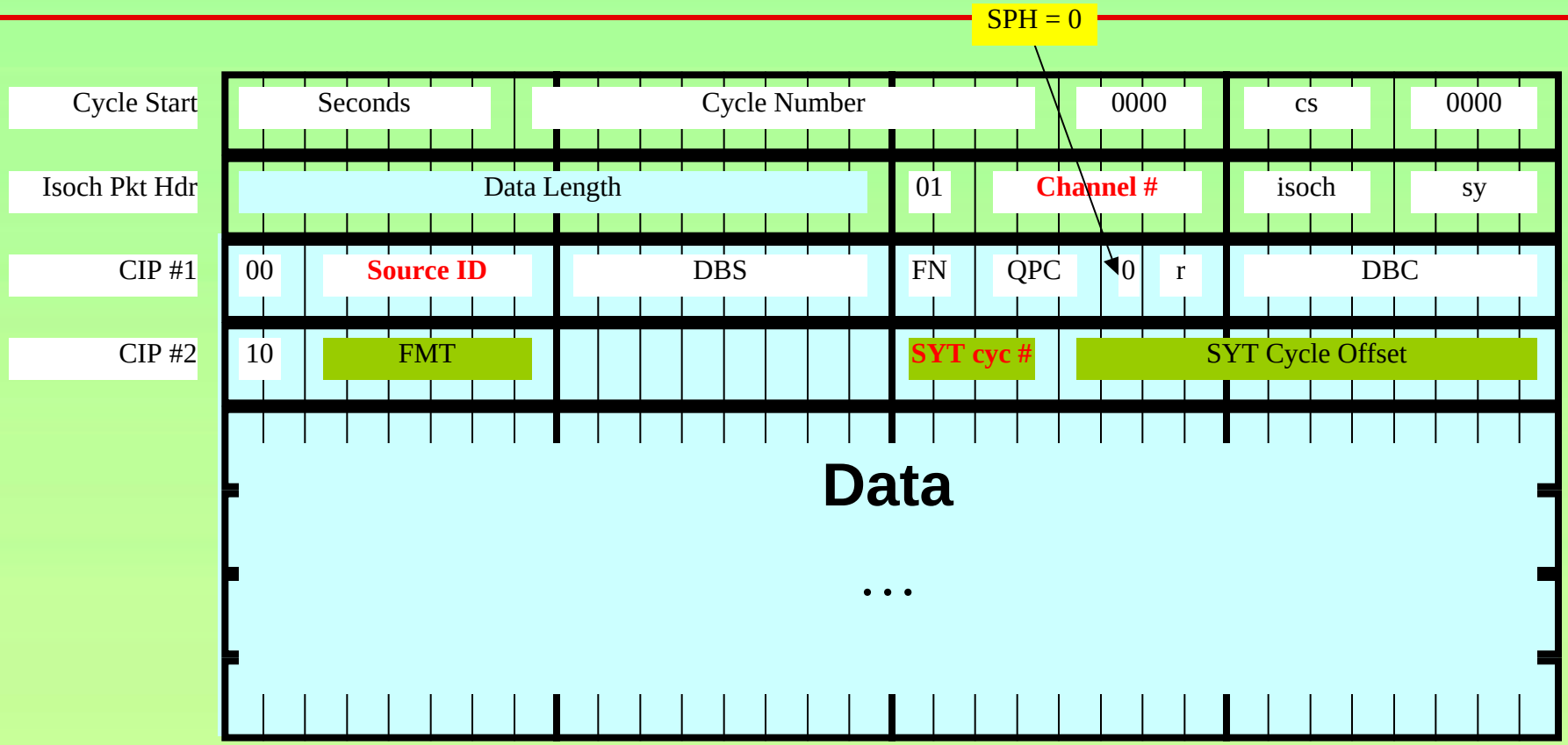
Why it Works Anyway

- All 1394 nodes share a common clock reference
  - Yes, due to reclocking at each node, and the fact that most 1394 implementations do not phase lock their PHY clocks to the cycle master, there can be bus time count discontinuities as discussed
  - But through the transmission scintillation, there is a 100ppm clock coming through
- MPEG2 TPs are stamped at the transmitter and consumed at the receiver based on this scintillating clock
- Empirically, satellite uplink/downlink has larger scintillation due to atmospheric conditions, especially due to inconstant ionosphere reflections and scattering
- In the lab, CE companies have experimented with MPEG2 TP jitter up to 4 milliseconds and have found no problem
  - This is a technical measurement of decoder performance and video clock extraction, and the results show no degradation in either
- The commodity MPEG2 decoders can handle MPEG2 transport streams delivered by satellite
  - Therefore: commodity MPEG2 decoders in real world installations have no problem with 1394 with 61883-4 or 61883-7 as a transport layer

The Effect of Bit Recorders

- Bit recorders capture the exact sequence of packets and recreate them later
- Time stamp transformation is in terms of cycle number (125us)
  - Cycle offset field is not altered
  - Time stamp irregularities due to cycle time scintillation are not affected by adjustments to the cycle number value
- Therefore: Recording the exact packets, then playing them back at a later time (with embedded time stamps properly adjusted) has no adverse effect on the integrity of the stream

Isochronous Recording Format SYT time stamp (Parts 2,3,5&6)



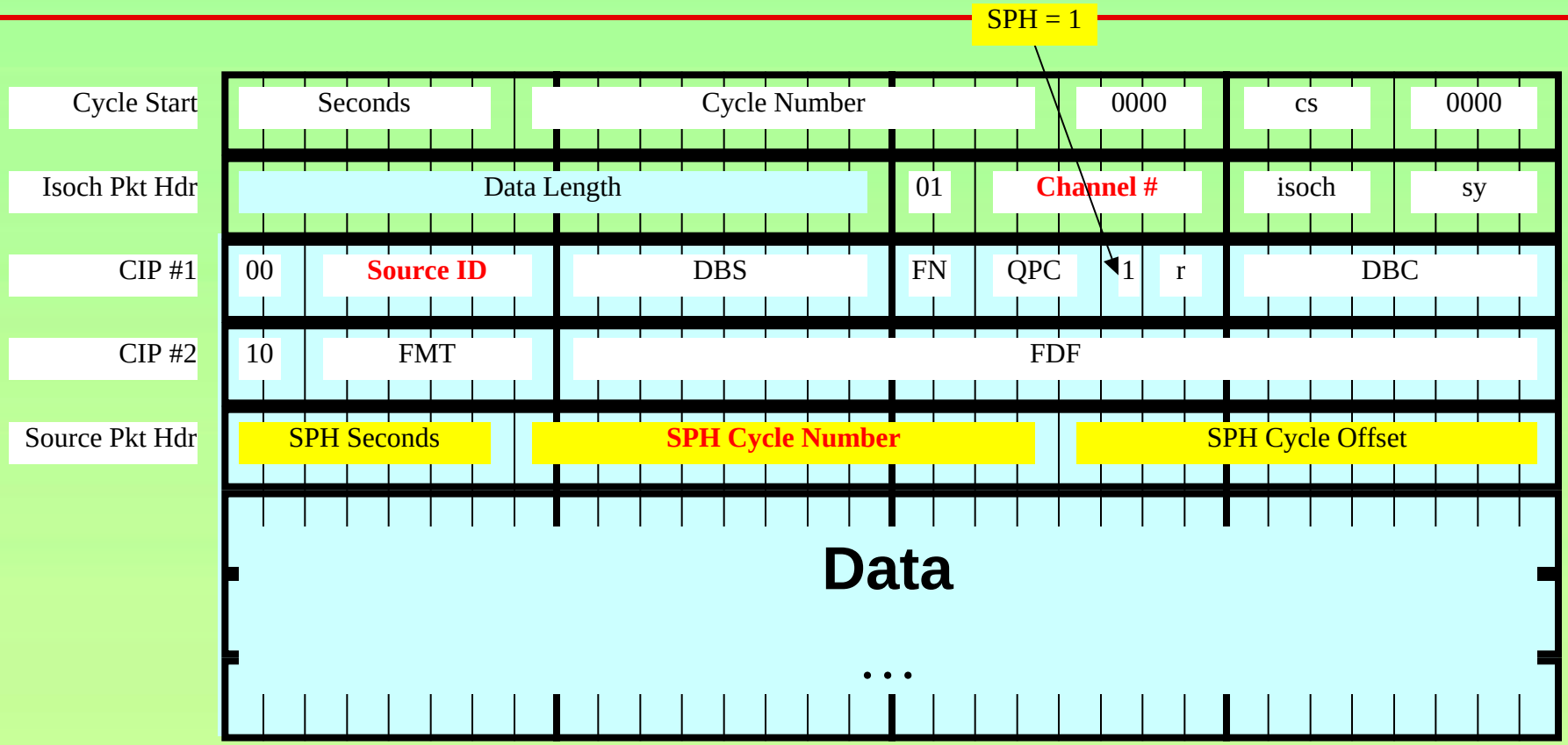
Cycle Start is recorded, but stripped on playback

Not mandatory, but useful for synch/resynch and stream navigation

CIP header <u>always</u> occupies first 2 quadlets of isoch packet

Fields in red must be modified by bit stream recorder

Isochronous Recording Format SPH time stamp (Parts 4&7)



CIP header <u>always</u> occupies first 2 quadlets of isoch packet

SPH does <u>not</u> always immediately follow CIP header

- **SPH only present in stream when SPH field =1 (in this case, SPH=1 for <u>all</u> packets in stream)**
- **If present, must examine DBS, DBC & FN fields to locate SPH**
- **If present (SPH=1), there may be zero, one or more than one SPH in an isoch packet**

Fields in red must be modified by bit stream recorder

Demonstration

- Previous demonstrations of this Technology
  - Quantum
    - Comdex 11/98, Las Vegas
    - Western Cable Show 11/98, LA
    - Winter CES 1/99, Las Vegas
  - Western Digital
    - Comdex 11/99, Las Vegas
    - Winter CES 1/00, Las Vegas
    - Winter CES 1/01, Las Vegas