SCSI signal modeling study group (SSM) 01-310r0
October 24-25, 2001
Colorado Springs, CO

Subject: Draft minutes for the SSM working group on October 24-25, 2001 in Colorado Springs, CO

This was the next meeting to address the general subject of modeling for parallel SCSI. Paul Aloisi of TI led the meeting. Bill Ham of Compaq took these minutes. Larry Barnes of LSI Logic hosted the meeting.

Last approved minutes: 01-261r1.

1. AGENDA SSM MEETING

2. Introductions

Paul Aloisi opened the meeting and conducted the introductions and reviewed the meeting purpose. He thanked Larry Barnes of LSI Logic for arranging the details for hosting the meeting.

Paul noted that this meeting will be focused on SSM letter ballot comments resolution -2 in this meeting.

3. Attendance

Attendance at working group meetings does not count toward attendance requirements for T10 plenaries.

The people in the following list attendee this meeting:

Name	Organization	e-mail	Phone
Lee Hearn	Adaptec	Lee_hearn@adaptec.com	408-957-6853
Greg Vaupotic	Amphenol Spectra-Strip	gvaupotic@spectra-strip.com	203-287-7425
Bill Ham	Compaq	Bill_ham@ix.netcom.com	978-828-9102
Zane Daggett	Hitachi Cable	zdaggett@hcm.hitachi.com	603-669-4347 x.236
Larry Barnes	LSI Logic	Larry.barnes@lsil.com	719-533-7432
John Lohmeyer	LSI Logic	John.Lohmeyer@lsil.com	719-533-7560
Martin Ogbuokiri	Molex	mogbuokiri@molex.com	630-527-4370
Bruce Manildi	Seagate	Bruce_manildi@notes.seagate.com	831-439-7729
Paul Aloisi	Texas Instruments	paul_aloisi@ti.com	603-222-8687

4. Agenda development

The agenda shown was that used.

5. Approval of previous minutes

The minutes of the last meeting were reviewed and minor changes were made. Motion Ham / Aloisi that the draft minutes be approved as modified. Motion passed unanimously.

6. Action item review

Review of action items was postponed to the next meeting.

7. Administrative structure

The present administrative structure for SSM / SSM-2 is:

Paul Aloisi, TI, chair SSM / SSM-2
Larry Barnes, LSI Logic, Vice chair and SSM / SSM-2 technical editor
Bill Ham, Compaq, Secy

8. Presentation Policy

This item is included for easy reference and will be retained in future minutes.

It is the policy of the SSM working group that all material presented at the SSM working group shall be made available electronically and posted on the T10 web site.

Material presented at the meeting should be uploaded to the T10 web site two weeks prior to the meeting. Alternatively the material may be electronically supplied to the chair or secretary at the meeting where the material is presented at the discretion of the chair.

Material should be free from any statement of confidentiality or restriction of use and should not contain any pricing or product scheduling information.

9. Presentations

9.1 Carry over presentations

9.1.1 Cable extraction data, Jie Fan, Umesh, Madison/Seagate

[Update on Gigatest in August]

2D extraction models from cable design information for round cable were determined to be not practical due in part to the intrinsically 3D nature of the problem. Gigatest labs is going to provide S-parameter measurements and RLGC models using a multiline approach on several constructions and Madison is attempting a single line matrix extraction approach on round cables.

When this effort is complete the intent is to use these RLGC models as part of the system simulation modeling effort (led by Bill Troop).

9.1.1.1 Single pair data extraction from electrical measurements on round shielded cable, Jie Fan

Jie has collected several round shielded bulk cable samples and done experimental work to calculate a set of RLGC parameters. An iterative optimal curve fitting approach is used here. This method is described in SSM (sort of). [Source figures describing the method need to be supplied to Larry.]

Jie will present the RLGC data resulting from the curve fitting at the next meeting.

9.1.1.2 Multiline data extraction from electrical measurements, Umesh

This effort is being focused through Gigatest labs.

An agreement with Gigatest labs has been concluded by a subset of participants of the SSM group for the purpose of doing some extractions from sample cables. This agreement is separate from any SSM work and this information is included in the minutes at the request of Bob Gannon, JPM, who is one member of this subset.

Several different constructions are being used: round, twist and flat, cable assembly

It is the present intent of this subgroup to present the results at the December 2001 meeting.

9.1.1.3 Parameter extraction for transition region models, Bob Gannon

The following is included in the Gigatest work:

An RLGC model of the types of transition region type identified below:

- 30 AWG solid shielded round to VHDCI

These models will be delivered to Bill Troop for integration with the system simulation effort.

[The following material has been mostly been moved into the document - material will be left in the minutes until after the letter ballot closes.]

In satisfaction of an action item the following matrix of transition regions and issues with each is defined:

Flat to connector- Boundary is the face of the IDC contact that touches the copper conductor.

Issues- Geometry of deformed insulation is difficult to measure and represent via CAD to capture impedance discontinuity. 3D CAD transformation needed to represent length of discontinuity is difficult to draw. Ansoft 3D package produces R,L, and C values, but no G.

Twist and Flat to connector- Boundary is the face of the IDC contact that touches the copper conductor.

Issues- Same as above with the additional concern of how to concatenate the twist and flat regions via SPICELink. There is no actual shield for physical ground reference. One needs to model +/- 1 signal sources, but the actual ground is virtual.

Round shielded to connector- Boundary is the beginning of the fan out required for attachment to connector at the point of crimp, solder or weld.

Issues- Accurate CAD representation of the fan out to contact to connector is very difficult to produce. Currently parameter extraction is under investigation with Gigatest Labs.

Round shielded (may be shielded and folded multi-twinax) to pcb- Boundary is the beginning of the fan out required for attachment to connector and the point of attachment of the wires to the pcb solder pads.

Issues- See above. The pcb solder to wire region is an additional CAD nightmare.

9.1.1.4 Parameter extraction from physical description of twist and flat constructions, Greg Vaupotic, Amphenol Spectra Strip

[This item appears to be complete - will remove from minutes if group agrees in October]

Using an electromagnetic simulator and a physical description Greg is deriving RLGC matrices using a 2D solver approach. Some of the results are in SSM (-1). Further work is not contemplated at the moment.

9.1.2 Periodic Structures in transmission lines, Larry Barnes, LSI Logic

Larry presented the results of a preliminary analysis that represents the effects of lumped capacitance loads added at periodic distances along an ideal infinitely long lossless transmission line. The purpose of this work is to provide a foundation for determining the likely spacings and frequencies where significant suckouts and other resonances may be expected. This is mainly useful for modeling of backplanes and twist and flat constructions.

Some basic equations and solutions have been formulated and the complex structure of the solutions indicates that more work is needed to refine the model. Definite suckout peak positions were noted whose intensity increases dramatically with increasing frequency. Due to the lack of detailed written explanations of the model Larry suggested that the details not be posted until the additional work and explanations are available.

The formal name for this kind of analysis is “Brillouin diagram for generic periodic loaded transmission line”.

Four orthogonal variables need to be related: spacing; periodic discontinuity e.g.capacitance, inductance; frequency; and resulting insertion loss. How to display this is left to the student at the moment.

9.1.3 IBIS presentations, Larry Barnes, LSILogic

Larry reviewed the present status with IBIS - no change from last meeting.

9.1.4 Models for instrumentation interfaces status, Jason Chou

[Jason intends to pursue the letter ballot comment process to include additional information into SSM concerning instrumentation interfaces.]

[No new technical input at this meeting]

[the following historical material is retained until after the SSM letter ballot]

The following url provides some information on information interfaces: www.agilent.com/find/randd. Some of this information may be placed in the SSM document.

Jason has been working on the models to be used for instrumentation interfaces (such as oscilloscope probes). His investigation showed that modeling is not in the mindset of the common instrumentation suppliers. Tektronix agreed to try to develop a model for the active differential probe. It was noted that the single ended probe may be more important because the differential probe gives no information about the common mode content of the signals and two single ended probes gives both the differential and the common mode.

Jason also explored the information available from basic circuit description of the probes. It was quickly determined that only active probes should be considered for SSM uses.

The capacitance levels reported by Jason appeared significantly higher than is available on state of the art probes.

Jason is actioned to provide a draft for the instrumentation interface section of the document.

9.2 New presentations

9.2.1 Gigatest status, Bruce Manildi, Seagate

Bruce presented a document that will be uploaded to the T10 web site that describes that present status of the work being done by Gigatest relating to SCSI interconnect modeling and verification. This work is sponsored by a subset of the companies but has no official link to the SSM working group. See this document for details.

10. SSM

SSM has completed the is out for Letter ballot - closed for this meeting until letter ballot comments at the next meeting in October. Ballot closes August 24, 2001.

11. SSM-2 Standard 1514-D

[no new input in October]

11.1 Ground work for the SSM-2 standard

Paul led the discussion for determining the content and organization of SSM-2. See item 17 below for the present thinking.

The framework for the SSM-2 document was reviewed and extensive modifications were made by the section editors.

The basic features to be standardized were discussed with the following results:

- method of validation for models for components
- method of validation for system models
- basic requirements on the format for the model description for specific component types
- methods for creating elemental component models (details of this topic are not yet agreed)
- system simulation methodologies
- information interchange specification across component boundaries
- information interchange specification into simulation tools

11.2 Matrix development for SSM-2

The following summarizes the present position for the SSM-2 matrix. This matrix is a concise description of the methodology to be used for the respective areas of the point to point SCSI bus segment. Several of the areas were significantly modified at this meeting. Note that the multidrop areas have not yet been identified.

11.2.1 Overview section: owner, Bill Ham

The basic content was discussed. SSM (-1) will be the basic material with a few additions.

11.2.2 Transceiver chips: owner, Larry Barnes

Interface is at packaging pins
Model types: Behavioral only (because it is the only transportable type)
Data patterns: TBD
ISI compensation: required but not presently believed compatible with IBIS capability – this means that IBIS will have to be enhanced.
Single line required - cross talk from non SCSI sources not considered in the model, SCSI line cross talk is not significant within the transceiver. Therefore multiline models are not required for transceivers. (Possible risk with some package types.)

11.2.3 Bus segment termination: owner, Paul Aloisi / Don Getty

No new content information.

Interface is at package pins
Model types: Either circuit or behavioral
Terminator type: multimode
Single line only

11.2.4 Host bus adapter (transceiver board): owners, (Need new owner)

Interface is at transceiver board connectors used for the SCSI link (at the board side of the connector - not including the connector), transceiver chip pins, terminator chip pins, unused connectors are part of the board
Model types: Circuit
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

11.2.5 Mated connectors: owner, Martin Ogbuokiri, Steve Wong

No new content information.

Interface is at transceiver board and the beginning of the cable assembly transition region
Model types: Circuit
Connector types: VHDCI, SCA-2, HD68
Mounting style: thru hole, SMT,

single line, multiline

Connector models are in place at the Molex web site and pointers are now in place on the T10 site.

11.2.6 Transition regions: owners, Bob Gannon, Jason Chou

Interfaces are at the connector termination and the uniform bulk cable
Model types: circuit
Construction types: twisted flat, round fanout, laminated round, IDC flat?
Single line multi-line

A start was made in this area – see Bob Gannon presentation above.

11.2.7 Bulk cable: owner, Jie Fan, Zane Daggett, Greg Vaupotic

Interfaces are at the beginning of the cable assembly transition region on either end.
Model types: RLGC
Cable types: flat, round shielded, round unshielded twisted flat?
Single line, multiline

11.2.8 Backplane: owner, Larry Barnes, Bruce Manildi

Interfaces: connectors mounted on the backplane, directly mounted components, (this subject is still not settled)
Model types: circuit
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

Issue: how to handle the unmated connectors on the backplane. Two sub issues: (1)lack of existence of unmated connector models and (2) convergence of the simulation with dangling open circuits. The latter can be handled by adding a high value resistance to the open circuit to “fool” the simulator.

11.2.9 Cable assemblies, owner Jason Chou (Lead), Bob Gannon, Steve Wong backups

Interfaces: connectors
Model types: circuit (possible combination of circuit and behavioral)
Constructions: point to point, multidrop

11.3 How to develop IBIS model section , Barnes

Not discussed at this meeting.

11.4 Simulation integration strategy

Determine the goal of the simulation (examples: validate the basic behavior of a new component in a system, troubleshooting guidance, qualification of the signal integrity in a specific configuration, characterization of the expected EMI performance)

Determine the specific characteristics that are sought (example: ??)

Define the topology

Define the collection of components

Obtain the models for all the components

…………subject discussion truncated – will continue next meeting.

11.5 System configurations - Topology, Bruce Manildi

[not discussed at this meeting]
[Need pictures for below]

The following is a starting list of system configurations that need different considerations from a modeling perspective. Note that a device may be a SCSI expander.

1. Basic structure shown in the trial simulation work (single initiator/cable/single target on backplane)

2. Basic structure shown in the trial simulation work (single initiator/cable/multiple targets on backplane)

3. Expander isolated backplane with multiple targets on backplane

4. Multi-drop flat cable connected to a single HBA board (terminator on cable on one end and on the HBA on the other end). All connectors have devices attached.

5. Multi-drop flat cable connected to a single HBA board (terminator on cable on one end and on the HBA on the other end). Only the far end connector has a device attached - all other connectors have no devices attached - requires an unmated half-connector model.

6. Single target in an enclosure with a cable connection on the enclosure bulkhead to a round cable to an HBA in a different enclosure

11.6 Data patterns, Bill Ham, Bruce Manildi

Not discussed at this meeting. The main issue appears to be the ability of specific simulation packages to handle logical data pattern specifications.

11.7 Data rate - group - Ultra640 & Ultra1280 additions

This item is left on the agenda due to lack of formal action on the topic. There is nothing special about the data rate that has been identified to date.

11.8 Tools:

Not discussed at this meeting. [Secy note, do we need to continue this item on the agenda?]

12. New business

12.1 Comment resolution for SSM, Barnes

The T10 letter ballot against revision 04a of SSM has completed. All the comments were addressed and resolutions proposed. The proposed resolutions are contained in 01-303r0.

Motion Barnes / Ham that the SSM working group recommend that resolutions contained in 01-303r0 be accepted by the T10 plenary in satisfaction of the T10 letter ballot against SSM rev 04a.

Motion passed unanimously

13. Status of models supplied to the T10 web site

The following table will substitute for the information in the minutes relating to the status of the models being made available to the T10 web site.

Model	Company	T10 web content	Future intentions	Issues
VHDCI	Molex	available		
HD68	Molex	available		
SCA-2	Molex	available		
VHDCI	Tyco/AMP	no	has not supported SSM	
HD68	Tyco/AMP	no	has not supported SSM	
SCA-2	Tyco/AMP	no	has not supported SSM	
VHDCI	ERNI	no	has not supported SSM	

HD68	ERNI	no	has not supported SSM	
SCA-2	ERNI	no	has not supported SSM	
VHDCI	FCI	no	has not supported SSM	
HD68	FCI	no	has not supported SSM	
SCA-2	FCI	no	has not supported SSM	
Transceivers	LSI logic	available for Ultra160 and Ultra2	Ultra320 to be supplied when chip ships publicly	
Transceivers	Seagate	not yet	to supply soon	
Transceivers	Adaptec	no	has declared non-support for their models	
Transceivers	Maxtor	not committed	not clear	
Transceivers	Fujitsu	not committed	not clear	
Terminators	TI	available		
Terminators	Dallas	no	has not supported SSM	
Transition region	JPM	not yet	will supply in August	
Backplanes	Compaq	not committed		
Backplanes	SCSI Harbor	no	not available	data base no longer exists
Backplanes	IBM	not committed		
Backplanes	HP	no	has not supported SSM	
Backplanes	Eurologic	no	has not supported SSM	
backplanes	nStor	no	has not supported SSM	
backplanes	Sun	no	has not supported SSM	
Backplanes	LSI Logic	not committed	not clear	
Backplanes	American Megatrends	no	has not supported	

			SSM	
HBA boards	Adaptec	no	has declared non-support for their models	
HBA boards	LSI Logic	not committed	not clear	
HBA boards	Q Logic	no	has not supported SSM	
HBA boards	Tekram	no	has not supported SSM	
HBA boards	Atto	no	has not supported SSM	
Target boards	Seagate	not committed	not clear	
Target boards	Maxtor	not committed	not clear	
Target boards	Fujitsu	no	has not supported SSM	
Target boards	IBM	no	has not supported SSM	
Target boards	Quantum	no	has not supported SSM	
bulk cable point to point	Madison	not yet	committed for near future	
Shielded cable assys	Amphenol	no	has not supported SSM recently	
Unshielded cable assys	Amphenol	no	has not supported SSM recently	
Shielded cable assys	JPM	not yet	probably committed for later	
Unshielded cable assys	JPM	not yet	probably committed for later	
Bulk cable point to point	C&M	not yet	not committed	
Bulk cable multidrop	C&M	not yet	not committed	
Shielded cable assys	C&M	not yet	not committed	
Multidrop cable assys	C&M	not yet	not committed	
Bulk cable multidrop	Amphenol Spectra-Strip	2D, not yet	committed for near future	3D TBD
bulk cable	Hitachi	not yet	committed	

point to point			for near future	
bulk cable multidrop	Hitachi	not yet	possible for later	
bulk cable multidrop	Temp-flex	not committed	not clear	

14. Next meetings

Approved schedule:

December 12-13, 2001 1:30PM to 6 PM 12/12; 9AM to 6PM 12/13 Guadalajara, MX (JPM)

Requested schedule:

Feb 19-20, 2002 (Tues/Wed) 9AM to 5 PM both days, 2/19 editing, 2/20 SSM working group, Santa Cruz, CA (Seagate)

April 03, 2001 (Wed) 9AM to 5PM, New Hampshire, (Hitachi)

15. Action Items:

15.1 Action items from previous meetings

Status as of this meeting is shown.

Bruce Manildi to provide access information for the Seagate transceiver models to the T10 web site.
Status: Seagate now has IBIS models (no precomp) available. Encrypted HSPICE models are also currently available from Seagate (NDA required). Information still needs to be loaded to the T10 web site. Umesh is the contact - nearly done.

Jie Fan, Madison Cable to provide access info for a point to point bulk cable model to the T10 web site.
Status: model is done, verified and are available internally in circuit form - still needs info supplied to T10 web site - needs web link from internal IT folks - carried over with progress - Paul A to write a brief note to Chuck Grant explaining the need to break thru Madison’s internal roadblocks.

Zane Daggett, Hitachi, to provide bulk cable models to the SSM web site (per last meeting minutes).
Status: expect posting before next meeting (round 30 AWG solid will go up first followed by flat TPO) - carried over with progress

Paul A to send emails to all folks with open action items on Tuesday of each week (until the action item is completed).
Status: ongoing

Larry Barnes to take the material in the SPI-3 and SPI-4 document relating to the signal budget and figure out how to incorporate into the SSM document
Status: carried over to SSM-2

Larry Barnes to send aperiodic emails to all folks with open document issues (until the issue is closed).
Status: done

Section editors to provide material to Larry for the next revision of the document.
Status: done except for Martin O, Bob Gannon, and Jason Chou – document will not be held up waiting for there inputs - overcome by events due to schedule of SSM letter ballot

Jason is actioned to provide a draft for the instrumentation interface section of the document.
Status: overcome by events due to schedule of SSM letter ballot

Ham to contact JL to determine position on providing pointers to extracted models not from suppliers.
Status: carried over

Paul Aloisi to make sure that there is a speaker phone connection available for the August meeting.
Status: done

Larry Barnes will set up a final editing meeting about the last week of June to complete the document before the July T10 meeting.
Status: done

15.2 New action items from present meeting

Greg Vaupotic to supply model for 30 AWG solid, TPE dielectric, twist and flat. Models for the flat region and for the twist region from 2D simulations, multiple frequencies to be supplied separately. Complete model for flat + twist needs to be constructed by the user from RLGC matrices.
Status: new

Jie to supply source figures describing the curve fitting extraction method to Larry.
Status: new

Jie to present the RLGC data resulting from the curve fitting at the October meeting.
Status: new

16. Adjourn

The meeting adjourned at 4:30 PM

17. Present view of the structure of SSM-2 (informative)

Document structure & work for SCSI Signal Modeling 2 - T10-1514-D
1 Scope   (Larry 1-4)

2 References
2.1 Overview (Change clause title to Normative Reference)
2.2 Approved references
2.3 References under development (Add SPI-5).(SPI-6?)
2.4 Other references – Publications (Changed)

3 Resources   – (move swap with 4 for the correct structure)
3.1 Tools
3.1.1 Simulation tools
3.1.2 Extraction tools
3.1.3 Model creation tools
3.1.4 Integrated simulation tools

4 Definitions, acronyms, symbols, abbreviations, keywords, and conventions
4.1 Definitions
4.2 Acronyms
4.3 Symbols and abbreviations
4.4 Keywords
4.5 Conventions

5 General
5.1 Overview ....(Bill)
5.2 Signal modeling purposes
5.2.1 Overview
5.2.2 Physical components and signals
5.2.2.1 Relationship between physical and modeling terminology
5.2.2.2 Elemental components
5.2.2.3 Composite components
5.2.2.4 Systems
5.2.2.5 Signals and measurement points
5.2.2.6 Run length dependent driver signals
5.2.2.7 Interactions between signals on different signal lines
5.2.3 Viewpoints
5.3 Application to measurement
5.4 Practical considerations for creating models
5.5 Relationship between components of the modeling environment
5.6 Relationship between signal specifications in standards and modeling
5.7 Accuracy and model validation considerations ...(new 5.7 Features that will be standardized)

6 Methodologies .....(Larry)
6.1 Overview
6.2 Behavioral
6.2.1 IBIS 3.2
6.2.1.1 Overview
6.2.1.2 IBIS model creation
6.2.1.3 Pre-modeling activities
6.2.1.3.1 IBIS version
6.2.1.3.2 Specific device
6.2.1.3.3 Corner limits
6.2.1.3.4 SSO effects
6.2.1.3.5 Schematics
6.2.1.3.6 Clamp diode and pullup references

6.2.1.3.7 Packaging information
6.2.1.3.8 Signal selection
6.2.1.3.9 Die capacitance
6.2.1.3.10 Vinl and Vinh parameters
6.2.1.3.11 Tco measurement conditions
6.2.1.3.12 Buffer grouping
6.2.1.4 Data extraction
6.2.1.4.1 s2ibis extraction
6.2.1.4.2 Direct simulation extraction
6.2.1.4.2.1 Extracting I/V data
6.2.1.4.2.2 Hi-Z buffers
6.2.1.4.2.3 Output only buffer
6.2.1.4.2.4 Open drain buffers
6.2.1.4.2.5 Input buffers
6.2.1.4.2.6 Sweep ranges
6.2.1.4.2.7 Pullup and power clamp sweeps relative to Vdd
6.2.1.4.2.8 Diode models
6.2.1.4.2.9 Extracting the Ramp Rate or V/s Waveform Data
6.2.1.4.2.10 Extracting Data for the [Ramp] Keyword
6.2.1.4.2.11 Extracting Data for the Rising and Falling Waveform Keywords
6.2.1.4.2.12 Minimum Time Step
6.2.1.4.2.13 Fallback drivers
6.2.1.5 Creating the IBIS file
6.2.1.5.1 Overview
6.2.1.5.2 Header Information
6.2.1.5.3 Component and pin information
6.2.1.5.4 Model description
6.2.1.5.4.1 [Model] keyword parameters
6.2.1.5.4.2 [Temperature Range] and [Voltage Range] keywords
6.2.1.5.4.3 I/V data section
6.2.1.5.4.4 [Pulldown] keyword
6.2.1.5.4.5 [GND Clamp] keyword
6.2.1.5.4.6 [Pullup] keyword
6.2.1.5.4.7 [POWER Clamp] keyword
6.2.1.5.4.8 Clamp keyword extrapolation caveats
6.2.1.5.4.9 [Ramp] keyword and waveform tables
6.2.1.5.4.10 [Driver Schedule] keyword
6.2.1.5.5 External Package Models
6.2.1.5.6 IBIS file conformance
6.2.1.6 IBIS model validation
6.2.1.7 IBIS model verification
6.2.1.8 Acceptance criteria
6.2.2 IBIS-X
6.2.3 Maxwell matrices (help from Cable and connector companies)
6.2.3.1 Overview
6.2.3.2 Emperical extraction (Jie)
6.2.4 Theoretical extraction (Greg)
6.2.5 Interpreting Maxwell matrices (Greg reading Ansoft matrix)
6.3 Circuit models

7 Elemental Component Models
7.1 Overview
7.2 General requirements
7.2.1 Applicability
7.2.2 Documentation
7.2.3 Model Name
7.2.4 Model class
7.2.5 Model boundary

7.2.6 Model limitations or dependencies
7.2.7 Model creation methodology
7.2.7.1 Model creation stimuli
7.2.7.2 Amplitude and timing
7.2.7.3 Frequency range
7.2.7.4 Rise time
7.2.8 Model validation
7.2.8.1 Accuracy requirements
7.2.8.2 Model validation stimuli
7.2.8.3 Amplitude and timing
7.2.8.4 Frequency range
7.2.8.5 Rise time
7.2.9 Model support contact information
7.2.10 License agreement
7.3 Interconnect component models
7.3.1 Overview
7.3.2 Bulk Cables (Greg)
7.3.2.1 Description
7.3.2.2 Model boundary
7.3.2.3 Model class
7.3.2.3.1 Methodology
7.3.2.3.2 Correlation accuracy
7.3.2.4 Transition region (Bob Gannon)
7.3.2.4.1 Description
7.3.2.4.2 Model boundary
7.3.2.4.3 Model class
7.3.2.4.4 Methodology
7.3.2.4.5 Validation
7.3.2.4.5.1 Ribbon or twisted flat cable to IDC connectors
7.3.2.4.5.2 Round cable to connector
7.3.2.4.5.3 Printed circuit board to connector
7.3.2.4.6 Correlation accuracy
7.3.2.5 Connectors (Martin)
7.3.2.5.1 Description
7.3.2.5.2 Model boundary
7.3.2.5.3 Model class
7.3.2.5.4 Methodology
7.3.2.5.5 Validation
7.3.2.5.6 Correlation accuracy
7.3.3 Unpopulated Printed circuit boards
7.3.3.1 Model boundary
7.3.4 Model class
7.3.4.1 Methodology
7.3.4.2 Validation
7.3.4.2.1 Test coupons
7.3.4.2.2 Correlation accuracy
7.4 Devices
7.4.1 Overview
7.4.2 Transceivers
7.4.2.1 Model boundary
7.4.2.2 Model class
7.4.2.3 Methodology
7.4.2.4 Validation
7.4.2.4.1 Correlation accuracy
7.4.3 Terminators (Aloisi)
7.4.3.1 Description
7.4.3.2 Model boundary
7.4.3.3 Model class
7.4.3.4 Description
7.4.3.4.1 Single-ended terminator
7.4.3.4.2 Low-voltage differential terminator

7.4.3.4.2.1 Y terminator
7.4.3.4.2.2 Resistor stack terminator
7.4.3.4.3 Multi-mode terminator
7.4.4 Methodology
7.4.5 Validation
7.4.5.0.1 Correlation accuracy
7.5 Instrumentation models (Jason Chou)
7.5.1 Description
7.5.2 Model boundary
7.5.3 Model Class
7.5.4 Probe models
7.5.5 Methodology
7.5.6 Correlation accuracy

8 Standard model constructions for composite components
8.1 Host bus adapter / target board (X, Umesh)
8.1.1 Description
8.1.2 Model boundary
8.1.3 Model class
8.1.3.1 Methodology
8.2 Cable assemblies (Jason Chou, Bob Gannon, Steve Wong)
8.2.1 Description
8.2.2 Model boundary
8.2.3 Model class
8.2.4 Methodology
8.3 Backplane   (Larry Barnes, Umesh Chandra, Bruce Manildi)
8.3.1 Description
8.3.2 Model boundary
8.3.3 Model class
8.3.4 Methodology
8.4 Terminator – terminator modules (Aloisi)
8.4.1 Description
8.4.2 Model boundary
8.4.3 Model class
8.4.4 Methodology
8.5 System models

9 Measurement and validation (Group) – Break into 2 sections, Measurement points and Validation – Responsibility is the persons defining each device.
9.1 Measurement points
9.1.1 Physical measurement points
9.1.1.1 Transceiver
9.1.1.2 Terminator
9.1.1.3 Transceiver board
9.1.1.4 Transceiver board assembly
9.1.1.5 Cable assemblies (media, transitions, connectors)
9.1.2 Device connector
9.1.3 Chip to board interface
9.1.4 Terminator connector
9.2 Acceptance criteria

10 Validation
10.3 Behavioral model validation procedure
10.3.1 Transceiver
10.4 Circuit model validation procedure
10.4.1 Validation methods
10.4.2 Cable assemblies
10.4.3 Transceiver boards, target boards, and backplanes
10.5 System model validation procedure

11 Simulation strategy
11.1 System configuration
11.2 Data patterns
11.2.1 Overview
11.2.1.1 TDT DATA IN phase training pattern
11.2.1.2 DATAOUT phase training pattern
11.3 Data rates
11.4 Instrumentation models
11.5 System simulation methodologies

Annex A Model database strategy
A.1 Overview
A.2 Location
A.3 Database content
A.4 License/confidentiality agreements
A.4.1 No-fee license agreement

Annex B N-Port Networks
B.1 Overview
B.2 2-Port network parameter conversions

Annex C Basic System Simulation Example (Bill converting Bill Troops work to Frame)

Annex D