Proposal for SPI-5 Programmable Termination   T10/01-270r0

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Purpose: The high frequency attenuation of signals for Fast-320 and higher speeds in cable and backplane systems is a major problem. The high frequency signal can be smaller than the reflected wave from the termination. The loaded cable and backplane high frequency impedance is often much lower than the 85 ohm specification due to the effects of Periodic Structures that create a Comb filter at these frequencies. The 100 -110 ohm termination needs to adjust to the impedance of the loading of the backplane. The backplanes are often designed a the upper range of the impedance limits of 135 ohms, but with the loading of the drives impedances in the 55 ohm range have been commonly seen on these systems.

This proposal changes the differential bias from a voltage to a current specification.

This proposal leaves the nominal termination at 100 to 110 ohms, but allows for an adjustable terminator that is set during the SCSI Domain Validation procedure.

Changes to section 7.3.1 LVD Terminations
Table 20 I-V requirements for differential impedance, common mode impedance, and V_{BIAS} tests.

Note: This table shows the Power up or reset Termination values for Differential impedance. S_1, S_2, V_1, V_2, I_{MAX} and I_{MIN} may be adjusted to match cable and backplane impedance. The values in the table are the power up or reset terminator values.

V_1 and V_2 should be changed to current values for better accuracy, V_1 and V_2 are the effects of current and impedance and should be changed to reflect just the current. V/S = I for I_1 to I_2 range of 1.0 to 1.1 mA.

Table 20 changes

Table 20 - I-V requirements for differential impedance, common mode impedance, and VBIAS tests

Values (figure 33)	Differential impedance and VBIAS tests a (figure 32)	Common mode impedance and VBIAS tests (figure 34)
V_1 (mV)	~~100~~ N/A	1125
V_2 (mV)	~~125~~ N/A	1375
I_1 (mA) *	1.0	N/A
I_2 (mA) *	1.1	N/A
V_3 (V)	1, 0	2,0
V_4 (V)	-1,0	0,5
I_{max} (mA)	9,00	N/A
I_{min} (mA)	-11,25	N/A
S_1 (Ohms)	100	100 **
S_2 (Ohms)	110	300 **
Measurement	D.C.	D.C.
a $V_A + V_B = 2,5 \pm 0,2$ V (figure 32)		
* I = V/S ** Initial values, when S1 and S2 are changed with Domain validation the range is 75 to 400 ohms.		
Note: S_1, S_2, I_1 and I_2 are initial Differential values that are adjusted with Domain Validation to minimize reflections.		

Note: The driver specifications should be changed to current drive, not the voltage into one termination arrangement. The drivers should be rated for system impedances from 55 to 130 ohms, not for a nominal impedance to insure the output cells will perform correctly over the system load range. A loaded backplane may see 55 ohm termination on both ends of the bus, versus 105 ohms. (this is a recommendation for another proposal, but not part of this proposal.)
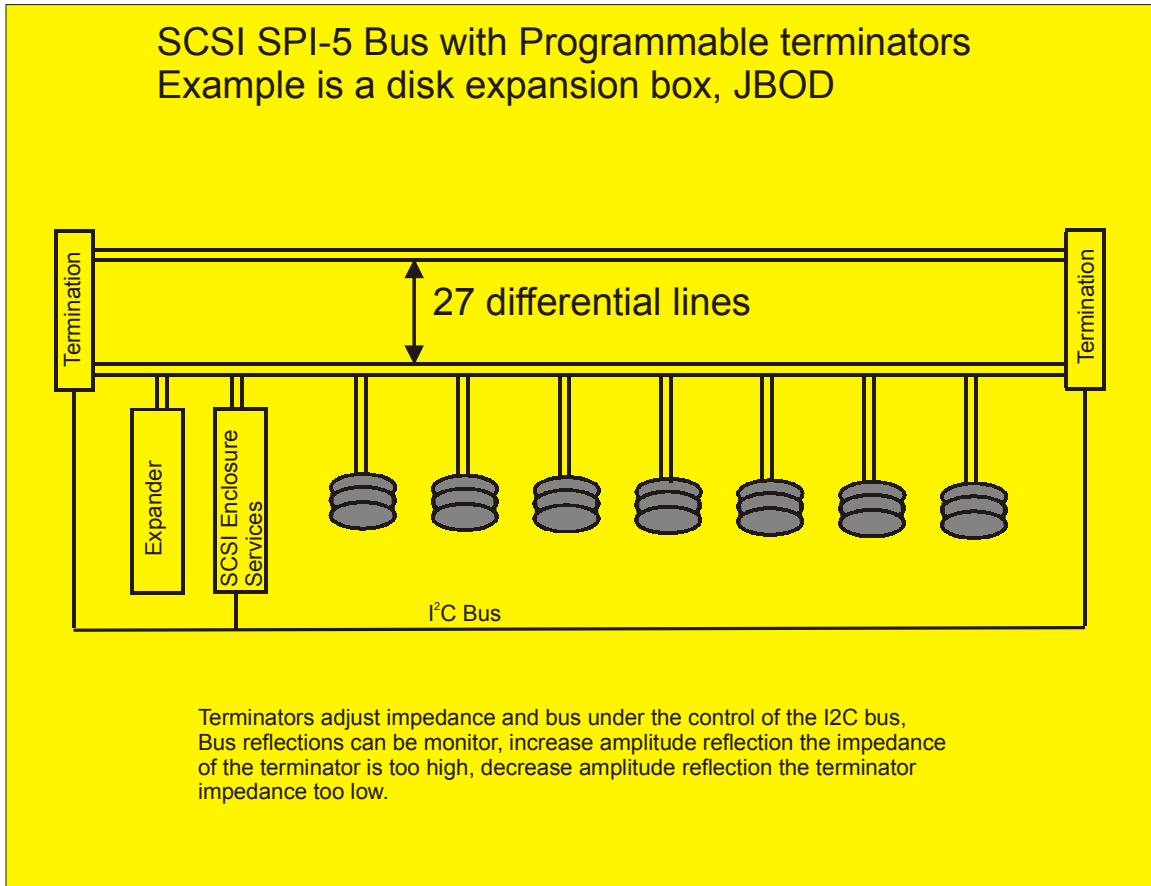
Add a paragraph below Table 20

Programmable terminators shall be adjustable in nominal 5 ohm monotonic steps from the nominal value of 105 ohms to a range between 55 and 130 ohms.

Bias current shall be adjustable in nominal 50 uA monotonic steps from 0.70 mA to 1.45 mA.

An informative annex for the program control of the terminators should be added to SPI-5. The terminator technology does not allow for a terminator that can be controlled directly from the SCSI bus. The SCSI enclosure services controllers normally use I^2C buses to monitor and control the enclosures, the easiest way to

control the terminators is with the I^2C bus. The I^2C bus controller may want to be added to expanders and SCSI controllers.

The control structure proposed is a single word with read/write capability.

SCSI SPI-5 Bus with Programmable terminators
Example is a disk expansion box, JBOD

27 differential lines

Termination

Termination

Expander

SCSI Enclosure Services

I^2C Bus

Terminators adjust impedance and bus under the control of the I2C bus, Bus reflections can be monitor, increase amplitude reflection the impedance of the terminator is too high, decrease amplitude reflection the terminator impedance too low.

New Annex - I^2C control of the SCSI bus terminators

Subject: Annex for SPI-5

Adjustable Terminator control using the I^2C bus

BUS Protocol

The adjustable terminator is configured from a 2-wire, 100khz, Bi -directional bus that is designed for 2.5V to 6V Vcc operation. This is a general-purpose 2-wire remote controlled bus used to adjust the SCSI terminator, controlled via 2-wire interface consisting of (serial clock (SCL), (serial Data (SDA)). The terminator device features 27 line adjustable SCSI termination impedance and separate 27 line adjustable bias for the SCSI Bus. The termination will default initially to a nominal setting on power up. The terminator is controlled by the disconnect signal like a normal SPI-3 terminator until programmed by the I2C bus. The 2-wire bus signals remain high when the 2-wire bus is not busy.

The 2-wire bus consists of 2 bi-directional signals. They are a serial clock (SCL) and serial data (SDA). The bus consists of Master and Slave devices, that maybe operating in a Multi-Master configuration where there maybe one or more masters. Each device has a unique address that is configurable for any one of 128 different addresses. The adjustable terminator is a slave device with Read and Write functions for use in setting the SCSI Bus termination and BIAS. Master devices are typically micro-computers and are the device's issuing the commands on the bus. All other devices on the 2-wire bus are considered slaves.

The terminators have switches to set the address, allowing each terminator to be controlled separately.

The 2-wire serial transmission sequence consists of the following actions. Start, Attention, Compare, Acknowledge, Read Data or Write Data and Stop. The sequence begins with a Start being issued from the master. That start is used as an attention signal for all devices on the bus to listen to the following 8-bit data for their address. When the address compares the slave device will respond to the master with an acknowledge. The master will follow up with either a read or write to the slave device who matched the address. Followed by a stop condition indicating the R/W is complete and the bus has been released. Indicating that the bus is free and is available for another transmission sequence.

Start and Stop is the signaling method for a sequence to initialize. Clock and Data must be high for Start or Stop to be generated. Data can only change while clock is low high during a sequence. During stop and start there maybe data transition while clock is Hi. Normal Data changes only when clock is low. Stop and start are exceptions. Master or slave may hold clock low until all data is processed.

Interface

Communication sequence is initiated with this device by a master sending a start condition, a high –to-low transition on the serial data (SDA) input/output while the serial clock (SCL) input is high. After the start condition, the device address byte

is sent, MSB first, including the data direction bit (R/W). This device does not answer to the general call address, does not support 10bit or 2-byte extended addressing. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA input/output during the high of the acknowledge-related clock pulse. The address inputs of the slave device must not be changed between the start and stop conditions.

The data byte follows the address acknowledge. If the R/W bit is high, the data from this are the values read from the Terminators present setting. The data byte is followed by an acknowledge sent from the device. If other data bytes are sent from the master, following the acknowledge, they are ignored by the device. Data are only output if complete bytes are received and acknowledged. The output data will be valid at time xx after the low-to-high transition of SCL, during the clock cycle for the acknowledge.

Stop condition, a low-to-high transition on the SDA input/output while SCL is high, is sent by the master.