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To: T10 Technical Committee
From: John Lohmeyer, LSI Logic Principal Member of T10
Subj: Clarification of SPI-4 DT Data Group Pad and pCRC Transfers

I have recently been made aware of a hole in the SPI-3 standard that permits a deadlock to occur during the transfer of the pad field and pCRC fields in data group transfers. This hole results from unclear or incomplete requirements being placed on the initiator during the transition from transferring data to the pad field.

The problematic wording persists in SPI-4. I believe that SPI-4 should be clarified as follows:

In 10.7.3.3.5, clarify item 3) of the second list as follows:

- 3) respond with an ACK transition without requiring a subsequent REQ transition.

In 10.7.3.3.6, clarify the following paragraph as follows:

The initiator shall read the value on the DB(15-0) signals within one receive hold time of the transition of the REQ signal. The initiator shall then respond with an ACK transition without requiring a subsequent REQ transition.