ULTRA320 TEST BOARD LICENSE

LSI Logic Corporation ("LSI") is a member of the SCSI Passive Interconnect Performance Working Group of the T10 Technical Committee (the "PIP Working Group") having the goal of identifying a backplane test methodology that will be designated as a Backplane Testing Standard for the PIP Working Group, project 1439-D. LSI developed an Ultra320 Test Board and related documentation (the "Materials") identified in Exhibit A suitable for use in conducting backplane testing, and LSI desires to make the Materials available to other members of the PIP Working Group (the "Group Members") through a round robin exchange. Pursuant to the round robin exchange, each Group Member will have the opportunity to measure test parameters relative to the Ultra320 Test Board as determined by the PIP Working Group before transferring the Materials to the next Group Member participating in the round robin exchange, wherein the results of each Group Members' measuring activity will be provided to the PIP Working Group.

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EXHIBIT A

DESIGNATED MATERIALS

Ultra320 Test Board: G12 Ultra-4 SCSI Buffer test board. Part number 001003-1

or G12 Ultra-4 SCSI Buffer test board. Part number 001003-2

Documentation: SCSI Ultra-4, test PCB. General description (8 pages) Attached.

Schematic diagrams. (5 pages)

LSI LOGIC

SCSI Ultra-4, test PCB. General description.

1. Introduction

There are two board types. The only difference between the two is that one has “on-board” SCSI multi-mode terminators, while the other board does not. In this way, the SCSI interface implementation bears more resemblance to a “Hard drive” (with no on-board terminators) and a “Host Adapter” (which typically has on-board terminators).
The boards are designed as a test vehicle for the L2B1715 SCSI Ultra-4 transceivers, which are implemented in LSI Logic G12P™ technology. The Round Robin test board has "on-board" SCSI miltimode terminators.

2. Board features.

Numerous switches and jumpers on the board are used to control the various functions of the chip and PCB. The detailed list of switches an jumpers are appended to the end of this document.

The twenty seven SCSI buffer I/O’s on the chip are brought out to a 68 pin high density SCSI connector to enable connection to cable media etc. Test points are provided near the SCSI connector to be able to observe each of the differential signal pairs.

The buffers are divided into three groups. Certain SCSI control signals do not need to employ pre-emphasis and are less sophisticated in the way they are internally connected. These are RST, ATN, BSY, MSG, SEL, C/D, I/O.

The rest of the SCSI bus signals are the ones which may be driven in pre-emphasis mode, hence there is a Primary and a Secondary input signal to the buffers.
For this group DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7, DBP, DBP1, REQ and ACK, the Primary data signals are applied to their respective inputs I_xxx and Secondary data signals are applied to their inputs I_xxx_S.
The Primary signal is the data that the “Customer” wishes to transmit. The Secondary signal is the suitably encoded signal which modifies the primary in order to accomplish the pre-emphasis modulation.

An internal encoder is employed for the following buffers. DB8, DB9, D10, DB11, DB12, DB13, DB14 and DB15. For these buffers the “Customer” input data applied to J13, J14 and J17 is encoded automatically. This is much simpler to use because any data pattern can be inserted without having to encode an external input for the Secondary driver.

There are two ways to transmit the data to the SCSI buffers. Synchronous mode or Asynchronous mode. This function is controlled by J74. In Asynchronous mode, the data from the internal core of the chip goes straight out through the buffer without any type of synchronization.
When the SCSI buffers are selected to operate in Synchronous mode The data is latched internally and synchronized by a clock.
There are two ways to do this. Firstly the “internal” method is where the 160 MHz clock from the “on-chip” PLL circuit. CLK_SEL (U9-2) is switched ON. Alternatively, with U9-2 switched OFF, an external

clock source is supplied to J11. Remember that the maximum data frequency is 80 MHz. The clock needs to be 160 MHz. (Always twice the data frequency.)

Primary data input signals to the SCSI buffer are labeled as I_xxx. (e.g. I_REQ)
Secondary data input signals are labeled as I_xxx_S. (e.g. (I_REQ_S)
The differential bi-direct output pins are labeled as xxx_PADM and xxx_PADP.
The Receiver output signals are labeled as Z_xxx.
Refer to the schematic diagram for the test points and connectors to gain access to these signals.

The LVD and SE drivers have 8 programmable levels of slew rate control. These are set by switches U8-2, U8-3 and U8-4.

The LVD driver has programmable drive strength. The Primary driver circuit has 8 programmable settings controlled by U8-8, U8-9 and U8-10. The Secondary driver circuit also has 8 settings controlled by U8-11, U8-12 and U9-1. These combinations provide a total of 64 different drive strengths each for "Standard" mode and for "Pre-emphasis" mode.
(Pre-emphasis mode is where drive strength is "cutback" after 1 clock period if there has not been a signal transition.)

5 Volt termpower can be provided to the SCSI connector, depending on the jumper configuration of J5.

For the board which has "on-board" SCSI multi-mode terminators, U15-2 is used to electrically enable/disable the terminator circuits.

3. Electrical/Power Requirements

One external regulated power supply at 5 VDC. (> 2 Amps) is used to provide primary power to the board. A "LINEAR" power supply is much preferred over a "SWITCHING" type of supply.

The PC board has regulators to provide 3.3VDC and 1.8 VDC to the chip and test circuits.

4. Quick reference Switch and Jumper settings.

Switch settings for Transmit / Receive					
Switch	**LVD transmit**	**SE transmit**	**LVD Receive**	**SE Receive**	
U8-1	OFF	OFF	OFF	OFF	
U8-2	OFF	OFF	OFF (NA)	OFF (NA)	Slew rate control switches.
U8-3	OFF	OFF	OFF (NA)	OFF (NA)	
U8-4	OFF	OFF	OFF (NA)	OFF (NA)	
U8-5	ON	ON	ON	ON	
U8-6	ON	ON	ON	ON	
U8-7	ON	ON	ON	ON	Reset chip by switching OFF then ON again.
U8-8	OFF	OFF (NA)	OFF (NA)	OFF (NA)	LVD Primary driver strength settings.
U8-9	ON	OFF (NA)	OFF (NA)	OFF (NA)	
U8-10	ON	OFF (NA)	OFF (NA)	OFF (NA)	
U8-11	OFF	OFF (NA)	OFF (NA)	OFF (NA)	LVD Secondary driver strength settings.
U8-12	OFF	OFF (NA)	OFF (NA)	OFF (NA)	
U9-1	OFF	OFF (NA)	OFF (NA)	OFF (NA)	
U9-2	ON	ON	ON (NA)	ON (NA)	Internal / External clock select.
U9-3	OFF	OFF	OFF	OFF	
U9-4	ON	OFF	ON	OFF	LVD / SE mode select
U9-5	OFF (NA)	OFF	OFF (NA)	OFF (NA)	Active negation switch (SE only)
U9-6	OFF (NA)	OFF (NA)	OFF (NA)	OFF (NA)	
U9-7	OFF	OFF (NA)	OFF (NA)	OFF (NA)	
U9-8	OFF (NA)	OFF (NA)	OFF (NA)	OFF (NA)	
J74-1	to J74-2	to J74-2	(NA)	(NA)	Synchronous mode select.
U9-10	OFF (NA)	OFF (NA)	OFF (NA)	OFF (NA)	
U9-11	ON	ON	OFF	OFF	Transmitter enable switch
U9-12	OFF (NA)	OFF (NA)	OFF (NA)	OFF (NA)	
U15-1	ON	ON (NA)	ON (NA)	ON (NA)	LVD Precomp. enable switch
U15-2	ON	ON	ON	ON	Enable on-board terminators. (If applicable)

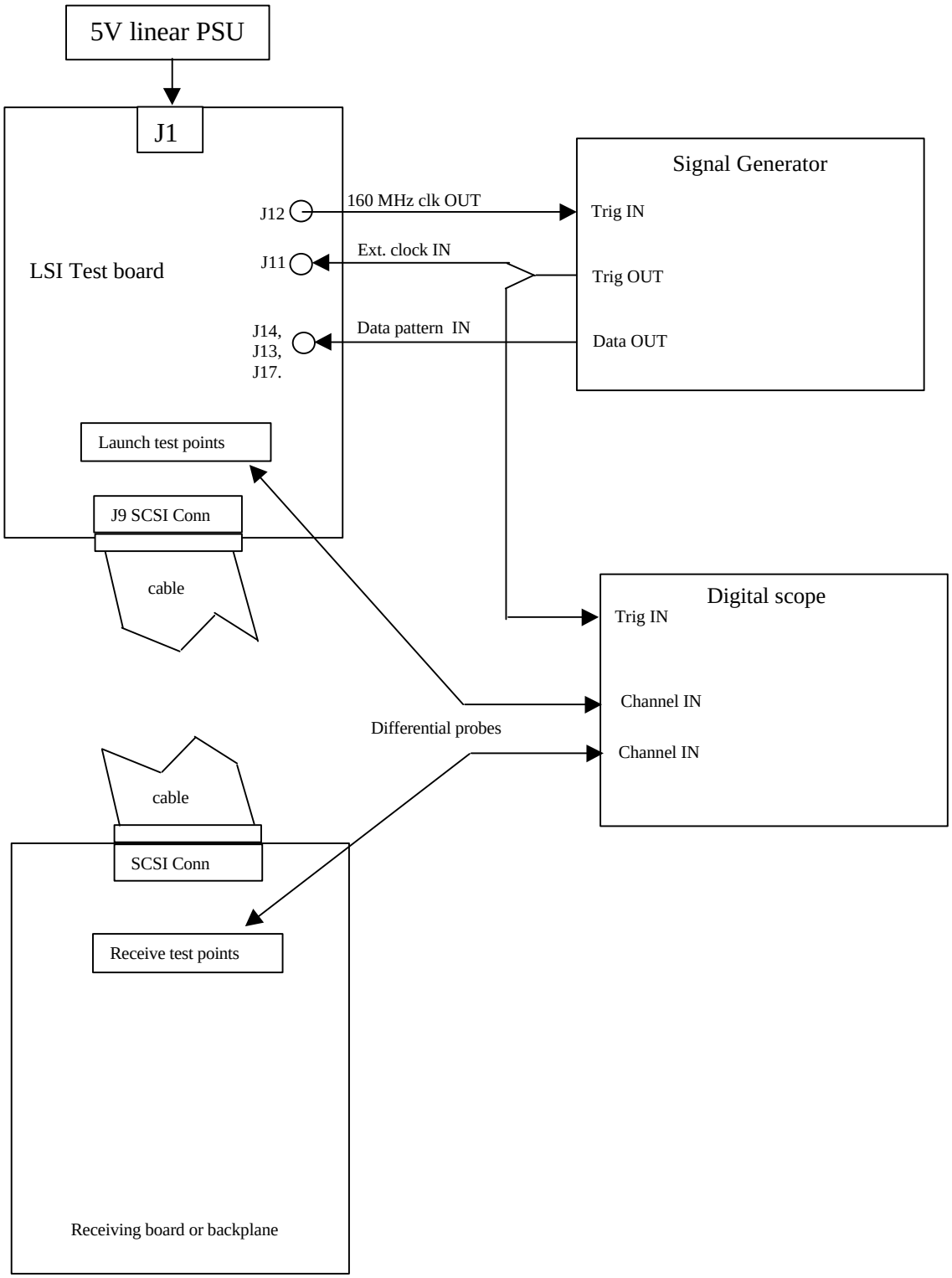
(N/A) means switch does nothing in this mode.

Default Jumper settings.

Jumper From	**Jumper To**	**Function**
J2-1	J2-2	1.8V power
J3-1	J4-1	3.3V power
J3-2	J4-2	3.3V power
J5-1	J5-2	5V “Termpower” to SCSI connector.
J6-2	J6-4	Supply variable voltage source to cable diffsense line.
J8-1	J8-2	Voltage supply to Bias resistor.
J110-1	J110-2	SCSI output breakpoints
J111-1	J111-2	
J112-1	J112-2	
J113-1	J113-2	
J127-1	J127-2	Provide 5V power to Terminator resistors.

5. Configuration for cable / back-plane signal testing.

Typical and simplest configuration.



Programmable settings.

LVD Driver Slew rate control.

Slew rate control bits.			
U8-4	U8-3	U8-2	Nominal Rise/Fall ns
ON	ON	ON	3.0
ON	ON	OFF	2.33
ON	OFF	ON	1.91
ON	OFF	OFF	1.61
OFF	ON	ON	1.40
OFF	ON	OFF	1.23
OFF	OFF	ON	1.10
OFF	OFF	OFF	1.0

Slew rate control. (Single Ended driver).

Slew rate control bits.			
U8-4	U8-3	U8-2	Slew rate mV/ns (nom). Measured between 0.7V and 2.3V
ON	ON	ON	220
ON	ON	OFF	240
ON	OFF	ON	260
ON	OFF	OFF	280
OFF	ON	ON	300
OFF	ON	OFF	320
OFF	OFF	ON	340
OFF	OFF	OFF	360

LVD Driver strengh

The LVD Drive current strength is made up of 3 factors. First the Primary current. Then the Secondary current is added or subtracted to the primary. (Depending on whether Pre-emphasis is Enabled or Disabled). Then a constant 2mA bias current is applied. (Terminator bias cancellation.)

Therefore the calculations for final currents are:

No CUTBACK
Assertion current = Primary current + Secondary current + 2 mA
Negation current = Primary current + Secondary current - 2 mA

With CUTBACK
Assertion current = Primary current - Secondary current + 2 mA
Negation current = Primary current - Secondary current - 2 mA

The LVD Primary driver current has eight programmable settings as determined by the switch settings as shown in this table.

SP0 U8-8	SP1 U8-9	SP2 U8-10	Primary Drive mA
ON	ON	ON	6.75
ON	ON	OFF	7.50
ON	OFF	ON	8.25
ON	OFF	OFF	9.00
OFF	ON	ON	9.75
OFF	ON	OFF	10.50
OFF	OFF	ON	11.25
OFF	OFF	OFF	12.00

The Secondary driver will add/subtract by the percentages shown in this table.

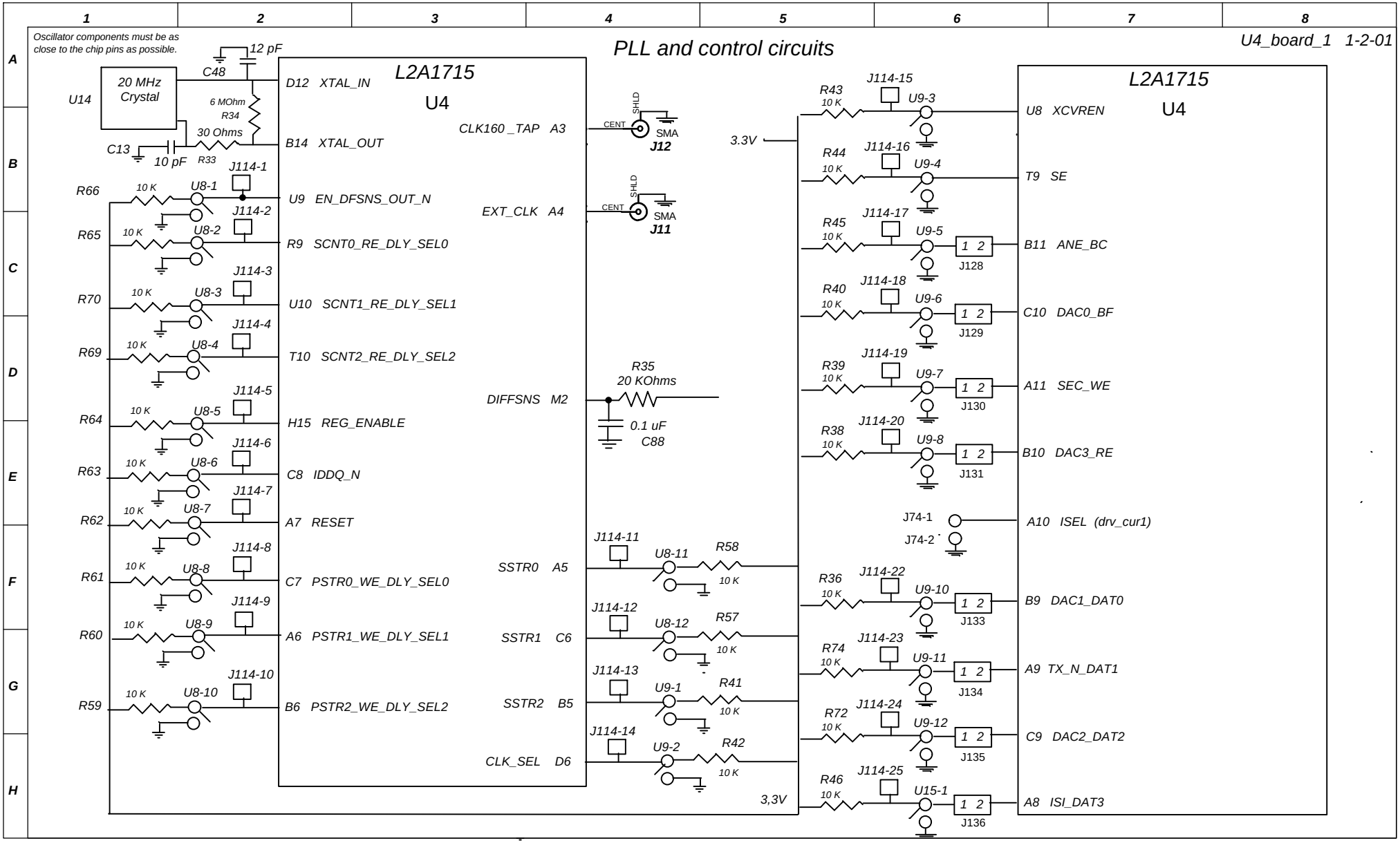
SS0 U8-11	SS1 U8-12	SS2 U9-1	Secondary Driver
ON	ON	ON	+/- 4.17 %
ON	ON	OFF	+/- 8.33 %
ON	OFF	ON	+/- 12.5 %
ON	OFF	OFF	+/- 16.67 %
OFF	ON	ON	+/- 20.83 %
OFF	ON	OFF	+/- 25.00 %
OFF	OFF	ON	+/- 29.17 %
OFF	OFF	OFF	+/- 33.33 %

Jumper and switch functions. (more details)

Switch	Signal	Function	Effect
U8-1	EN_DFSNS_OUT_N	Diffsense Receiver control	ON = Low = Enable OFF = High = Disable
U8-2	SCNT0_RE_DLY_SEL0	Slew rate control LSD	ON = Low OFF = High
U8-3	SCNT1_RE_DLY_SEL1	Slew rate control	ON = Low OFF = High
U8-4	SCNT2_RE_DLY_SEL2	Slew rate control MSD	ON = Low OFF = High
U8-5	REG_ENABLE and Miscellaneous	Voltage Regulator control Needs to be ON to permit input signals ANE etc.	ON = Low = Enable OFF = High = Disable
U8-6	IDDQ_N	Controls High-Z leakage test function for entire chip	ON = Low = Disable leakage test OFF = High = Enable leakage test
U8-7	RESET	Reset for entire chip	ON = Low = Disable RESET OFF = High = Enable RESET
U8-8	PSTR0_WE_DLY_SEL0	Primary Drive strength. LSD	ON = Low OFF = High
U8-9	PSTR1_WE_DLY_SEL1	Primary Drive strength. LSD	ON = Low OFF = High
U8-10	PSTR2_WE_DLY_SEL2	Primary Drive strength. MSD	ON = Low OFF = High
U8-11	SSTR0	Secondary drive strength LSD.	ON = Low OFF = High
U8-12	SSTR1	Secondary drive strength	ON = Low OFF = High
U9-1	SSTR2	Secondary drive strength. MSD	ON = Low OFF = High
U9-2	CLK_SEL	Clock select switch.	ON = Internal 160 MHz clk OFF = External clk.
U9-3	XCVREN	Transceiver enable	ON = Low = Disable transceiver OFF = High = Enable transceiver
U9-4	SE	Mode control for SE and LVD	ON = Low = LVD OFF = High = SE.
U9-5	ANE_BC	Active Negation Enable	ON = Low = Disable Active neg. OFF = High = Enable Active neg.
U9-6	DAC0_BF	DAC0 for Voltage Regulator BF for Register file.	ON = Low OFF = High
U9-7	SEC_WE	Secondary driver disable	ON = Low = Disable secondary Dr OFF =High = Enable secondary Dr
U9-8	DAC3_RE	DAC3 for Voltage Regulator RE for Register file	ON = Low OFF = High
J74-1	ISEL	Select Synch or Asynch. mode.	J74-1 jumper to J74-2 = Low = Synchronous mode J74-1 open = Asynchronous mode

U9-10	DAC1_DAT0	DAC1 for Voltage Regulator DAT0 for Register file	ON = Low OFF = High
U9-11	TX_N_DAT1	Transmit enable	ON = Low = Enable transmit OFF = High = Disable transmit
U9-12	DAC2_DAT2	DAC2 for Voltage Regulator DAT2 for Register file	ON = Low OFF = High
U15-1	ISI_DAT3	Pre-compensation enable.	ON = Low = Disable Pre-comp OFF = High = Enable Pre-comp.
U15-2	Disconnect (Terminator board only)	Control on-board terminators.	ON = Low = Enable Term. OFF = High = Disable Term.

Jumper	**Signal**	**Function/Effect**
J1	5 Volt	Main power connector.
J2-1,2,3,4,5	1.8V power	See Schematic
J3, J4	3.3V power	Short to connect power to chip
J5-1,2	5 Volt power	Short to supply “Termpower” to SCSI connector and resistor chips
J6-1,2,3,4	Variable V source	See Schematic
J7-1, J7-2	5V and 0V	Test point for 5V. DO NOT SHORT
J8	BIAS1	Short to enable voltage supply to Bias resistor.
J9	SCSI	SCSI bus connector
J10	PWR_GOOD	Test point for Voltage regulator
J110, 111, 112 ,113	SCSI outputs	See Schematic
J114-n	Test points	See Schematic
J127-1, 2		Short to provide 5V power to Terminator resistors.
All others	Test points	See Schematic


PLL and control circuits
U4_board_1 1-2-01
Oscillator components must be as close to the chip pins as possible.
L2A1715
U4
U14
20 MHz Crystal
C48
12 pF
6 MOhm
R34
30 Ohms
C13
10 pF
R33
D12 XTAL_IN
B14 XTAL_OUT
CLK160 _TAP A3
EXT_CLK A4
DIFFSNS M2
SSTR0 A5
SSTR1 C6
SSTR2 B5
CLK_SEL D6
U9 EN_DFSNS_OUT_N
R9 SCNT0_RE_DLY_SEL0
U10 SCNT1_RE_DLY_SEL1
T10 SCNT2_RE_DLY_SEL2
H15 REG_ENABLE
C8 IDDQ_N
A7 RESET
C7 PSTR0_WE_DLY_SEL0
A6 PSTR1_WE_DLY_SEL1
B6 PSTR2_WE_DLY_SEL2
CENT
SHLD
SMA
J12
J11
R35
20 KOhms
0.1 uF
C88
3.3V
3,3V
R66
R65
R70
R69
R64
R63
R62
R61
R60
R59
10 K
U8-1
U8-2
U8-3
U8-4
U8-5
U8-6
U8-7
U8-8
U8-9
U8-10
J114-1
J114-2
J114-3
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J114-5
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J114-12
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U8-11
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U9-2
R58
R57
R41
R42
R43
R44
R45
R40
R39
R38
R36
R74
R72
R46
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J114-18
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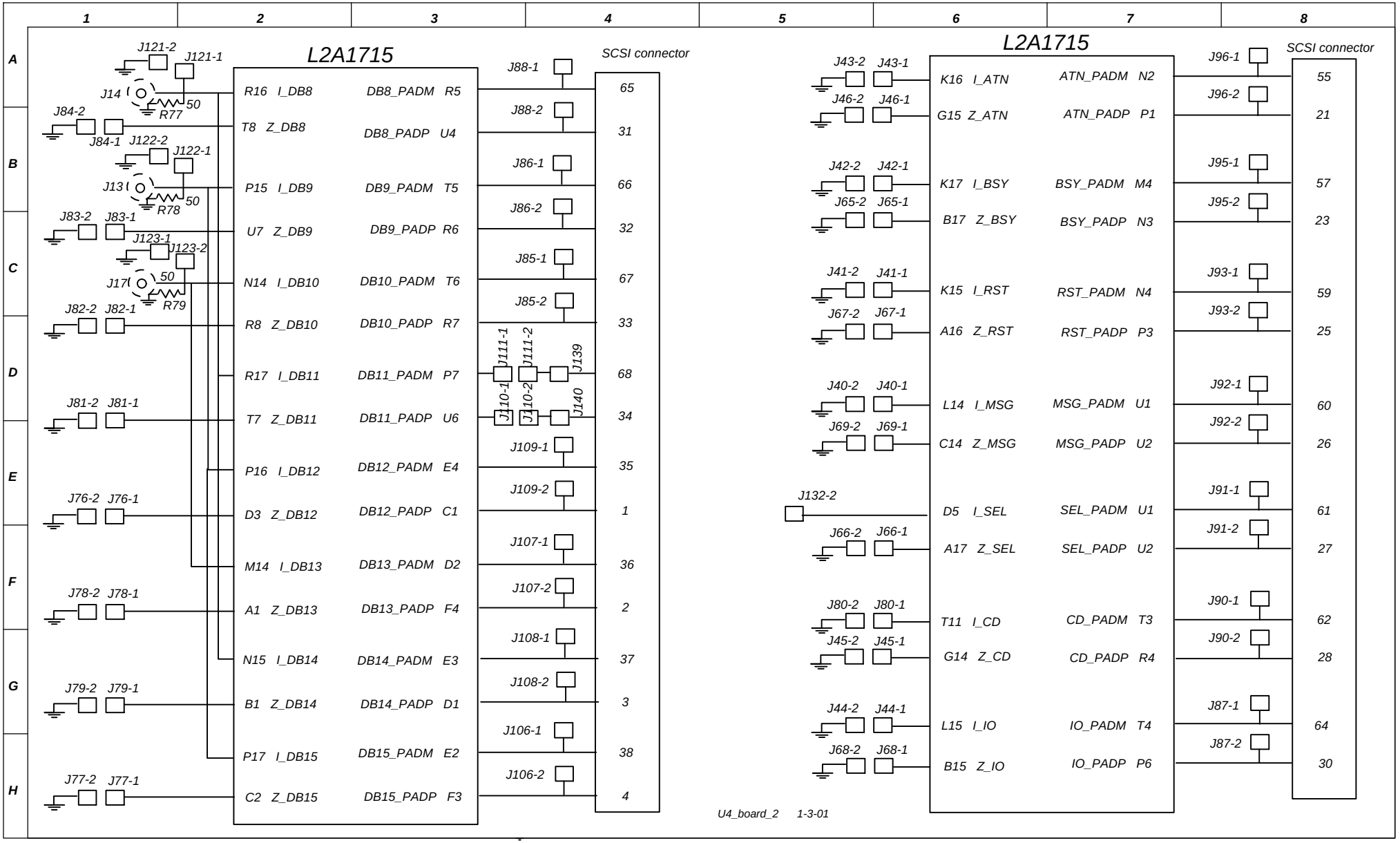
U9-4
U9-5
U9-6
U9-7
U9-8
U9-10
U9-11
U9-12
U15-1
1 2
J128
J129
J130
J131
J133
J134
J135
J136
J74-1
J74-2
U8 XCVREN
T9 SE
B11 ANE_BC
C10 DAC0_BF
A11 SEC_WE
B10 DAC3_RE
A10 ISEL (drv_cur1)
B9 DAC1_DAT0
A9 TX_N_DAT1
C9 DAC2_DAT2
A8 ISI_DAT3


L2A1715
SCSI connector
R16 I_DB8
T8 Z_DB8
P15 I_DB9
U7 Z_DB9
N14 I_DB10
R8 Z_DB10
R17 I_DB11
T7 Z_DB11
P16 I_DB12
D3 Z_DB12
M14 I_DB13
A1 Z_DB13
N15 I_DB14
B1 Z_DB14
P17 I_DB15
C2 Z_DB15
DB8_PADM R5
DB8_PADP U4
DB9_PADM T5
DB9_PADP R6
DB10_PADM T6
DB10_PADP R7
DB11_PADM P7
DB11_PADP U6
DB12_PADM E4
DB12_PADP C1
DB13_PADM D2
DB13_PADP F4
DB14_PADM E3
DB14_PADP D1
DB15_PADM E2
DB15_PADP F3
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J88-2
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J85-1
J85-2
J111-1
J111-2
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J110-1
J110-2
J140
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J107-1
J107-2
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35
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36
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37
3
38
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J121-2
J121-1
J14
50
R77
J84-2
J84-1
J122-2
J122-1
J13
50
R78
J83-2
J83-1
J123-1
J123-2
J17
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R79
J82-2
J82-1
J81-2
J81-1
J76-2
J76-1
J78-2
J78-1
J79-2
J79-1
J77-2
J77-1
L2A1715
SCSI connector
K16 I_ATN
G15 Z_ATN
K17 I_BSY
B17 Z_BSY
K15 I_RST
A16 Z_RST
L14 I_MSG
C14 Z_MSG
D5 I_SEL
A17 Z_SEL
T11 I_CD
G14 Z_CD
L15 I_IO
B15 Z_IO
ATN_PADM N2
ATN_PADP P1
BSY_PADM M4
BSY_PADP N3
RST_PADM N4
RST_PADP P3
MSG_PADM U1
MSG_PADP U2
SEL_PADM U1
SEL_PADP U2
CD_PADM T3
CD_PADP R4
IO_PADM T4
IO_PADP P6
J96-1
J96-2
J95-1
J95-2
J93-1
J93-2
J92-1
J92-2
J91-1
J91-2
J90-1
J90-2
J87-1
J87-2
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28
64
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J43-2
J43-1
J46-2
J46-1
J42-2
J42-1
J65-2
J65-1
J41-2
J41-1
J67-2
J67-1
J40-2
J40-1
J69-2
J69-1
J132-2
J66-2
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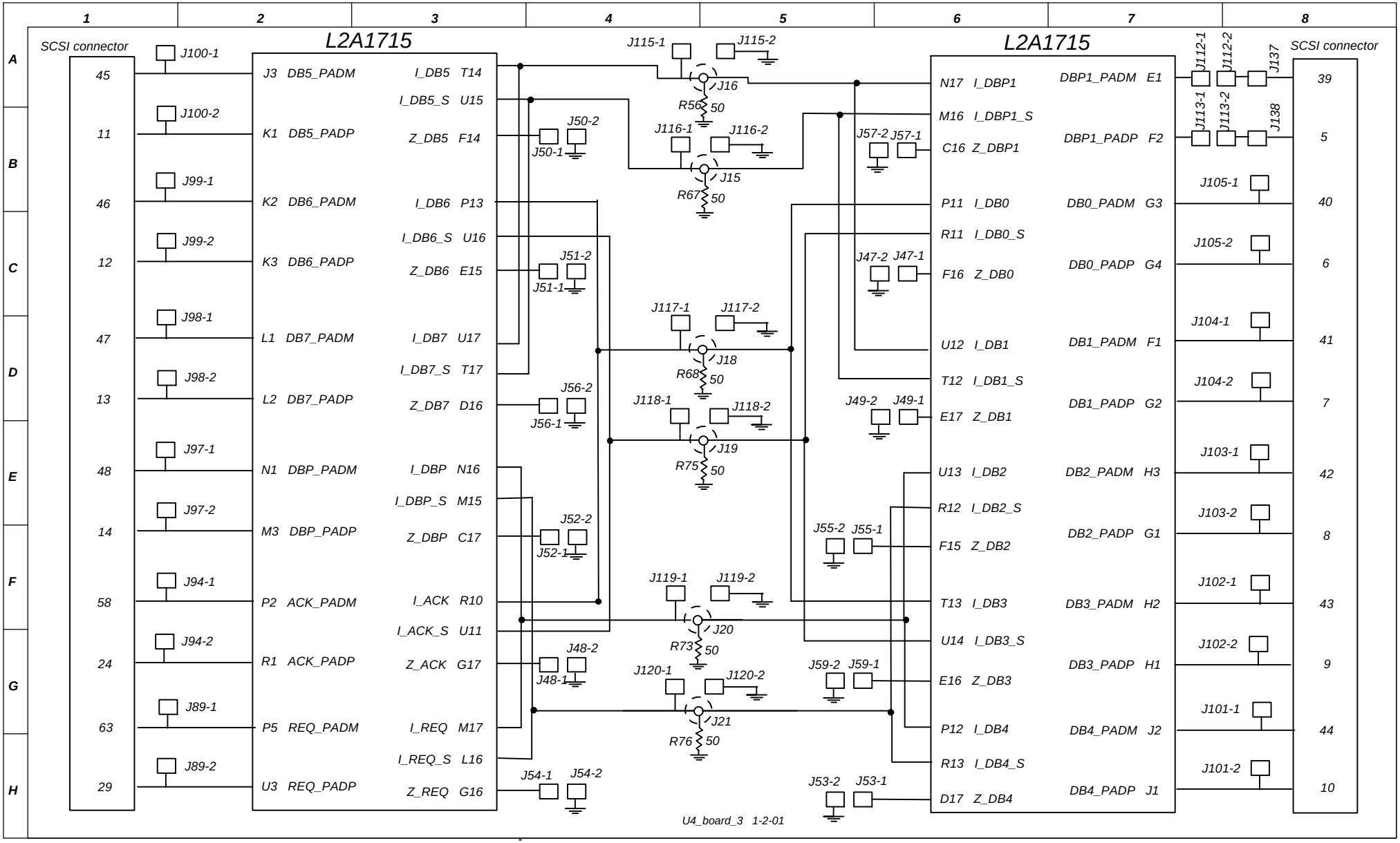
U4_board_2 1-3-01


SCSI connector
L2A1715
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SCSI connector
J100-1
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J97-2
J94-1
J94-2
J89-1
J89-2
J3 DB5_PADM
K1 DB5_PADP
K2 DB6_PADM
K3 DB6_PADP
L1 DB7_PADM
L2 DB7_PADP
N1 DBP_PADM
M3 DBP_PADP
P2 ACK_PADM
R1 ACK_PADP
P5 REQ_PADM
U3 REQ_PADP
I_DB5 T14
I_DB5_S U15
Z_DB5 F14
I_DB6 P13
I_DB6_S U16
Z_DB6 E15
I_DB7 U17
I_DB7_S T17
Z_DB7 D16
I_DBP N16
I_DBP_S M15
Z_DBP C17
I_ACK R10
I_ACK_S U11
Z_ACK G17
I_REQ M17
I_REQ_S L16
Z_REQ G16
J115-1
J115-2
J16
R56 50
J116-1
J116-2
J15
R67 50
J117-1
J117-2
J18
R68 50
J118-1
J118-2
J19
R75 50
J119-1
J119-2
J20
R73 50
J120-1
J120-2
J21
R76 50
J50-2
J50-1
J51-2
J51-1
J56-2
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J55-2
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J59-2
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J53-2
J53-1
N17 I_DBP1
M16 I_DBP1_S
C16 Z_DBP1
P11 I_DB0
R11 I_DB0_S
F16 Z_DB0
U12 I_DB1
T12 I_DB1_S
E17 Z_DB1
U13 I_DB2
R12 I_DB2_S
F15 Z_DB2
T13 I_DB3
U14 I_DB3_S
E16 Z_DB3
P12 I_DB4
R13 I_DB4_S
D17 Z_DB4
DBP1_PADM E1
DBP1_PADP F2
DB0_PADM G3
DB0_PADP G4
DB1_PADM F1
DB1_PADP G2
DB2_PADM H3
DB2_PADP G1
DB3_PADM H2
DB3_PADP H1
DB4_PADM J2
DB4_PADP J1
J112-1
J112-2
J137
J113-1
J113-2
J138
J105-1
J105-2
J104-1
J104-2
J103-1
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J102-1
J102-2
J101-1
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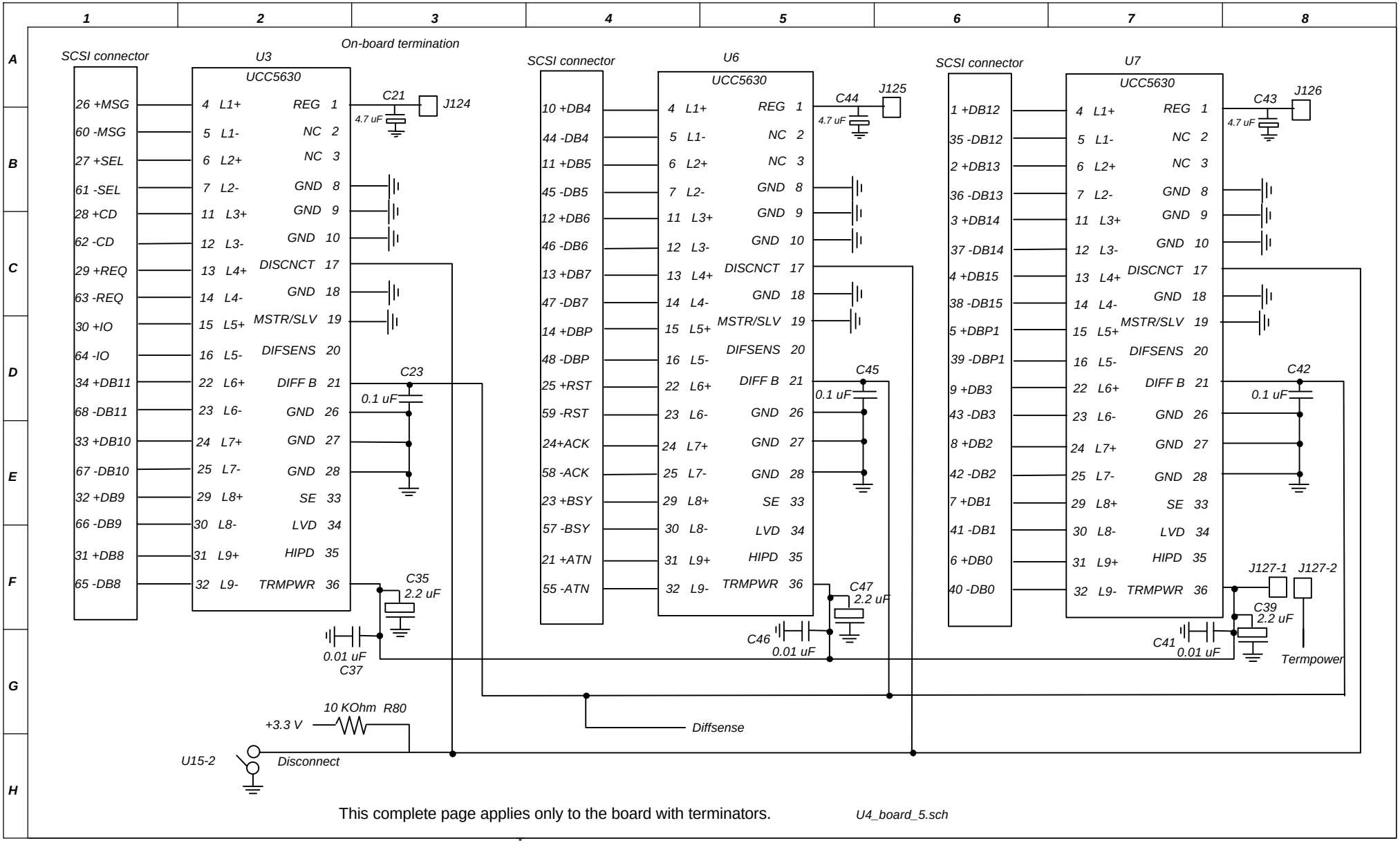
U4_board_3 1-2-01



This complete page applies only to the board with terminators.

U4_board_5.sch

G12 Ultra-4 SCSI BUFFER TEST BOARD.

Power distribution