Backplane Round Robin 1
Test Plan - SCSI PIP
T10/01-132r2
Umesh Chandra

Overview

The objective of this Round Robin is to use a standardized method to characterize Backplanes. Two backplanes will be provided for this Round Robin: 1) Harbor, 2) Intel.

The "eye pattern" method will be used to characterize the two backplanes. A detailed description of how to generate eye patterns is presented in this report.

In addition to measuring "eye patterns", transient data patterns will be captured using a single ended and differential probes. "Attenuation" measurements will be made, a detailed description follows.

Documentation

The following LSI Logic documents are required for using this Test Plan:

1) U320 testboard_Agreement.PDF (License Agreement)

2) SCSI_Ultra_4_testboard.PDF (General Description)

3) U4_board_PWR.PDF (Test board block diagram)

4) U4_board_1.PDF (Circuit schematic page 1)

5) U4_board_2.PDF (Circuit schematic page 2)

6) U4_board_3.PDF (Circuit schematic page 3)

7) U4_board_4.PDF (Circuit schematic page 4)

8) U4_board_5.PDF (Circuit schematic page 5)

9) Impedence Measurement - (Larry Barnes)

Test Board

Use SCSI_Ultra_4_testboard.PDF for detailed descriptions of the Test Board, all page numbers are with reference to this document. Read this document before starting this Test Plan.

1) Test board type used for this Test Plan has 'on-board' SCSI multi-mode terminators, which will be enabled for all tests - see page 1.

2) Below are the U8, U9 and U15 DIP switch settings (On is marked on the switch, see page 3 for switch functionality).

U8

1	2	3	4	5	6	7	8	9	10	11	12
off	on	off	on	on	on	on	off	on	on	on	on

U9

1	2	3	4	5	6	7	8	9	10	11	12
off	on	off	on	off	off	off	off	off	off	on	on

U15

1	2	3	4	5	6	7	8	9	10	11	12
on	on	<---------- not used---------->									

Test Equipment

The following test equipment was used by Seagate and is recommended for the Test Plan. However other equipment can be used, but results may be different. In order to standardize the "eye pattern" collection format, it is strongly recommended that a Tektronix 600 or 700 series digital scope be used, so that data can be readily captured, compared and interchanged between the Round Robin participants.

1) Digital Oscilloscope - TEK684B, 1 GHz, 5 GS/s, 4 channel

2) Differential Probe - TEK P6247, 1 GHz, input impedance 200Kohm in parallel with <1pF

3) Single Ended probe - TEK P6205, FET Probe, 750 MHz, <2pF, 1 Mohm, 10X

3) Arbitrary Waveform Generator - TEK AWG2040, clock freq. 1 GHz, 8 bit DA converter, 1 M word waveform memory. If a TEK610 is used, a built in utility needs to be run to convert the random waveforms in a WFM format, sent with the Round Robin, to the TEK610 WFM format. Even though the .wfm extension is the same, the formats are different between the AWG 2040 and the AWG 610.

4) SMA to BNC cables and 50 ohm terminators as required by the particular termination requirements of equipment used

5) LSI Logic G12 Ultra-4 SCSI Buffer Test Board with LSI TSTCHIP3 installed (supplied)

6) 2 X 5 slot Harbor Backplane with differential probe test points on DB10 and DB13 (supplied)

7) Twist and Flat cable assembly (Supplied), short (.25") and 18". A short rigid Interposer PCB was considered, but due to fixturing constraints and required flexing, this approach was abandoned.

8) 5 plug in Seagate Drive PCBs (supplied)

9) 'Random.wfm' and 'Signalamplitude.wfm' data patterns on a floppy, required by the AWG2040 (supplied)

External terminators are not required for this test.

Test Configuration - LSIL Test Board to AWG

Please reference page 4 of the SCSI_Ultra_4_testboard.PDF document for configuring the Test Board.

1) The LSIL Test Board power connector is a standard 4 pin SCSI connector, only 5 Vdc and GND are required.

2) Connect 'J12' (160MHz clk OUT, LSIL Test Board) to 'Trig IN'(external trigger input of AWG). The random data generated by the AWG will then be synchronized with the the 160 MHz clock from the LSI Logic test chip.

3) DO NOT CONNECT 'J11' to 'Trig OUT'(trigger out of AWG). This connection is only used if the AWG is used to trigger the Test Chip. In our test plan, the Test Chip is used to trigger the AWG.

4) Connect 'J17'(LSIL Test Board) to 'Data OUT'(data pattern output of AWG). This injects random data into DB10 and DB13 of the LSI Logic Test Chip.

5) Connect 'J13'(LSIL Test Board) to 'Data OUT, inverted' (inverted data pattern output of AWG). This injects random data (inverted with respect to DB10 and DB13) into DB9, DB12 and DB15. This is used to simulate a worst case cross talk signal. 'J14' is internally connected to 'J13' on the Test Board. This injects the same cross talking signal, into DB8, DB11 and DB14. To summarize:

Data pattern IN (AWG) - DB10 and DB13 (LSIL Test Chip)

Cross Talk (inverted Data Pattern IN, AWG) - DB8, DB9, DB11, DB12, DB14 and DB15 (LSIL Test Chip)

Experiment is repeated with using the inverted Data Pattern IN ,AWG, for DB10 and DB13 and Data Pattern IN, AWG for the Cross Talking signal.

Test Configuration - LSIL Test Board to Digital Scope

Please reference page 4 of the SCSI_Ultra_4_testboard.PDF document for configuring the Test Board.

1) Connect J12, 160 MHz clk OUT (LSIL Test Board) to Channel 4 (Trigger input for Digital Scope).

2) Connect 'Launch test points, DB10 or DB13' (Jumper block LSIL Test Board, to the left of the 68 pin SCSI connector) to Channel 1 (Differential Probe Digital Scope).
J85 is the (-) DB10 output, the (+) DB10 output is the adjacent jumper pin.
J107 is the (-) DB13 output, the (+) DB13 output is the adjacent jumper pin)

3) Similar type of connections, measurements can be done on the REQ and ACK signals, near end and far end. For connection details refer to the LSIL Documentation and circuit schematics.

Test Config - Harbor Backplane to LSIL Test Board & Digital Scope

Please reference page 4 of the SCSI_Ultra_4_testboard.PDF document for configuring the Test Board.

1) Connect 'Receive test points, DB10 or DB13 on the back of the 80 pin SEA connector of the Harbor Backplane, at each of the slot positions (1 through 10) to Channel 2 (Differential Probe Digital Scope).

2) Connect J9, 68 pin SCSI connector (LSIL Test Board) to J14 or J13, 68 pin SCSI connector (Harbor backplane) using the SCSI twist and flat cable provided.

3) Harbor Backplane

The backplane has two independent 5 slot backplanes, each has its own terminator. If the SCSI cable is connected to J14, then drive slots 1, 2, 3, 4 and 5 are active, the terminator is closest to drive slot 5.
If the SCSI cable is connected to J13, then drive slots 6, 7, 8, 9 and 10 are active, the terminator is closest to drive slot 10.

Each of the 5 slot backplanes have a separate 4 pin standard SCSI power connector.

Similar type of connections, measurements can be done on the REQ and ACK signals, near end and far end. For connection details refer to the LSIL Documentation and circuit schematics.

Attenuation Measurement Method

Load the 'signalamplitude.wfm" waveform into the AWG2040 or equivalent. The 'signalamplitude.wfm' waveform has a low frequency of 1 MHz (to simulate DC), followed by a burst of 80MHz.

Measure the peak to peak differential amplitude of the 1 MHz at the 'launch test points' for DB10 and DB13, refer to page 6 for connection information. This measurement gives the low frequency or DC amplitude at the driver output of the LSIL Test Chip. This measurement is made using the horizontal cursors on the TEK scope. The cursors can be selected by pressing the 'Cursor' button and then the 'Horizontal' button. The 'launch test point' amplitude measurement is made only once.

Measure the peak to peak differential amplitude of the 80 MHz at the 'receive test points' for DB10 and DB13, refer to page 7 for connection information. This measurement gives the high frequency amplitude at the backplane slot (receiver end). Repeat this measurement for slot positions 1 -5 and 6 -10. Use horizontal cursors to make this measurement.

Attenuation = 20 log (peak-peak amplitude at receive test point / peak-peak amplitude at launch)

Verify calibration by making single ended amplitude measurements.

Trigger Method for Eye Pattern Generation

1) Channel 4 - Trigger from J12 on LSIL Test board, 160MHz clk Out

Trigger - Normal

Type - Edge

Source - CH4

Coupling - DC

Slope - +

Adjust trigger level to get a stable trigger on the clock signal.

2) Channel 1 or 2

Vertical - Channel 1 or 2

Coupling - Dc

Bandwidth - full

Fine Scale - 200mv/div

Position - 0 div

Offset - 0 v

Deskew - 0 s

3) Display Settings - Infinite Persistence

Horizontal - 1 nsec/div

Data Points - 500

4) Saving Data

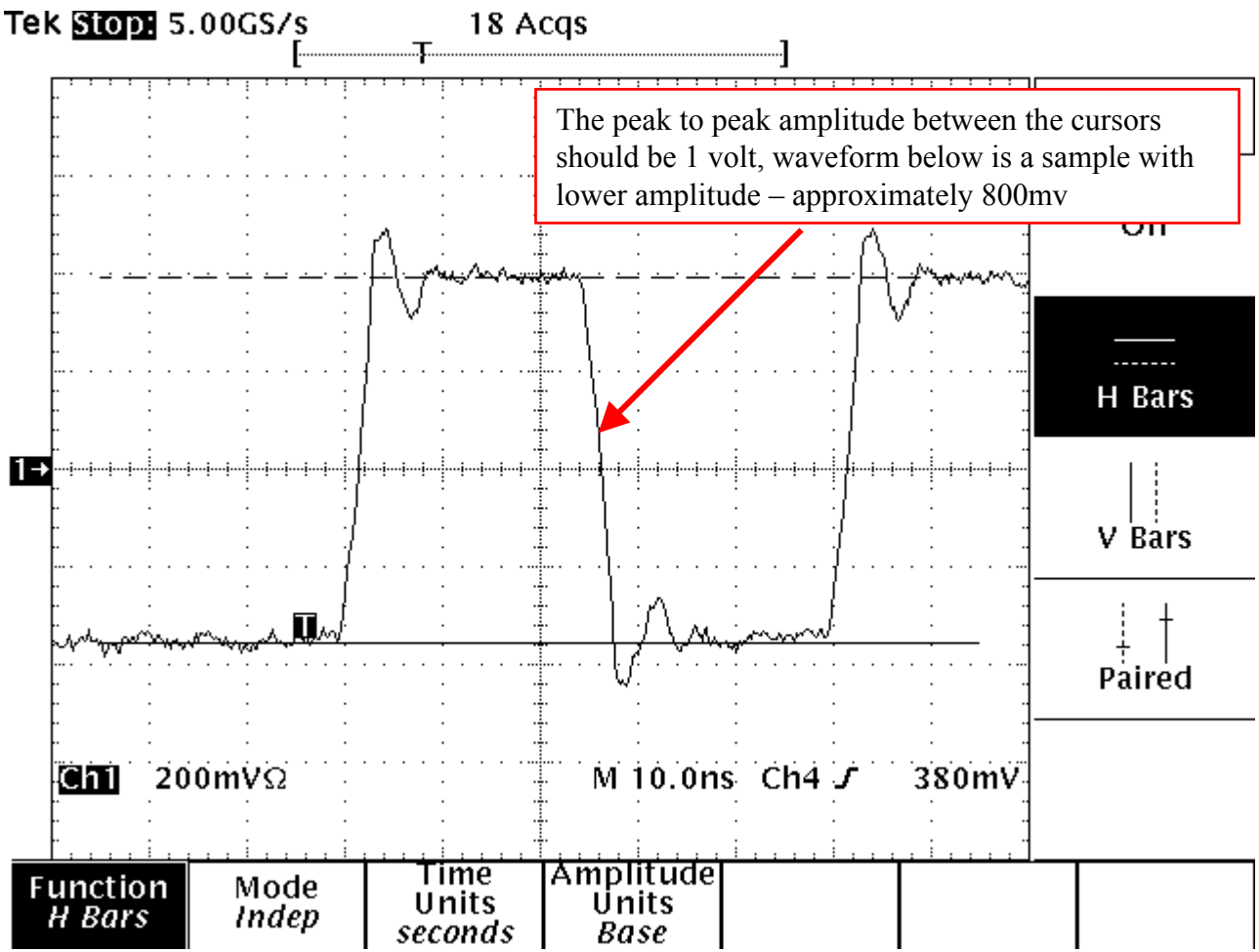
Use the floppy drive in the Tek scope to save eye diagrams.

Press the 'Run' button to start acquisitions.

After 30 sec., press the 'Run' button again to Stop acquisitions.

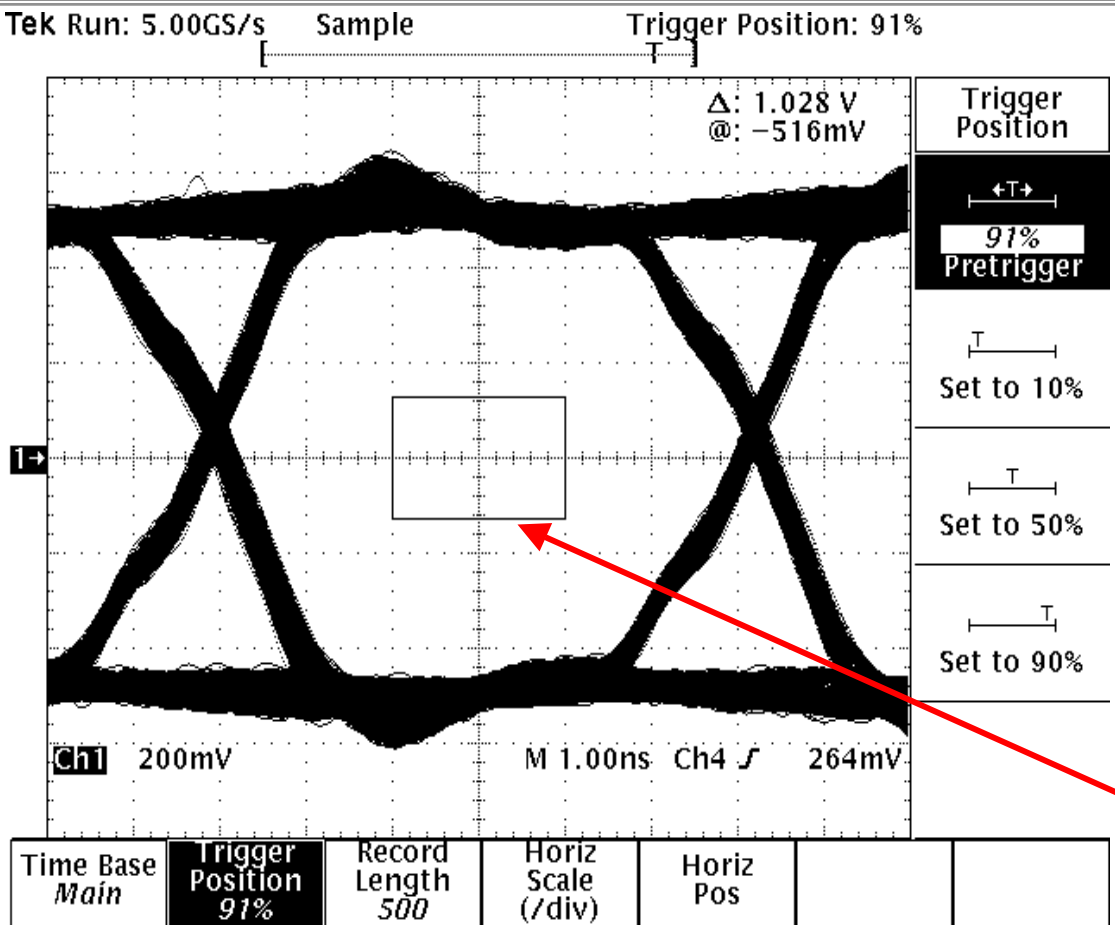
Save in PCX format by pressing the 'Waveform' button

Sample Scope Settings for Amplitude Measurement



Seagate
Information the way you want it™

Sample Scope Settings for Eye Pattern Measurement



Seagate
Information the way you want it™

Test Procedure

1) Attenuation - Use the method described on page 8 to make attenuation measurements. The input signal amplitude is measured at the launch test point (DB10 and DB13, Channel 1). The output amplitude is measured at the receive test point (DB10 and DB13, Channel 2).

The attenuation is calculated for every slot position: 1 - 5, and 6 -10.

Do a single ended measurement on the (+) & (-) outputs and "sum" them, the amplitude should be "0" ideally.

2) Eye Diagram - Use the method described on page 9 to capture "eye diagrams" at every slot position: 1 -5 and 6 -10.

All the above measurements were made with nominal slew rate and driver strength of 1 volt peak to peak, with precomp disabled, as per the switch settings on page 4.

Change the slew rate settings, by adjusting U8 switches 2, 3, and 4, to visually open the eye diagram, if possible, repeat measurements 1 & 2 for the new slew rate setting.

This is the basic set of recommended measurements. The user can change slew rate, drive strengths and precomp levels to make other measurements. Also this basic setup can be used to make cable measurements. Instead of using a backplane, use a long cable (round shielded or twist & flat) and a feed through terminator at the far end and a drive PCB load, and make cable attenuation and eye diagram measurements.

Users interested in impedance measurements, please refer to document created by Larry Barnes (LSIL).