To: T10 Technical Committee
From: Rob Elliott, Compaq Computer Corporation (Robert.Elliott@compaq.com)
Date: 9 April 2001
Subject: SPI-4 reset cleanup

Revision History
Revision 0 (28 March 2001) first revision
Revision 1 (9 April 2001) changed WAKEUP and RESET SERVICE DELIVERY SUBSYSTEM to map to bus reset condition rather than a TARGET RESET message.

Related Documents
spi4r03 – SCSI Parallel Interface-4 revision 3
sam2r16 – SCSI Architecture Model-2 revision 16

Overview
There has been some confusion about how to implement LOGICAL UNIT RESET task management function on parallel SCSI devices. For a device with a single logical unit target like a disk drive, it is not simply an alias for TARGET RESET. The PPR/WDTR/SDTR negotiation settings are not reset by a LOGICAL UNIT RESET but are reset by a TARGET RESET.

While researching this, I noticed a lot of text concerning "reset" is due a cleanup. The concepts of hard reset, reset event, and reset condition are not clearly defined.

The SAM-2 definitions are:
hard reset: A target action in response to a reset event in which the target port performs the operations described in 5.7.6.
reset event: A protocol specific event that triggers a hard reset from a SCSI device as described in 5.7.6.
logical unit reset: A logical unit action in response to a logical unit reset event in which the logical unit performs the operations described in 5.7.7.
logical unit reset event: An event that triggers a logical unit reset from a logical unit as described in 5.7.7.

The suggested changes for SPI-4 follow these conventions:
- **RST** = name for the bus reset signal (RST is to RESET as DB is to DATA)
- **hard reset** = target action in response to a reset event. Generates logical unit resets for all logical units as specified in SAM-2. Also clears out the negotiated settings and releases all signals (SPI specific requirements). A previous reference to "internal hard reset" is changed to just "hard reset."
- **reset event** = something that causes a hard reset. Protocol-specific reset events defined for SPI are:
    - **bus reset event** = detection of the RST signal changing from false to true
    - **transceiver mode change reset event** = detection of the DIFFSENS signal changing
    - **power on reset event** = detection of power on. By including this, we no longer have to say "hard reset or power cycle" everywhere – just "hard reset" covers both.
    - **target reset event** = receipt of a TARGET RESET message
- **bus reset condition** = the RST signal being true (stays around after the bus reset event)
- **target reset** = response to a TARGET RESET message
- **logical unit reset** = response to a LOGICAL UNIT RESET message
- **power on** = power being applied
- **power cycle** = power off and power on

Suggested Changes
All references to "reset" in SPI-4 are excerpted below.

3.1.x bus reset condition: State when the RST signal is true as described in 12.3.

3.1.x bus reset event: Detection of the RST signal changing from false to true as described in 12.5.2.

3.1.x hard reset: A target action in response to a reset event in which the target port performs the operations described in 12.4.

3.1.x logical unit reset: A logical unit action in response to a logical unit reset event in which the logical unit performs the operations described in SCSI Architecture Model-2.

3.1.x logical unit reset event: An event that triggers a logical unit reset from a logical unit as described in SCSI Architecture Model–2.

3.1.x power cycle: Power off followed by power on.

3.1.x power on reset event: Detection of power application as described in 12.5.3.

3.1.x power on: Power being applied.

3.1.x reset event: An event that triggers a hard reset from a SCSI device as described in 12.5. Reset events defined in this standard are bus reset event, power on reset event, target reset event, and transceiver mode change reset event.

3.1.x target reset event: Successfully receipt of a TARGET RESET message as described in 12.5.4 and 16.5.7.

3.1.x transceiver mode change reset event: Detection of a change in the DIFFSENS signal as described in 12.5.5.

6.1 SCSI bus interconnect overview
The interconnect shall meet the specified characteristics to ensure that compliant worst case transmitted signals result in received signals that meet the requirements in clause 7. Signals for this requirement include DB(0) through DB(15), P_CRCA, DB(P1), C/D, I/O, MSG, BSY, SEL, ATN, REQ, ACK, DIFFSENS, and R~~E~~S~~E~~T. At least minimum TERMPWR shall be delivered to the terminator from minimum sources per the requirements in subclause 7.5.

8.2 Signal descriptions
RST (RESET). An "OR-tied" signal that indicates the ~~RESET~~ bus reset condition.

9.1 SCSI parallel bus timing values (Tables 33-35)
NOTE Fast 160 SCSI devices shall not change timing parameters between training or reset events.

9.2.40 Reset delay
The minimum time that the RST signal shall be continuously true before the SCSI device shall initiate a hard reset (see 12.4).

9.2.41 Reset hold time
The minimum time that the RST signal is asserted. There is no maximum time.

9.2.42 Reset to selection
The recommended maximum time from after a reset event ~~reset condition~~ until a SCSI target is able to respond with appropriate status and sense data to the TEST UNIT READY, INQUIRY, and REQUEST SENSE commands (See SCSI Primary Commands-2 standard).

[Editor's note: should this be "bus reset condition" (RST only) or "reset event" (RST, transceiver change, TARGET RESET message, power on)?]

[Editor's note: the next two sections are merged and reorganized.]

10.3 ~~Unexpected~~ Expected and unexpected bus free phases

[Editor's note: move the first sentence down after the lists]

~~An unexpected bus free occurs when an initiator detects a BUS FREE phase that is not expected.~~

[Editor's note: reword this in terms of what a target does, not what an initiator expects. Don't use "shall" here – the descriptions of each event include the necessary shalls. This section just summarizes the events.]

~~Initiators shall expect a BUS FREE phase to occur after one of the following occurs:~~

Targets create a BUS FREE phase after one of the following:

a) after a ~~hard~~ bus reset event (see 12.5.2)~~is detected~~;

a2) after a transceiver mode change reset event (see 12.5.5);

b) after an ABORT TASK task management function is successfully received by a target;

c) after an ABORT TASK SET task management function is successfully received by a target;

d) after a CLEAR TASK SET task management function is successfully received by a target;

e) after a LOGICAL UNIT RESET task management function is successfully received by a target;

f) after a TARGET RESET task management function is successfully received by a target;

g) after a CLEAR ACA task management function is successfully received by a target;

h) after a DISCONNECT message is successfully transmitted from a target;

i) after a TASK COMPLETE message is successfully transmitted from a target;

j) after the release of the SEL signal after a SELECTION or RESELECTION phase time-out;

~~k) after a transceiver mode change:~~

l) after a PPR negotiation in response to a selection using attention condition when information unit transfers are enabled (see 16.3.12): or,

m) after any successful message negotiation that causes information unit transfers to be enabled (see 16.3.12) or disabled (see 16.3.12).

[Editor's note: The original "may expect" wording below is incorrect. That implies that initiators are allowed to expect bus frees at these times and treat it as an error if they don't see one. This list is identifying cases that the initiator shall not treat as errors.]

~~Initiators may expect a bus free to occur after one of the following:~~

Targets may create a BUS FREE phase after one of the following:

a) after the last SPI command information unit is successfully received by a target;

b) after a SPI data information unit is successfully received by or transmitted from a target;

c) after a SPI status information unit is successfully transmitted from a target;

d) after a SPI L_Q information unit if the SPI L_Q information unit DATA LENGTH field is zero; or

e) during a QAS phase.

An unexpected bus free occurs when an initiator detects a BUS FREE phase that is not expected. The target uses an unexpected bus free to inform the initiator of a protocol error. The target may switch to a BUS FREE phase at any time, except during an ARBITRATION phase, independent of any attention condition.

The target shall terminate the task that was the current task before the BUS FREE phase by clearing all data and status for that task. The target may optionally prepare sense data that may be retrieved by a REQUEST SENSE command. However, an unexpected bus free shall not create an exception condition.

The initiator shall terminate the task that was the current task before the BUS FREE phase occurred and shall manage this condition as an exception condition.

~~**10.4 Expected bus free phases**~~

~~Initiators may expect a bus free to occur after one of the following:~~

~~a) after the last SPI command information unit is successfully received by a target;~~
~~b) after a SPI data information unit is successfully received by or transmitted from a target;~~
~~c) after a SPI status information unit is successfully transmitted from a target;~~
~~d) after a SPI L_Q information unit if the SPI L_Q information unit DATA LENGTH field is zero; or~~
~~e) during a QAS phase.~~

10.12.4 MESSAGE OUT phase

…

If the target receives all of the message byte(s) successfully (i.e. no parity errors), it shall indicate that it will not retry by changing to any information transfer phase other than the MESSAGE OUT phase and transferring at least one byte. The target may also indicate that it has successfully received the message byte(s) by changing to the BUS FREE phase (e.g. after receiving ABORT TASK SET, LOGICAL UNIT RESET or TARGET RESET messages).

10.13 Signal restrictions between phases

…

h) The ATN and RST signals may change as defined under the descriptions for the attention condition (see 12.2) and ~~hard~~ bus reset condition (see 12.3).

12 SCSI bus conditions

12.1 SCSI bus conditions overview

The SCSI bus has asynchronous conditions that cause the SCSI device to perform certain actions that may alter the phase sequence.

Furthermore, SCSI devices may not all be powered on at the same time. This standard does not address power sequencing issues. However, each SCSI device, as it is powered on, should perform appropriate internal reset operations and internal test operations. Following a power on to selection time after powering on, SCSI targets should be able to respond with appropriate status and sense data to the TEST UNIT READY, INQUIRY, and REQUEST SENSE commands.

12.2 Attention condition

…

[Editor's note: sort the list]

During a RESELECTION phase the initiator should only create an attention condition to transmit an ABORT TASK ~~SET~~, ABORT TASK SET, ~~TARGET RESET,~~ CLEAR TASK SET, DISCONNECT, LOGICAL UNIT RESET, ~~or~~ NO OPERATION, or TARGET RESET message. Other uses may result in ambiguities concerning the nexus.

12.3 Bus reset condition

The bus reset condition is used to create a hard reset (see 12.4) for all SCSI devices on the bus and change the bus to a BUS FREE phase. This condition shall take precedence over all other phases and conditions. Any SCSI device may create the bus reset condition by asserting the RST signal for a minimum of a reset hold time.

Environmental conditions (e.g. static discharge) may generate brief glitches on the RST signal. SCSI devices shall not react to glitches on the RST signal that are less than a reset delay. The manner of rejecting glitches is vendor-specific. The bus clear delay following a RST signal transition to true is measured from the original transition of the RST signal. This limits the time to confirm the RST signal to a maximum of a bus clear delay.

12.~~3~~ 4 Hard reset

~~The hard reset is used to clear all SCSI devices from the bus. This condition shall take precedence over all other phases and conditions. Any SCSI device may create the reset condition by asserting the RST signal for a minimum of a reset hold time.~~

~~All SCSI devices~~A SCSI device detecting a reset event shall release all SCSI bus signals (except the RST signal, if it is asserting RST) within a bus clear delay of the transition of the RST signal to

true. The BUS FREE phase always follows the bus reset condition. The SCSI device shall not assert the RST signal in response to a reset event.

The effect of the hard reset on tasks that have not completed, SCSI device reservations, and SCSI device operating modes is defined in the SCSI Architecture Model-2 standard. Any SCSI device that detects a hard reset shall also:
a) set the data transfer width to eight-bit transfer mode,
b) set the data transfer mode to asynchronous transfer mode, and
c) set to zero all the PPR protocol options bits (see 16.3.12).

~~Environmental conditions (e.g. static discharge) may generate brief glitches on the RST signal. SCSI devices shall not react to glitches on the RST signal that are less than a reset delay. The manner of rejecting glitches is vendor-specific. The bus clear delay following a RST signal transition to true is measured from the original transition of the RST signal, not from the time that the signal has been confirmed. This limits the time to confirm the RST signal to a maximum of a bus clear delay.~~

12.~~4~~ 5 Reset events

12.~~4~~5.1 Reset events overview

When a SCSI device detects a reset event it shall ~~only~~ initiate a~~n internal~~ hard reset (see 12.4) ~~(i.e., the SCSI device shall not assert the RST signal)~~.

12.5.2 Bus reset event

When a SCSI device detects a bus reset condition by detecting RST true for a reset delay, it shall cause a reset event. In response to a bus reset event, a target shall create a unit attention condition for all initiators. The sense key shall be set to UNIT ATTENTION and the additional sense code shall be set to either SCSI BUS RESET OCCURRED or POWER ON, RESET, OR BUS DEVICE RESET OCCURRED.

12.5.3 Power on reset event

When a SCSI device is powered on, it shall cause a reset event. In response to a power on reset event, the target shall create a unit attention condition for all initiators. The sense key shall be set to UNIT ATTENTION and the additional sense code set to either POWER ON OCCURRED or POWER ON, RESET, OR BUS DEVICE RESET OCCURRED.

12.5.4 Target reset event

When a SCSI device successfully receives a TARGET RESET message, it shall cause a reset event. In response to a target reset event, the target shall create a unit attention condition for all initiators. The sense key shall be set to UNIT ATTENTION and the additional sense code set to either BUS DEVICE RESET FUNCTION OCCURRED or POWER ON, RESET, OR BUS DEVICE RESET OCCURRED.

12.~~4~~5.~~2~~ 5 Transceiver mode change reset event

[Editor's note: SPC-2 spells out SINGLE-ENDED]

When a SCSI device that contains multimode transceivers detects a transceiver mode change from LVD mode to MSE mode it shall cause a reset event. In response to the transceiver mode change reset event, a target shall create a unit attention condition for all initiators. The sense key shall be set to UNIT ATTENTION~~,~~ and the additional sense code shall be set to TRANSCEIVER MODE CHANGED TO ~~SE~~SINGLE-ENDED.

When a SCSI device that contains multimode transceivers detects a transceiver mode change from MSE mode to LVD mode it shall cause a reset event. In response to the transceiver mode change reset event, a target shall create a unit attention condition for all initiators. The sense key shall be set to UNIT ATTENTION~~,~~ and the additional sense code shall be set to TRANSCEIVER MODE CHANGED TO LVD.

[Editor's note: check elsewhere for "The sense key shall be set to …, and the additional sense code set to"]

~~Any SCSI device that detects a transceiver mode change shall:~~
~~a) set the data transfer width to eight-bit transfer mode~~
~~b) set the data transfer mode to asynchronous transfer mode, and~~
~~c) set to zero all the PPR protocol options bits (see 16.3.12).~~
~~In addition any target that detects a transceiver mode change shall switch to a BUS FREE phase."~~

13.1 SCSI bus phase sequences overview
The order in which phases are used on the SCSI bus follows a prescribed sequence.

During DT DATA phases the target shall not change phases except at data group boundaries or SPI information unit boundaries. If an initiator detects a change to the C/D, I/O, or MSG signals within a data group or information unit it shall consider any data transferred for that data group or information unit to have been transferred incorrectly. The initiator shall consider this condition a protocol error and respond accordingly.

A hard reset (see 12.4) aborts any phase and is always followed by the BUS FREE phase. Also, any phase may be followed by the BUS FREE phase, but many such instances are exception conditions for initiators (see 10.3).

14.3.1, Table 42 - TASK MANAGEMENT FLAGS
08h The task manager shall perform a ~~hard reset to~~logical unit reset of the selected logical unit as defined in the LOGICAL UNIT RESET message (see 16.5.6).
20h The task manager shall perform a ~~hard~~ target reset as defined in the TARGET RESET message (see 16.5.7).

16.3.12.1 PARALLEL PROTOCOL REQUEST message description
…
A PARALLEL PROTOCOL REQUEST message exchange shall be initiated by an initiator whenever a previously arranged parallel protocol agreement may have become invalid. The agreement becomes invalid after any ~~condition~~ event that may leave the parallel protocol agreement in an indeterminate state such as a reset event (see 12.5).~~:~~
~~a) after a hard reset;~~
~~b) after a TARGET RESET message;~~
~~c) after a power cycle;~~
~~d) after a change in the transceiver mode (e.g., LVD mode to SE mode).~~

A logical unit reset has no effect on the parallel protocol agreement.

16.3.16.1 SYNCHRONOUS DATA TRANSFER REQUEST message description
…
An SDTR message exchange shall be initiated by a target whenever a previously arranged synchronous transfer agreement may have become invalid. An SDTR message exchange shall be initiated by an initiator if that initiator does not support the PPR message or the initiator has determined the target does not support the PPR message whenever a previously arranged synchronous transfer agreement may have become invalid. The agreement becomes invalid after any ~~condition~~ event that may leave the data transfer agreement in an indeterminate state such as a reset event (see 12.5).~~:~~
~~a) after a hard reset;~~
~~b) after a TARGET RESET message;~~
~~c) after a power cycle; and~~
~~d) after a change in the transceiver mode (e.g., LVD mode to MSE mode).~~

A logical unit reset has no effect on the data transfer agreement.

16.3.18.1 WIDE DATA TRANSFER REQUEST message description

…

A WDTR message exchange shall be initiated by a SCSI device whenever a previously arranged wide transfer agreement may have become invalid. The agreement becomes invalid after any ~~condition~~ event that may leave the wide transfer agreement in an indeterminate state such as a reset event (see 12.5).~~:~~

~~a) after a hard reset;~~

~~b) after a TARGET RESET message;~~

~~c) after a power cycle; and~~

~~d) after a change in the transceiver mode (e.g., LVD mode to MSE mode).~~

A logical unit reset has no effect on the wide transfer agreement.

16.5.1, Table 74 - Task attribute message codes

[Editor's note: Mark LOGICAL UNIT RESET as mandatory and remove the footnote about hierarchical addressing (to match the latest SAM-2). I think we changed the IU enabled entries to Os in the March Parallel SCSI WG meeting.]

17h, O, ~~O~~M, ~~n/a~~O, ~~n/a~~M, LOGICAL UNIT RESET ~~(Note)~~, Out, Yes

~~Note-The LOGICAL UNIT RESET message is mandatory if hierarchical addressing (see SCSI Architecture Model-2 standard) is implemented by the target.~~

16.5.6 LOGICAL UNIT RESET

The LOGICAL UNIT RESET message is defined in the SCSI Architecture Model-2 standard.

If only an I_T nexus has been established the LOGICAL UNIT RESET message shall be ~~performed~~ interpreted as if it were a TARGET RESET message. If an I_T_L nexus has been established, successful receipt of a LOGICAL UNIT RESET message is a logical unit reset event (see SCSI Architecture Model-2).

In addition to the requirements in the SCSI Architecture Model-2 standard, the target shall go to the BUS FREE phase following the successful receipt of the LOGICAL UNIT RESET message.

NOTE: A logical unit reset has no effect on the parallel protocol agreement, wide transfer agreement, or data transfer agrement.

[Editor's note: The second paragraph is a bit confusing. The only case this can happen is when information units are enabled; when information units are disabled, the target is required to reject a LOGICAL UNIT RESET if it arrives as the first message per this section:

> **16.2.1 Message protocol rules**
>
> If information unit transfers are disabled, the first message sent by the initiator after a successful SELECTION phase with an attention condition shall be an IDENTIFY, ABORT TASK SET (see 16.5.3), or TARGET RESET message. If a target receives any other message it shall cause an unexpected bus free by generating a BUS FREE phase (see 10.3).

]

16.5.7 TARGET RESET

The TARGET RESET message is defined in the SCSI Architecture Model-2 standard. Successful receipt of a TARGET RESET message is a target reset event (see 12.5.4).

In addition to the requirements in the SCSI Architecture Model-2 standard, the target shall go to the BUS FREE phase~~,~~ following the successful receipt of the TARGET RESET message ~~shall go to the BUS FREE phase~~.

17.3 Incorrect initiator connection

[Editor's note: sort the list]

An incorrect initiator connection occurs during an initial connection if an initiator creates a nexus that already exists and does not send an ABORT TASK SET, ABORT TASK, CLEAR TASK SET, DISCONNECT, LOGICAL UNIT RESET, or TARGET RESET~~, CLEAR TASK SET, DISCONNECT, or LOGICAL UNIT RESET~~ message as one of the messages of the MESSAGE OUT phase or as one of the task management flags in the SPI command information unit.

18.1.4 Port control mode page

The port control mode page (see table 79 and table 80) contains those parameters that ~~select~~ affect SPI SCSI device port operation options. The page shall be implemented by LUN 0 of all SPI SCSI devices. The page shall not be implemented by logical units other than LUN 0. The implementation of any bit and its associated functions is optional. The page follows the MODE SENSE / MODE SELECT rules specified by SCSI Primary Commands-2 standard.

The target shall maintain an independent set of port control mode page parameters for each initiator. The parameters saveable bit in the mode page format header returned with MODE SENSE command shall be set to zero if the long mode page format is being used (i.e., LONG bit set to one), indicating the parameters are not saved through resets.

After a MODE SELECT command, parameter settings shall remain in effect until either:
a) settings are changed by another MODE SELECT command,
b) a ~~reset condition~~logical unit reset of LUN 0 occurs,
c) an SDTR negotiation successfully completes,
d) a WDTR negotiation successfully completes, or
e) a PPR negotiation successfully completes with the MAINTAIN MARGIN CONTROL SETTINGS bit set to zero.

19.5.2 Task management function service

This standard handles task management functions as a four step confirmed service that provides the means to transfer task management functions to a task manager.

The task management functions are defined in the SCSI Architecture Model-2 standard. This standard defines the actions taken by the SCSI parallel interface service to carry out the requested task management functions.

[Editor's note: I suggest replacing the last sentence with "The task management functions for SPI are defined in 14.3.1 and 19.5." and deleting all the subsequent sections. FCP-2 removed sections like these after its revision 4a, replacing them with pointers to its IU definitions. WAKEUP and RESET SERVICE DELIVERY SUBSYSTEM are only used by SBC and SBC-2 and a separate proposal may propose removing them.]
]

19.5.3 ABORT TASK

The SCSI parallel interface services request the initiator issue an ABORT TASK message (see 16.5.2) to the selected SCSI device.

19.5.4 ABORT TASK SET

The SCSI parallel interface services request the initiator issue an ABORT TASK SET message (see 16.5.3) to the selected SCSI device.

19.5.5 CLEAR ACA

The SCSI parallel interface services request the initiator issue a CLEAR ACA message (see 16.5.4) to the selected SCSI device.

19.5.6 CLEAR TASK SET

The SCSI parallel interface services request the initiator issue a CLEAR TASK SET message (see 16.5.5) to the selected SCSI device.

19.5.7 LOGICAL UNIT RESET

The SCSI parallel interface services request the initiator issue a LOGICAL UNIT RESET message (see 16.5.6) to the selected SCSI device.

19.5.8 RESET SERVICE DELIVERY SUBSYSTEM

The SCSI parallel interface services request the initiator ~~create a issue a hard reset (see 12.3)~~bus reset condition (see 12.3) ~~to~~ on the SCSI bus containing the selected SCSI device.

19.5.9 TARGET RESET

The SCSI parallel interface services request the initiator issue a TARGET RESET message (see 16.5.7) to the selected SCSI device.

19.5.10 WAKEUP

The SCSI parallel interface services request the initiator ~~issue a~~ create a ~~hard reset (see 12.3)~~bus reset condition (see 12.3) ~~to~~ on the SCSI bus containing the selected SCSI device.

B.1 (SCSI bus fairness) Model, fourth paragraph:

SCSI IDs shall also be cleared if a SCSI device discontinues arbitration (e.g., as a result of an ABORT TASK message, ABORT TASK SET message, CLEAR TASK SET message, or logical unit reset~~TARGET RESET message, hard reset~~).

B.3.1 Fairness states overview

A SCSI device shall be in one of three fairness states. A SCSI device shall be in fairness wait state if it is waiting for a clear fairness register to participate in arbitration. A SCSI device shall be in the fairness participate state if it is participating in arbitration. A SCSI device shall be in the fairness idle state for all other conditions. A SCSI device shall enter the fairness idle state after any reset event. A SCSI device shall implement a lockout delay to prevent devices that stop arbitrating from causing deadlock.

F.4 Simple bus expanders:

…

g) Simple expanders ~~that are powered on~~ shall retransmit RE~~E~~SE~~E~~T assertions from one bus segment to the other regardless of the state of any other SCSI signals on either side;

…

k) Transceiver mode changes (e.g., SE to LVD) on one bus segment shall cause the simple expander to ~~issue a hard reset~~create a bus reset condition (see 12.3) on the ~~an~~other bus segment.

F.8.3 Rule 2

…

The intermediate bus segment in this example receives signals at the higher transfer rate on the DATA BUS, DB(P_CRCA), and/or DB(P1) signals, but since the devices in the intermediate bus segment are not participating in the higher transfer rate and are waiting for the next BUS FREE phase~~, hard reset,~~ or some other phase they are unaffected by the higher transfer rates.

For multimode bus segments, any dynamic transceiver mode change (e.g., LVD to SE) is treated as a fault and the simple expander shall create a ~~hard reset~~bus reset condition (see 12.3) on the segment opposite the one that experienced the transceiver type change. The simple expander shall detect this change by sensing the DIFFSENS line. This scheme ensures that the initiators on the other bus segments are aware of the transceiver mode change and may reassess whether this new transceiver type is consistent with the performance requirements for the bus segments and the overall parameters for the SCSI domain before allowing information transfers to resume. Once a ~~hard~~ bus reset event is detected, initiators shall renegotiate with all targets in the SCSI domain.

G.4 Enabling ECP

Following a ~~power cycle or bus~~ hard reset (see 12.4), a communicative expander shall function as a simple expander for each initiator until the initiator enables ECP as follows:

G.6.1.2 ASSIGN ADDRESS

An ASSIGN bit of 1 indicates that the expander shall respond to the expander address specified in the EXPANDER ADDRESS field for single functions from this initiator. The address assignment shall remain in effect until changed by another ASSIGN ADDRESS function from this initiator or ~~until the next reset condition~~by a hard reset ~~(see 12.4)or power cycle~~. An ASSIGN bit of 0 indicates that the expander shall not change its expander address assignment for this initiator.

G.6.1.3 MARGIN CONTROL

The MARGIN CONTROL expander function sets parameter settings in the initiator or expander for usage between the I_T nexus on subsequent synchronous transfers and paced transfers. These parameter settings shall remain in effect until changed by another MARGIN CONTROL expander function or by a ~~reset condition~~hard reset (see 12.4).

G.6.2.2 CONTROL (Table G.8 – FAR_CTL field values)

100b, Reset far port, Shall cause the expander to create a ~~hard~~ bus reset condition (see 12.3) on the specified far port upon the next BUS FREE phase on the near port (i.e., the expander creates a pulse on the RST signal). The expander shall not propagate this ~~hard~~ bus reset condition to any other of its ports.

O.3.1 Protection code usage overview

Protection code checking is enabled or disabled on an I_T nexus basis. All COMMAND, MESSAGE, and STATUS phase information is checked for an I_T nexus while checking is enabled. Protection code checking is disabled after a ~~power cycle, after a~~ hard reset (see 12.4)~~, after a TARGET RESET message, and after a change in the transceiver mode (e.g., LVD mode to MSE mode)~~. Protection code checking is always disabled for information unit transfers.

O.3.3 Enabling protection code checking

A SCSI device enables protection code checking for an I_T nexus when it detects that valid protection code data is being transmitted on the upper byte of the SCSI bus. The frequency that a SCSI device will try to enable protection code checking and the number of valid protection code bytes required is vendor specific. The following are some potential times when a SCSI device may try to enable protection code checking:

a) During the first COMMAND, MESSAGE, or STATUS phase after a ~~power cycle, after a~~ hard reset (see 12.4)~~, after a TARGET RESET message, or after a change in the transceiver mode~~.