Determining First Pulse Attenuation

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Managing Output Driver Power

- PCI-X is looking at increase speed or a possible increased bus loading, but mostly increased speed.
- PCI-X power dissipation can double, because of the above
- Need to insure that we haven't 'over' worst cased the SCSI driver.

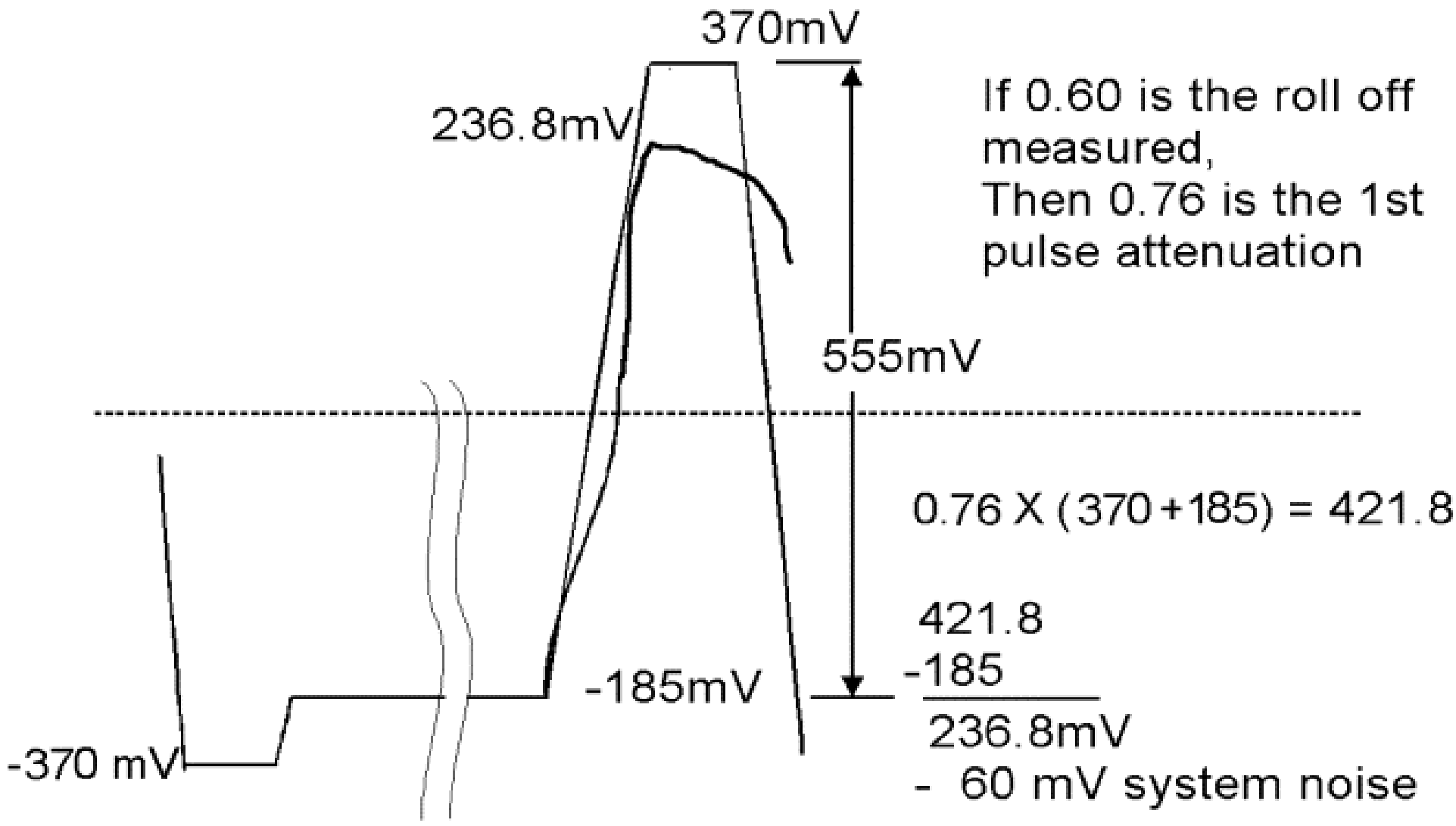
Creating a 1st pulse model

- Determine cable attenuation vs. frequency
- Create Hspice W element cable model that matches frequency roll off characteristics.
- Find cable length for 12db loss @ 200MHz
- Sweep cable length, and display result such that 12db loss @ 200MHz is 100% point of the X-axis

185mV holding level assumptions

- Eye mask has always allowed for dips to 30mV.
- 60mV X-talk is not likely because, if it is on a quite output from the driving side, then 22mV is the X-talk.
- If you consider X-talk on the clock that is flowing in the direction against the data, there is always at least 1 quiet signal right next to it on one side, and many quiet signals on the other side.
- Anyway, if you add 30mV + 60mV, plus allow 95mV for more than 25% reflections, = 185mV.
- 185mV holding is after any driver or system offset.

Good Model

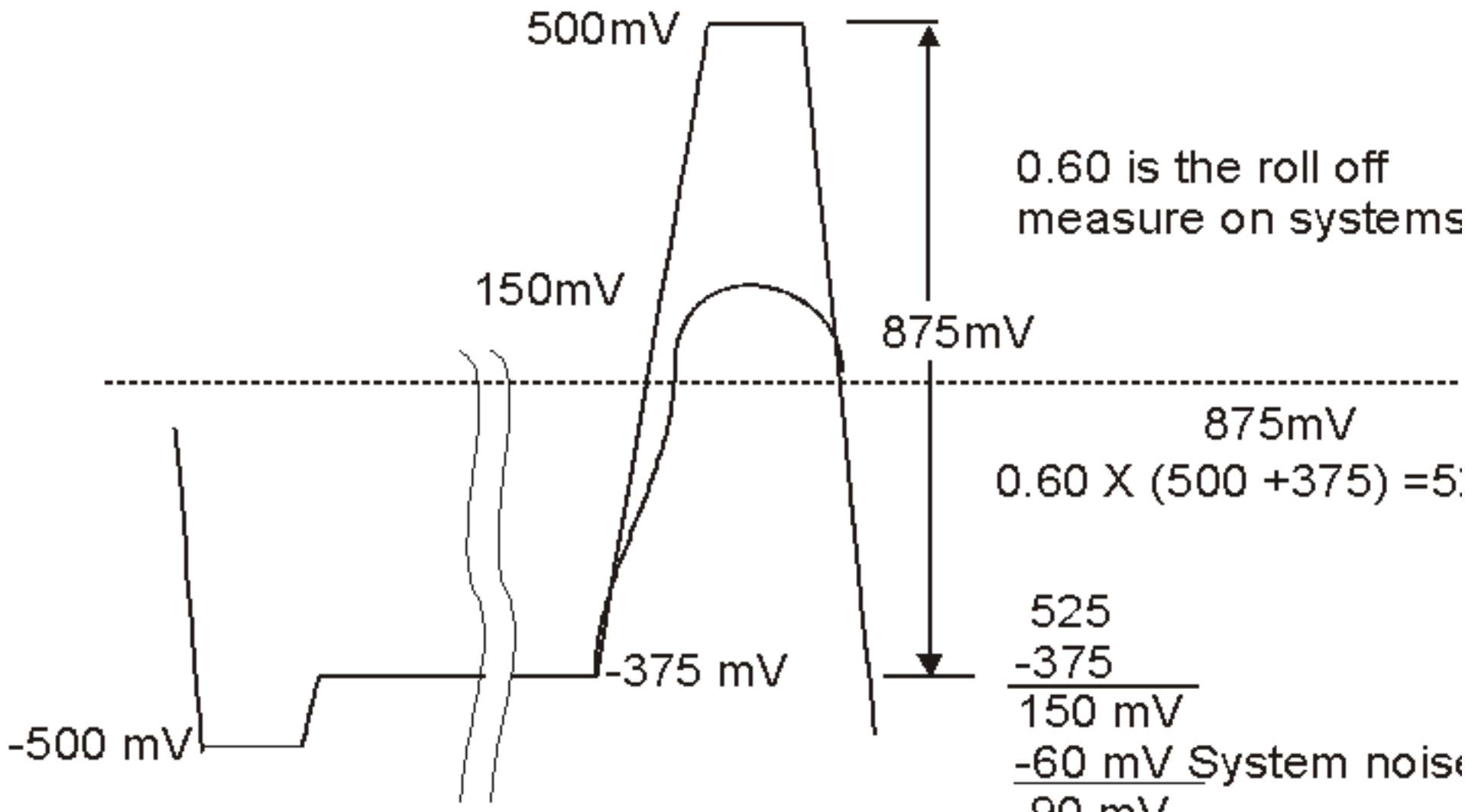


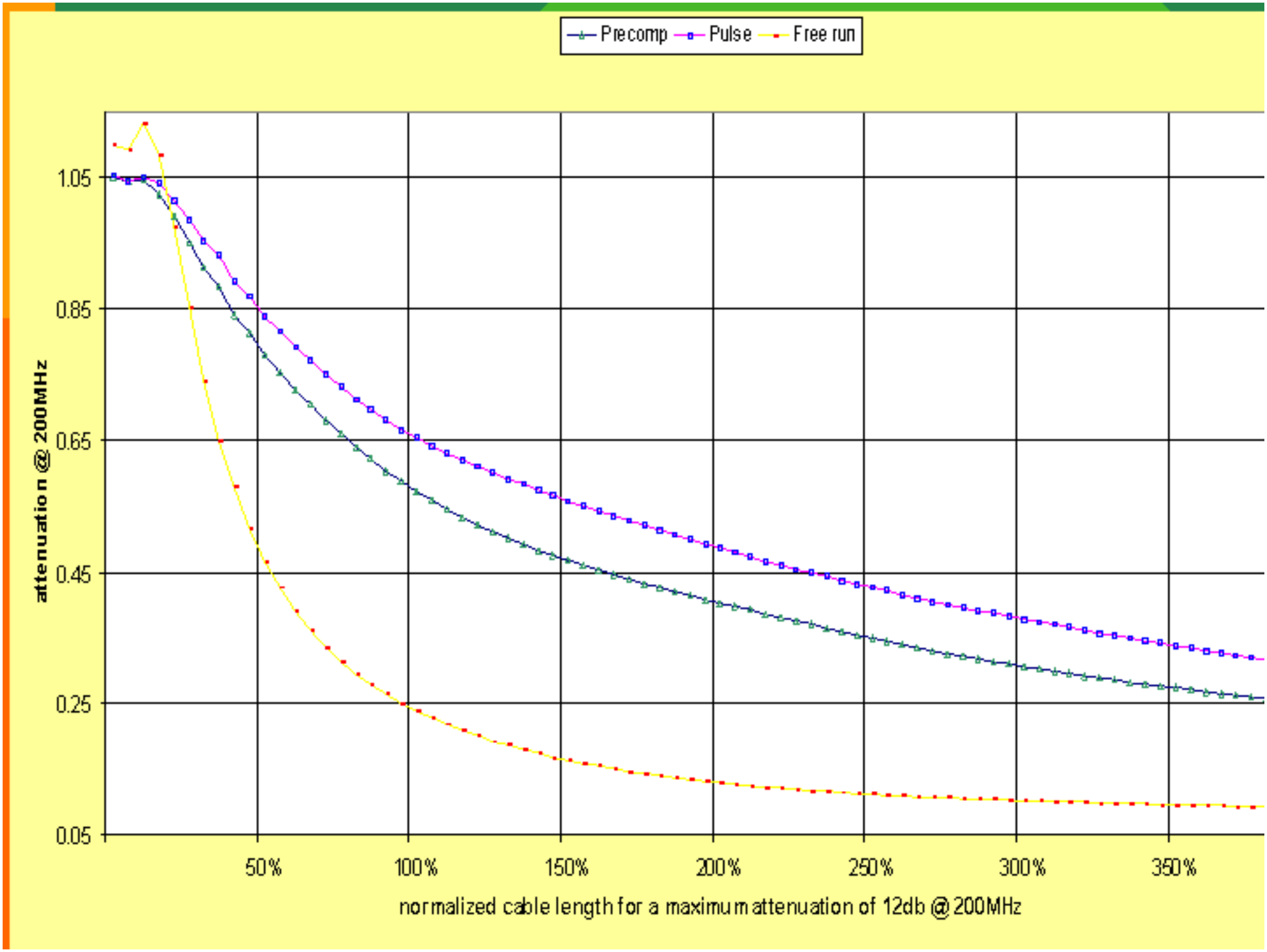
If 0.60 is the roll off measured,
Then 0.76 is the 1st pulse attenuation

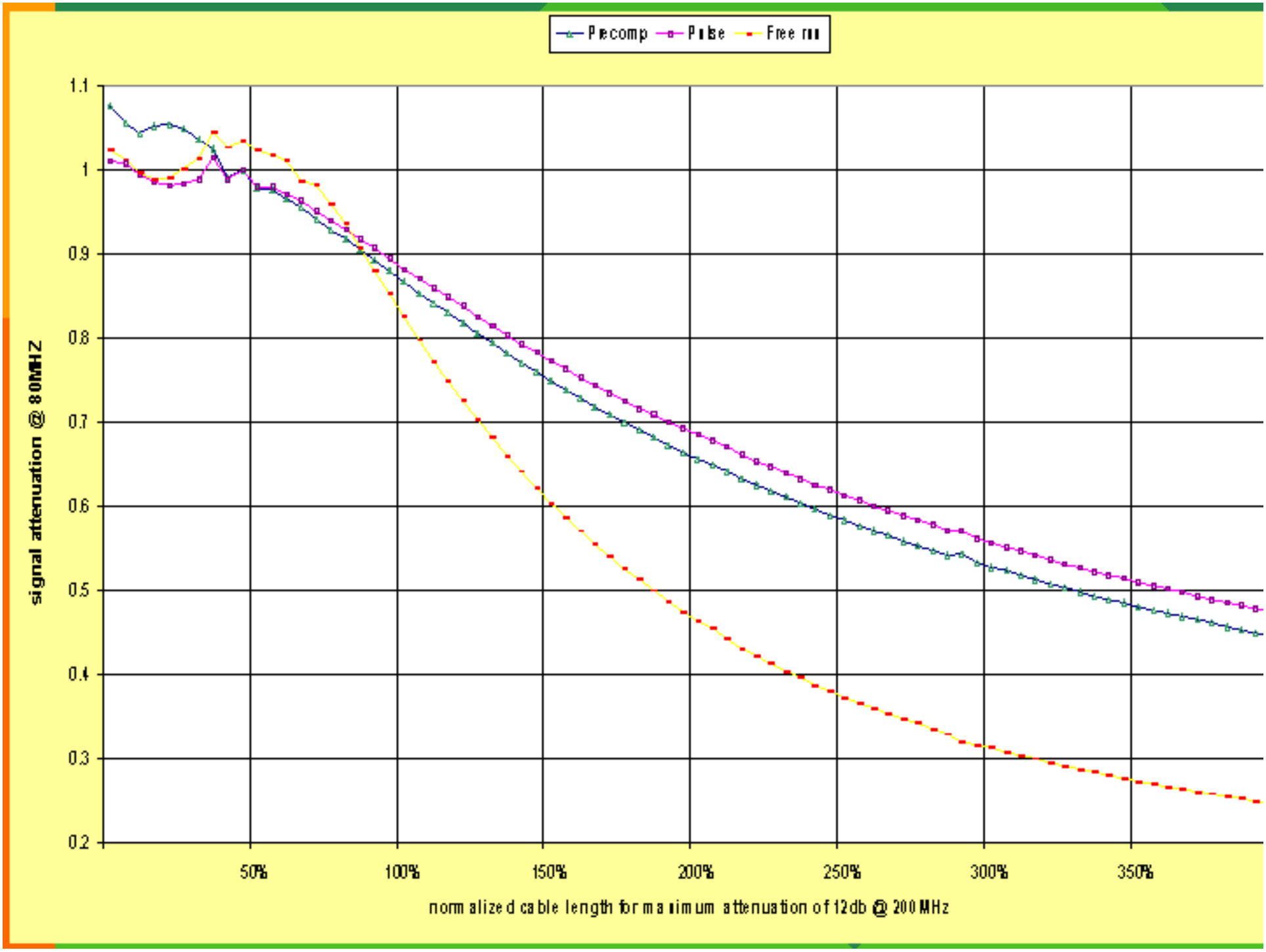
0.76 X (370 + 185) = 421.8

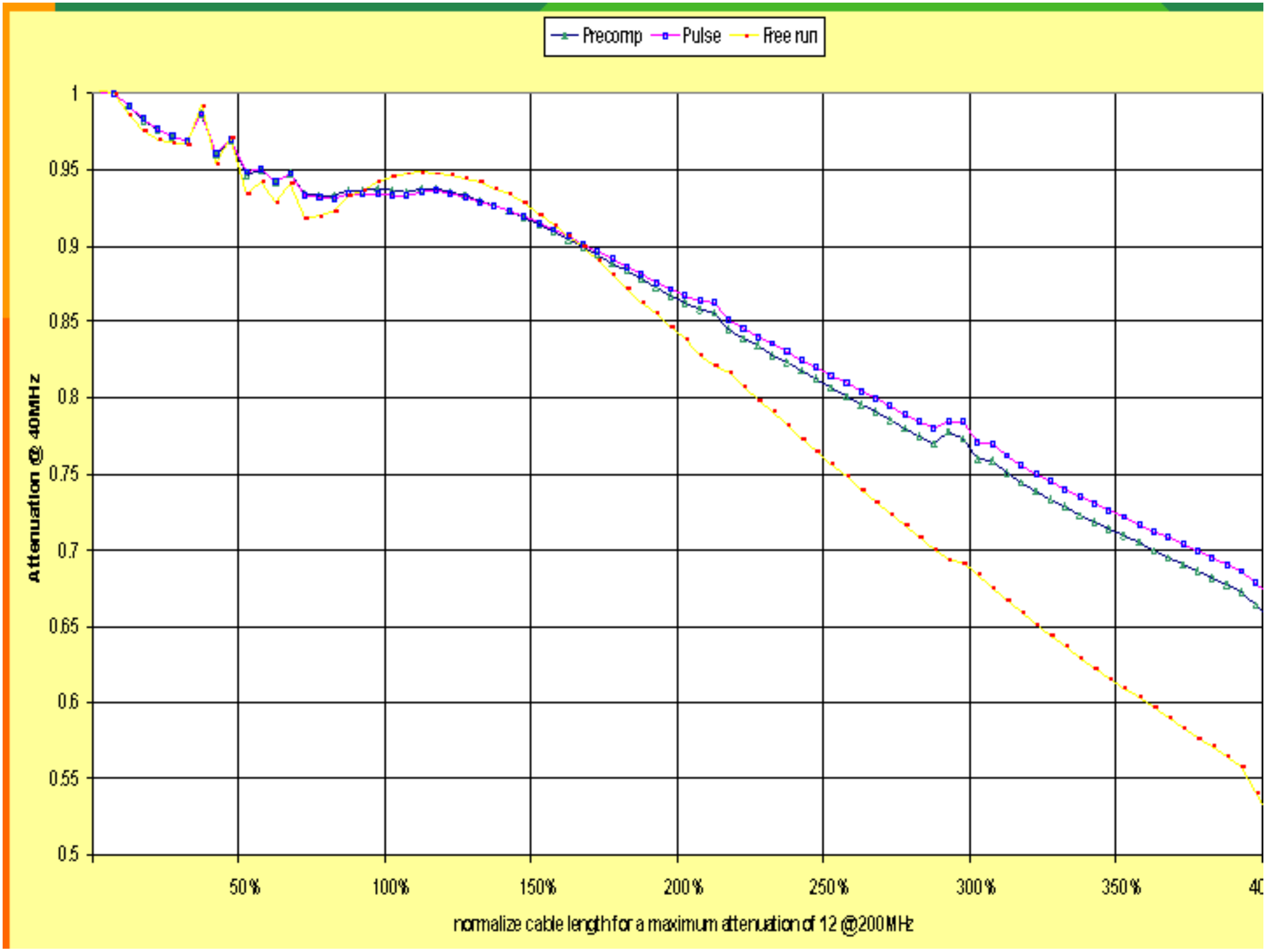
421.8
-185
236.8mV
- 60 mV system noise
176.8mV

Old model


500mV
150mV
875mV
-375 mV
-500 mV
0.60 is the roll off
measure on systems
875mV
0.60 X (500 +375) =5
525
-375
150 mV
-60 mV System noise
90 mV


Precomp
Pulse
Free run
1.05
0.85
0.65
0.45
0.25
0.05
attenuation @ 200MHz
50%
100%
150%
200%
250%
300%
350%
normalized cable length for a maximum attenuation of 12db @ 200MHz

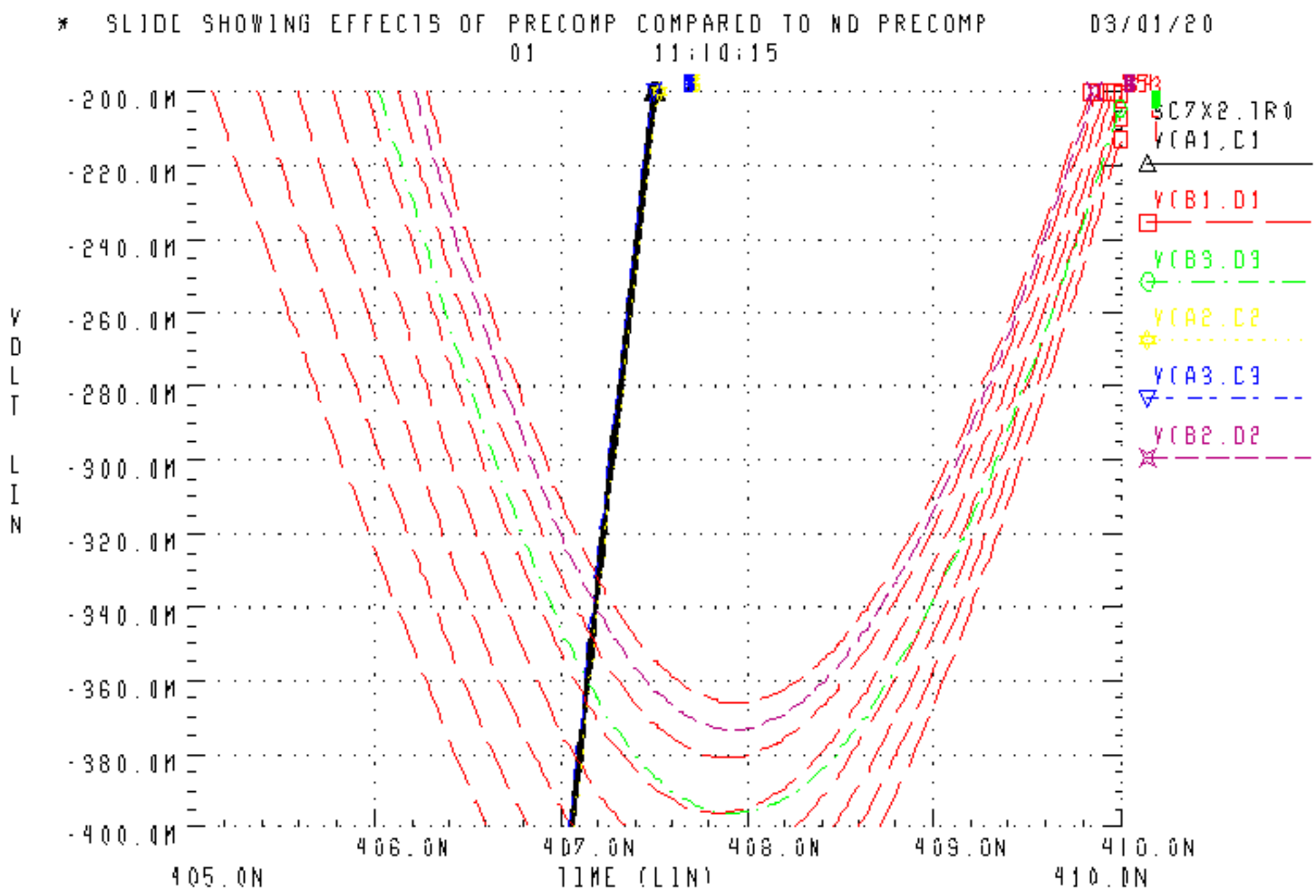

Precomp
Pulse
Free run
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
signal attenuation @ 80MHZ
50%
100%
150%
200%
250%
300%
350%
normalized cable length for maximum attenuation of 12db @ 200 MHz


Precomp
Pulse
Free run
1
0.95
0.9
0.85
0.8
0.75
0.7
0.65
0.6
0.55
0.5
Attenuation @ 40MHz
50%
100%
150%
200%
250%
300%
350%
normalize cable length for a maximum attenuation of 12 @200MHz

Corrected Spread Sheet

Voltage level in table represents ~3ns signal width

Cable roll off to 60% signal -60 mV crosstalk & Noise				23% DC loss from cable, connectors and terminators					
Trans FB 22% roll off to 60%	103.19072	149.5016	158.3227	160.528	186.9914	213.4547	248.7392	266.3814	292.8448
Trans FB 33% roll off to 60%	111.39584	160.0352	169.2998	171.616	199.4099	227.2038	264.2624	282.7917	310.5856
Trans FB 40% roll off to 60%	115.4984	165.302	174.7884	177.16	205.6192	234.0784	272.024	290.9968	319.456
Trans FB 50% roll off to 60%	122.336	174.08	183.936	186.4	215.968	245.536	284.96	304.672	334.24
Right equation	((((V+VFB)*.76)-Vfb)*0.77)-60)								
	100 mV receiver required, 60 mV Crosstalk and System Noise								


* SLIDE SHOWING EFFECTS OF PRECOMP COMPARED TO NO PRECOMP 03/01/20
01 11:10:15
-200.0M
-220.0M
-240.0M
-260.0M
-280.0M
-300.0M
-320.0M
-340.0M
-360.0M
-380.0M
-400.0M
VOLT LIN
405.0N
406.0N
407.0N
408.0N
409.0N
410.0N
410.0N
TIME (LIN)
SC7X2.1R0
V(A1,C1
V(B1,D1
V(B3,D3
V(A2,C2
V(A3,C3
V(B2,D2

In Closing

- Free running attenuation is much greater than 1st pulse attenuation
- There was no need for such a high holding level after pre-comp cutback.
- Let each company decide it's own driver output offset budget.

termination bias.

Table A.2 - Driver steady-state test limits and conditions for ~~synchronous~~ non-paced transfers

Test parameter	Test conditions (figure A.1)(note 1)	Minimum (mV) (note 2)	Maximum (mV)
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted) (note)	V_1 = 1,056 V V_2 = 0,634 V	320	800
	V_1 = 1,866 V V_2 = 1,444V	320	800
$\lvert V_N \rvert$ Differential output voltage magnitude (negated) (note)	V_1 = 1,056 V V_2 = 0,634 V	320	800
	V_1 = 1,866 V V_2 = 1,444V	320	800
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted)	All four above conditions	0,69 x $\lvert V_N \rvert$ + 50	1,45 x $\lvert V_N \rvert$ - 65

Notes:
1 The test circuit (figure A.1) is approximately equivalent to two terminators creating the normal system bias.
2 Minimum standard drive level. If there is a pre-comp cutback, then the minimum drive level after cutback must be greater than 185mV after all system & driver offsets are taken into account.
3 The test limits shall be within the shaded area of figure A.2.

Table A.3 - Driver steady-state test limits and conditions for paced transfers

Test parameter	Test conditions (figure A.1)(note 1)	Minimum (mV) (note 2)	Maximum (mV)
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted) (note)	V_1 = 1,056 V V_2 = 0,634 V	370	800
	V_1 = 1,866 V V_2 = 1,444V	370	800
$\lvert V_N \rvert$ Differential output voltage magnitude (negated) (note)	V_1 = 1,056 V V_2 = 0,634 V	370	800
	V_1 = 1,866 V V_2 = 1,444V	370	800
$\lvert V_A \rvert$ Differential output voltage magnitude (asserted)	All four above conditions	0,90 x $\lvert V_N \rvert$ - 23	1,11 x $\lvert V_N \rvert$ + 26

Notes:
1 The test circuit (figure A.1) is approximately equivalent to two terminators creating the normal system bias.
2 Minimum standard drive level. If there is a pre-comp cutback, then the minimum drive level after cutback must be greater than 185mV after all system & driver offsets are taken into account.
3 The test limits shall be within the shaded area of figure A.3.