

T10/01-045 r0

LSI LOGIC®

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Jan 16, 2001

To: T10 Technical Committee
From: William Petty, LSI Logic Corp.
Subj: **Actual Pre-Compensation Eye Diagrams**

The following data is taken from actual silicon drivers and measured at the worst point on the following segment configurations. It shows the effect that various levels of pre-compensation have on the received waveforms.

Equipment Setup:

HP 81110A Pattern Generator

PRBP (Pseudo Random Bit Pattern) = $2^n - 1$ (n=7)

Subject bit = DB9

Aggressors = DB8 and DB10 driven with random phase relative to DB9

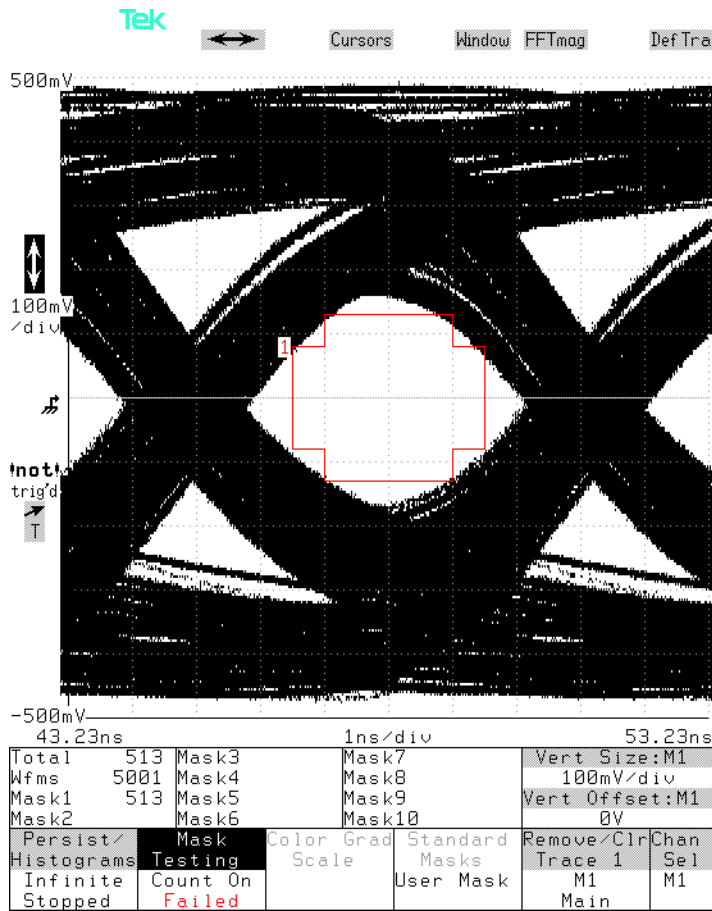
Tektronix 11801A Digital Sampling Scope (20GHz)

Probes = P6248 differential (1.7GHz)

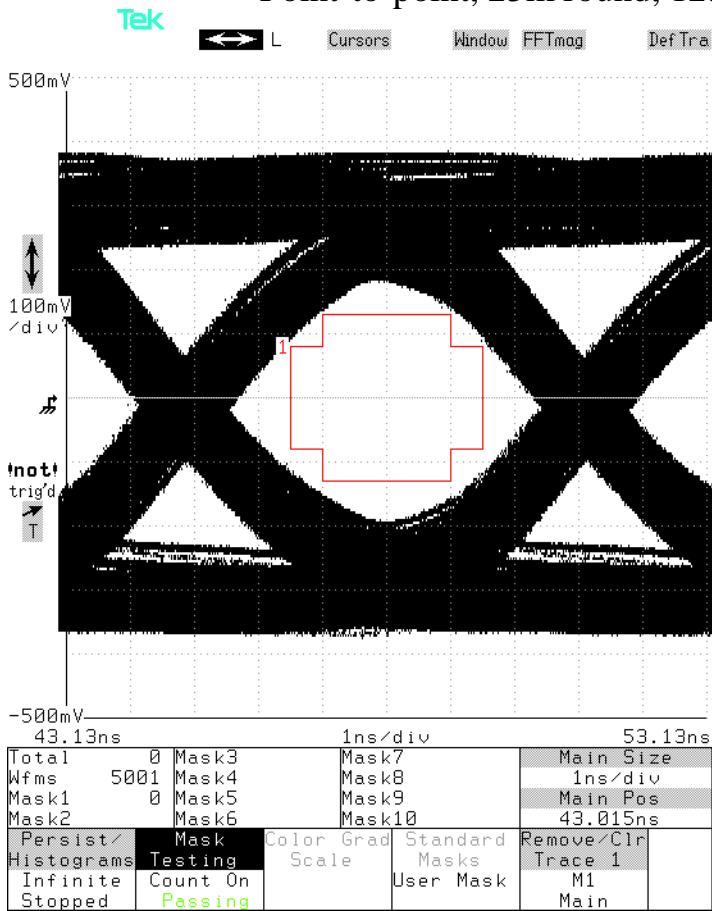
Configurations:

1. Point to point cable = Hitachi 25m round (HCM 48783)
2. 1m round Madison cable (28 AWG) to backplane (10 drive, slot 4)
3. 12m flat Hitachi cable (E15369) to backplane (10 drive, slot 4)

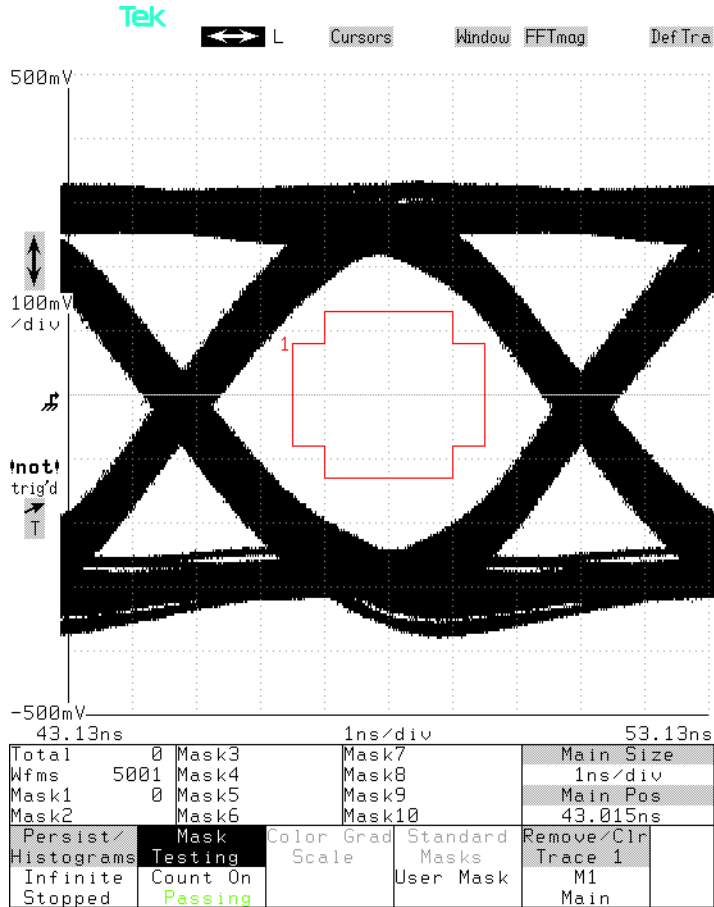
Point-to-point, 25m round, no precomp



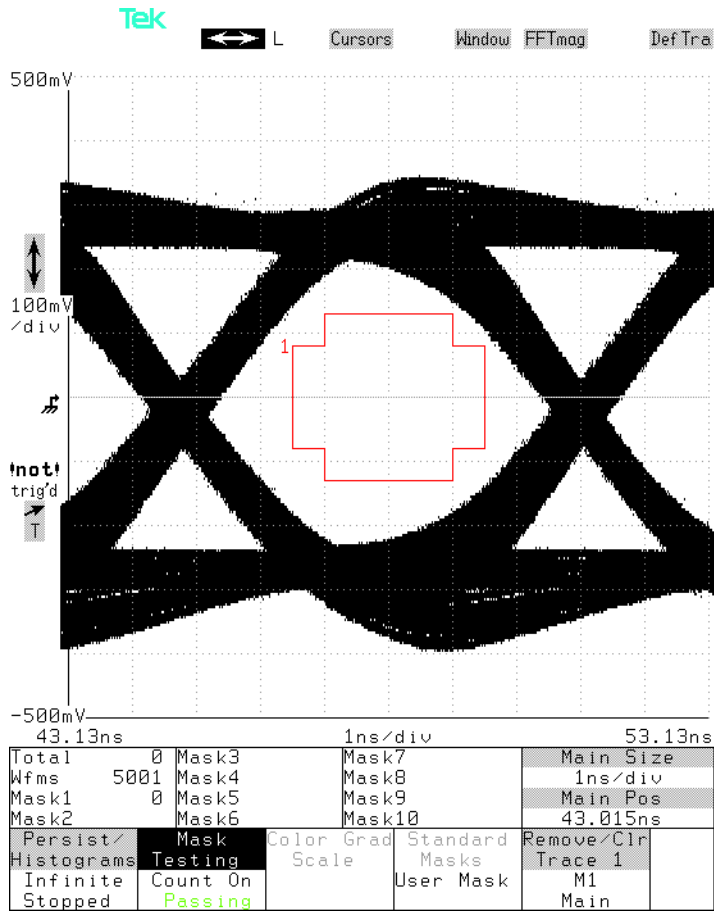
Point-to-point, 25m round, 12.5% precomp



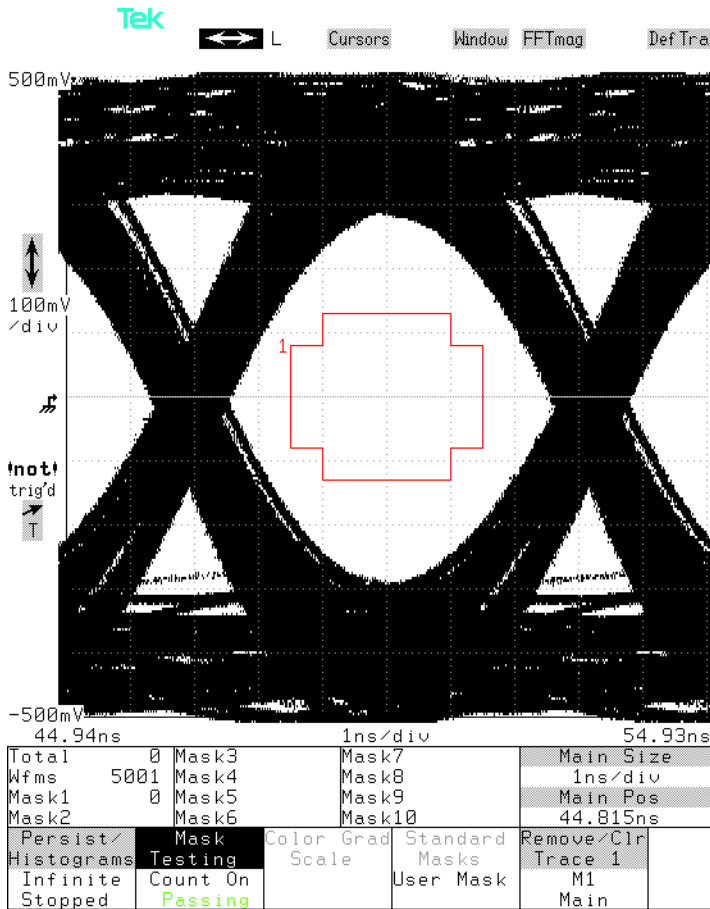
Point-to-point, 25m round, 25% precomp



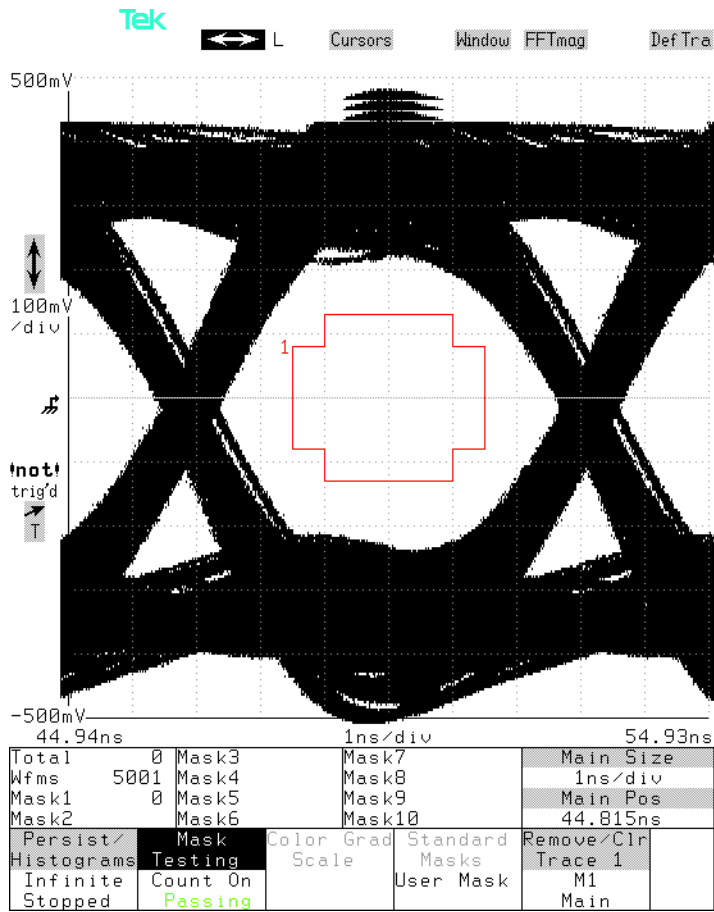
Point-to-point, 25m round, 33% precomp



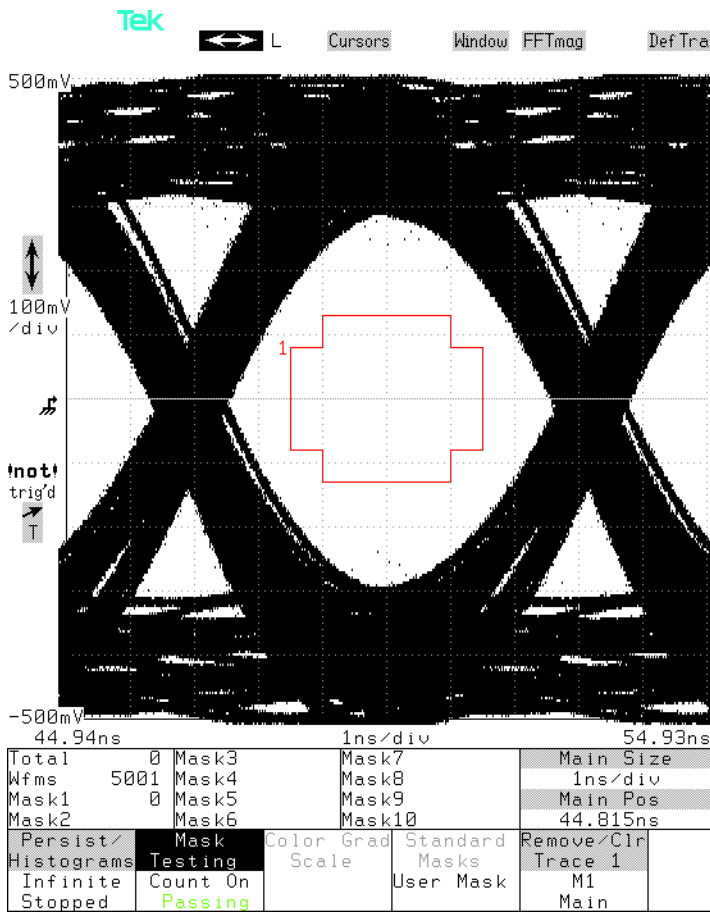
10 Drive backplane, 12m flat, no precomp



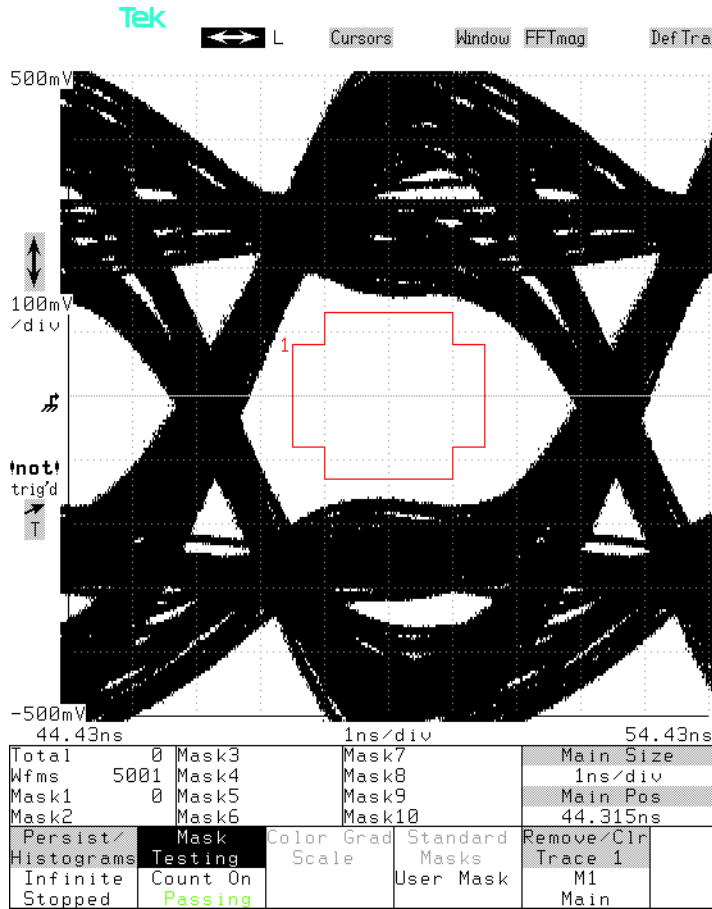
10 Drive backplane, 12m flat, 12.5% precomp



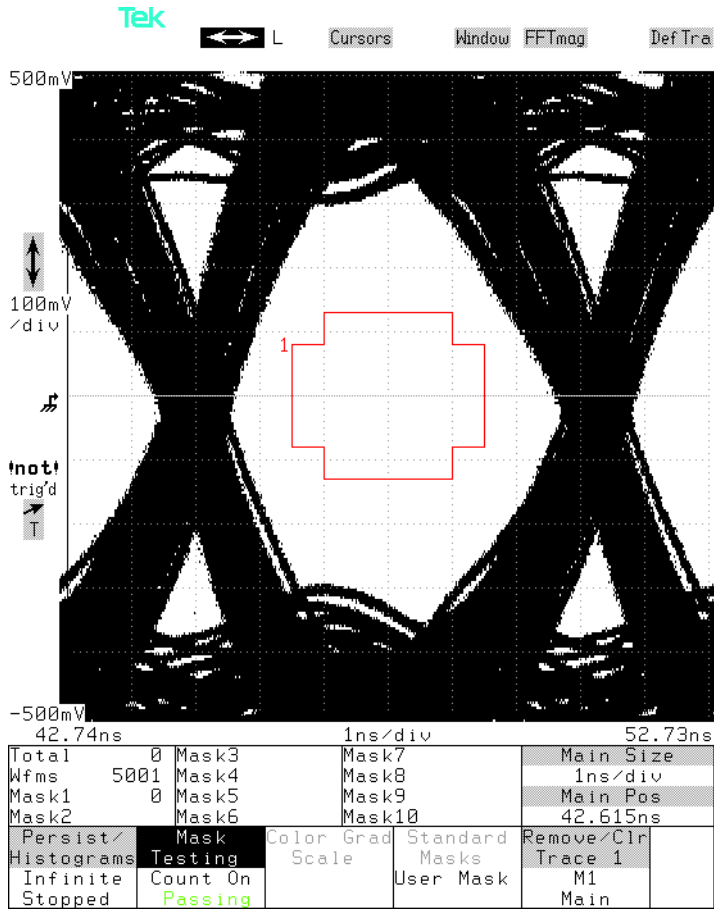
10 Drive backplane, 12m flat, 25% precomp



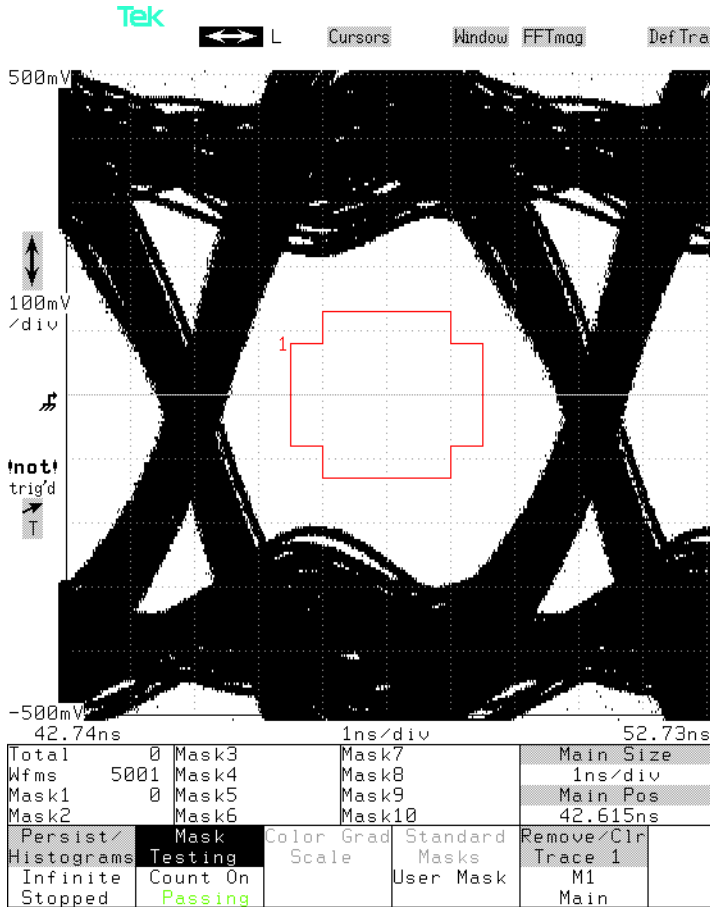
10 Drive backplane, 12m flat, 33% precomp



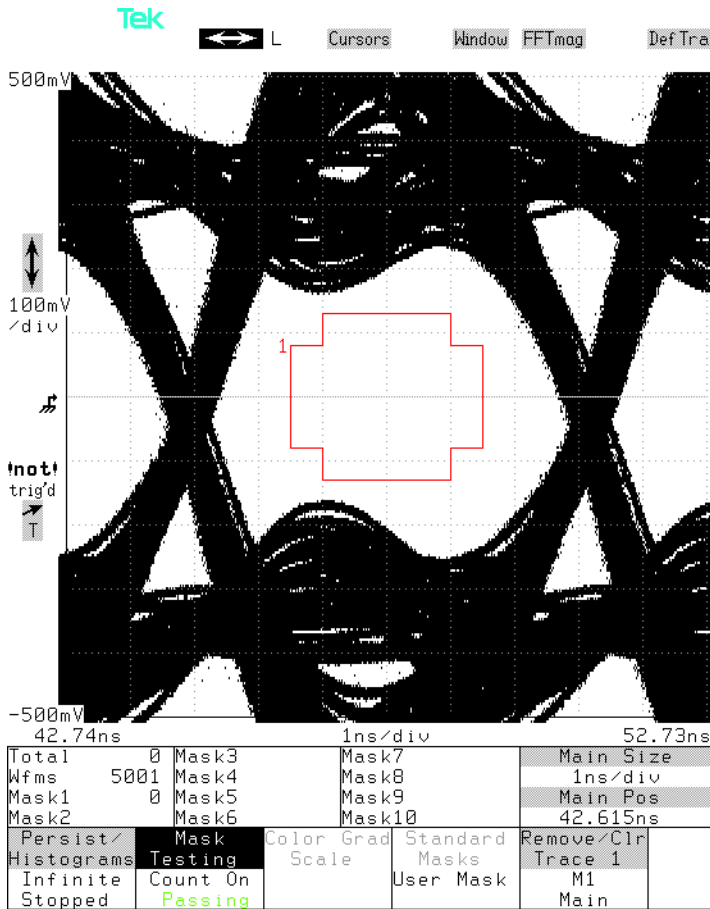
10 Drive backplane, 1m round, no precomp



10 Drive backplane, 1m round, 12.5% precomp



10 Drive backplane, 1m round, 25% precomp



10 Drive backplane, 1m round, 33% precomp

